Analytical Model of the Forward Operation of 4H-SiC Vertical DMOSFET in the Safe Operating Temperature Range

Authors

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ABSTRACT

With the purpose to provide an analytical instrument to design power DMOSFETs in 4H-SiC, capable to safely operate in the entire Forward Bias Safe Operating Area (FBSOA), in this paper a new analytical model of the device is presented. The model is capable to describe with closed form equations the forward DC current-voltage characteristics of the devices, including the parasitic resistance, the effects of the insulator-semiconductor interface traps on the threshold voltage and their temperature dependences. Numerical simulations have been used to verify the model in 200K temperature range and in presence of insulator-semiconductor interface trap density in the range [0;10^{14}] $cm^{-2}eV^{-1}$. Additionally, a model of the current temperature coefficient is derived which demonstrate that, differently than what usually observed for silicon, in 4H-SiC devices it is mandatory to account for both saturation and triode region of operations, for the series resistance and the change in the slope of the transfer characteristics caused by the interface traps. Comparisons with experimental data of a 1.7kV commercial device are used to validate the model.

Index Terms— Semiconductor device modeling, Silicon Carbide, DMOSFET, Thermal stability, Interface Traps

I. INTRODUCTION

The good performance of MOS devices in terms of switching capability and forward ohmic drop, in conjunction with the superior thermal conductivity and electric strength that Silicon Carbide (SiC) [1], [2], [3] exhibits with respect to Silicon (Si), have encouraged an intense research activity aimed to the development of 4H-SiC FET devices for power applications. At the present, 4H-SiC vertical DMOSFETs with Blocking Voltage (BV_{DSS}) to ON resistance (R_{DSON}) ratio in the range of kilovolt/ohm are commercially available [4], [5], as well as DMOSFET prototypes working in the range of 50kVA output power, [6], [7], credited to match silicon IGBTs in medium power applications [2]. An effective exploitation of such devices requires stable operations along the projected safe operating temperature range, typically $\Delta T = 150 - 200K$, to avoid thermal runaways and the consequent formation of hot spots in power modules [9]. It is well known [10] that the high thermal stability observed in Si MOS-like devices, during forward operations, is determined by the favorable trade-off between the negative temperature coefficients of the transconductance coefficient, K, and the threshold voltage, V_{TH}, which governs the temperature variation of the transfer characteristics, I_D-V_{GS}, and determines the points where current begins to decrease with the temperature. At low voltages the variation of the intrinsic carrier concentration, induced by the increment of the temperature, causes the reduction of V_{TH} and the unstable increment of the I_D-V_{GS} curves; while at slightly higher voltages, when the effect of the mobility reduction prevails, the transfer characteristics tend to interlace in a Zero Temperature Coefficient (ZTC) point, which brings to a thermally stable behavior. Based on these considerations, in [11]-[13] the repercussions of these effects on the Forward Bias Safe Operating Area (FBSOA) of Si DMOSFET have been quantitatively analyzed, by means of the temperature coefficient $\alpha_T = \frac{\partial I_{D,SAT}}{\partial T}$, where the saturation current $I_{D,SAT}$ accounts for the temperature dependence of the trans-conductance and the threshold voltage. Differently than silicon, the presence of a high trap DOS (Density Of States) at the insulator-semiconductor interfaces is yet a major concern in 4H-SiC, that strongly influences all the operation condition of MOS-like devices, from accumulation to strong inversion, determining phenomena like NBTI (Negative Bias Temperature Instability) [14], [15], [16]. During forward operations, in particular, the gradual fulfillment of the

acceptor-like traps as the Fermi level moves towards the lower limit of the conduction band, E_C, causes a positive shift of V_{TH} and a macroscopic increment of the I_D-V_{GS} curves slope, which completely change the electrical conditions of the intrinsic electro-thermal stability (α_T<0) with respect to what usually observed in silicon devices [17]. Furthermore, in [3] a more pronounced current increment in 4H-SiC MOSFETs with the temperature than that usually observed in similar Si devices has been observed, whose dominant mechanism has been attributed to the increment of the free carrier density in the channel region, due to the ionization of the interface traps as the temperature increases. These conclusions are also confirmed by the experimental data of commercial devices, (for example [4], [5]) that report I_D-V_{GS} curves intersecting in both saturation and triode regions of operation, where the parasitic series resistance, and its thermal variation, plays a fundamental role. Such role has been qualitatively observed in [18], where the increment of the parasitic series resistance as the temperature increases can mask the variation of the channel resistance in a way not observable in silicon devices. From the aforementioned considerations, it follows that, contrarily to what stated in [12], in spite of the good thermal properties of SiC, the achievement of the electro-thermal stability is a critical aspect to be adequately modeled and dimensioned. Since the existing analytical models developed for silicon DMOSFETs assume a good quality of insulator-semiconductor interface layer, they cannot be directly applied to SiC, while Spice-like numerical and mixed numerical-analytical models, recently proposed in the literature [6], [19], [20] for their nature to be targeted to specific devices, are not sufficiently general to provide a comprehensive model. Existing physically-based models of 4H-SiC devices [21], [22] do not account for the effects of the interface traps on the threshold voltage. Additionally, freely available Spice models of commercial devices [4] do not describe correctly the electro-thermal operations of the devices, returning intersection points at much lower currents and voltages than those shown in the related datasheets. In this paper, for the first time in the literature, an analytical model of the 4H-SiC DMOSFET is presented which is able to express with closed form equations the forward DC current-voltage characteristics of the devices, including all the key physical parameters and their temperature dependence, like the parasitic resistance and the effects of the insulator-semiconductor interface traps on the threshold voltage. Comparisons with numerical simulations [23] demonstrate that the model is capable to predict the behavior of 4H-SiC

vertical DMOS transistor in all the projected safe operating temperature range and with different interface trap density. Furthermore, simple formula are derived from the current-voltage model for the analysis of the intrinsic stability of 4H-SiC DMOSFETs, when the device is forward biased, which account for both saturation and triode region of operations, for the series resistance and the curve sloping effect. Comparisons with experimental data of commercial devices [24] in a wide range of temperatures validate the model. The paper is organized as follows: in section II the model is presented; in section III the model is verified by comparisons with numerical simulations and experimental data; section IV concludes the paper.

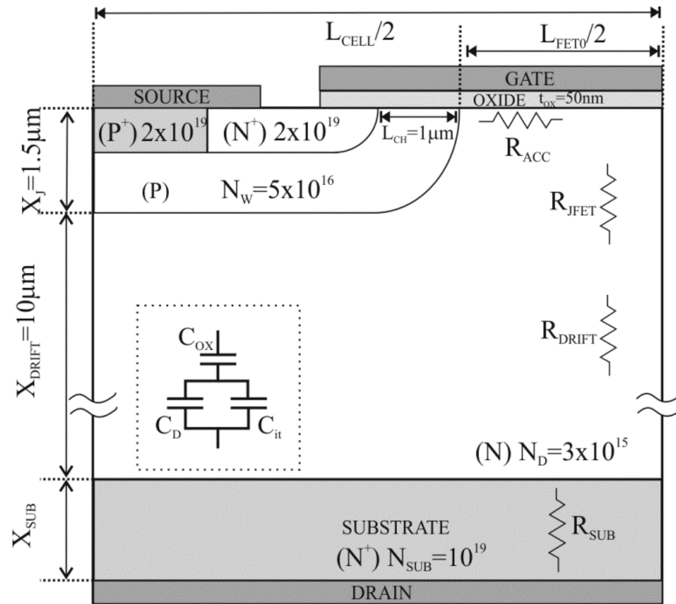

Fig. 1: Half structure of the reference devices. The inset shows the equivalent capacitances associated to the channel region under equilibrium conditions: the insulator capacitance C_{OX}, the diffusion capacitance C_D and the capacitance associated to the interface traps, C_{it}.

II. ANALITYCAL MODEL

A simplified scheme of the half 4H-SiC DMOS cell, used as reference device for our analysis, is shown in Fig. 1, along with the notations of the main doping densities and geometries. Although a unified MOSFET model valid with continuity from weak to strong inversion has been proposed so far for Spice modeling of Si MOSFETs [12], [25], the Level 1 voltage-current equations have been chosen as the starting-point of the proposed model for the possibility to obtain all the equations in, closed form and to evidence the separate contributions of the different operation regions:

$$I_{DS} = \begin{cases} 0 \quad \text{for } V_{GS,Int} < V_{TH} \\ K_n \left[2\left(V_{GS,Int} - V_{TH}\right) V_{DS,Int} - V_{DS,Int}^2 \right] \text{ for } V_{DS,Int} \le V_{GS,Int} - V_{TH} \\ \frac{K_n}{2} \left(V_{GS,Int} - V_{TH}\right)^2 \left(1 + \lambda V_{DS,Int}\right) \quad \text{for } V_{DS,Int} > V_{GS,Int} - V_{TH} \end{cases} \tag{1}$$

where K_n and V_{TH} are the transconductance parameter and the threshold voltage, respectively, λ is the channel length modulation coefficient, and $V_{GS,Int}$, $V_{DS,Int}$ are the intrinsic voltages, applied across the channel region, obtained by reducing the terminal voltages by the parasitic ohmic drops:

$$\begin{aligned} V_{GS,Int} &= V_{GS} - R_S \times I_D \approx V_{GS} \\ V_{DS,Int} &= V_{DS} - R_{TOT} \times I_D \end{aligned} \tag{2}$$

In (1) the subthreshold behavior has been intentionally omitted for the negligible effects on the forward operations and to the determination of the forward electro-thermal stability condition. In (2), for the small geometries and high doping level, the parasitic series resistance of the source region, R_S, has been neglected. The resistance, R_{TOT} , groups all the parasitic ohmic contributions from the *n*-side channel limit to the drain contact. As schematized in Fig. 1, it has been calculated as the series of four resistances associated to as much device regions: that associated to the JFET portion of the epilayer, between the two *p*-wells, R_{JFET}; the drift resistance, R_{DRIFT}, associated to the part of the epilayer between the JFET portion and the substrate; the resistance associated to the substrate, R_{SUB}; the resistance describing the accumulation channel, R_{ACC}, that originates under the gate insulator in the *n* region next to the channel. With reference to the notations in Fig. 1, $R_{TOT} = R_{ACC} + R_{JFET} + R_{DRIFT} + R_{SUB}$ where [26]:

$$\begin{aligned} R_{ACC} &= \frac{L_{FET0}}{W C_{OX} \mu_{na} \times \left(V_{GS} - V_{TH}\right)} \\ R_{JFET} &= \frac{1}{q \mu_{nn} N_{EPI}} \times \frac{X_J + W_{SCV}}{W \times L_{FET}} \\ R_{DRIFT} &= \frac{1}{q \mu_{nn} N_{EPI} W \times L_{CELL}} \times \left[X_{DRIFT} + \frac{L_{FET} - L_{CELL}}{2} \right] \\ R_{SUB} &= \frac{1}{q \mu_{n,sub} N_{SUB}} \times \frac{W_{SUB}}{W \times L_{CELL}} \end{aligned} \tag{3}$$

where W is the device width, μ_{na} , μ_{nn} , $\mu_{n,sub}$ are the concentration dependent mobilities of the accumulation layer, the epitaxial layer and the substrate, respectively, which have been modelled by the same expression employed in [27] for a 4H-SiC *p-i-n* diode, together with the parameters extracted by the measurements in [28]. The extension of the space charge region (scr) into the epitaxial layer, along the vertical direction of the device has been described as $W_{SCV} = \sqrt{\frac{2\varepsilon}{qN_{EPI}} \times \left[V_T \ln\left(\frac{N_W N_{EPI}}{n_i^2} \right) + \frac{X_J}{X_J + X_{DRIFT}} V_{DS} \right]}$, where V_T is the thermal voltage and the dependence on V_{DS} has been weighted by the ratio $\frac{X_J}{X_J + X_{DRIFT}}$ to account for the vertical voltage drop, assumed linear from the substrate to the bottom of the *p*-region; $L_{FET} = L_{FET0} - 2W_{SCV}$ is the width of the JFET region, calculated in terms of the metallurgical width, L_{FET0}, decremented by the extension of the scr. By using (2), (3), eq. (1) can be rewritten in terms of the terminal voltages and the parasitic resistances as:

$$I_{DS} = \begin{cases} 0 \quad \text{for } V_{GS} < V_{TH} \\ R_{TOT}^{-1} \left(V_{DS} - V_{GS} + V_{TH} - \frac{1}{K_n R_{TOT}} \right) + \sqrt{\left(\frac{1}{K_n R_{TOT}^2} + \frac{V_{GS} - V_{TH}}{R_{TOT}} \right)^2 - 2 \frac{V_{DS}}{K_n R_{TOT}^3}} \quad \text{for } V_{DS} \le V_{GS} - V_{TH} \\ \frac{K_n \left(V_{GS} - V_{TH} \right)^2 \left(1 + \lambda V_{DS} \right)}{2 + K_n \left(V_{GS} - V_{TH} \right)^2 \lambda R_{TOT}} \quad \text{for } V_{DS} > V_{GS} - V_{TH} \end{cases} \quad (4)$$

The temperature dependence of the transconductance coefficient has been expressed as $K_n = K_{n0} \times \left(\frac{T}{300} \right)^{-1.5}$ with $K_{n0} = \mu_{n,CH} C_{OX} \frac{W}{L_{CH}}$, where the field dependent channel mobility, $\mu_{n,CH}$, has been expressed in terms of the mean value of the electric field in the channel, E_m, calculated from the channel charge density:

$$\mu_{n,CH} = \frac{\mu_{n0,CH}}{\left[1+\left(\frac{\mu_{n0,CH} E_m}{v_{SAT}}\right)^{\beta}\right]^{1/\beta}}$$

with

$$E_m = \frac{1}{\varepsilon_{SiC}}\left[\sqrt{2q\varepsilon_{SiC} N_W \Psi_{S0}} + 0.5C_{OX}\left(V_{GS} - V_{TH}\right)\right]$$

where β=2, the saturation velocity $v_{SAT} = 2\times10^7 cm\times s^{-1}$ and the surface potential at the beginning of the strong inversion is $\Psi_{S0} = 2V_T \ln\left(\frac{N_W}{n_i}\right)$. The $\mu_{n0,CH}$ value has been imposed constant to $100 cm^2V^{-1}s^{-1}$, in order to obtain $\mu_{n,CH}$ values consistent with those measured in the literature [21], [29], usually limited in the range [20;50] $cm^2V^{-1}s^{-1}$ by the current process quality.

2.1 Threshold Voltage

The threshold voltage, V_{TH}, has been modelled by using the well-known equation derived in the case of a fully depleted channel:

$$V_{TH} = V_{FB} + \Psi_{S0} + \frac{qN_W}{C_{OX}}\sqrt{\frac{2\varepsilon_{SiC}}{q}\frac{\Psi_{S0}}{N_W}} - V_{it} \quad (5)$$

where $V_{it} = \frac{Q_{it}}{C_{OX}}$ is the voltage shift due to the oxide-semiconductor interface charge, Q_{it}, and the flat-band voltage $V_{FB} = \Phi_m - \chi - V_{th}\ln\left(\frac{N_W}{n_i}\right) - \frac{V_{G0}}{2}$ is expressed in terms of the gate metal work-function, Φ_m, the 4H-SiC electron affinity, χ, and the band-gap at T=300K, V_{G0}.

According to the results in [14], [30], the total DOS, D_{it}, due to the traps at the insulator-semiconductor interface, has been modeled as the superposition of four energy bands, symmetrically placed with respected to the center of the band-gap, which therefore results the neutral energy level. An exponential-shape tail band for the acceptors has been located in the upper half of the band-gap, $D_{it,TA}\left(E_t\right)$, and a symmetrical one for donors in the lower half, $D_{it,TD}\left(E_t\right)$, and one acceptor and one

donor Gaussian bands have been placed near the mid-gap, symmetrically around the neutral energy level, $D_{it,GA}(E_t)$, $D_{it,GD}(E_t)$:

$$\begin{aligned} &D_{it}(E_t) = D_{it,TA}(E_t) + D_{it,TD}(E_t) + D_{it,GA}(E_t) + D_{it,GD}(E_t) \\ &\text{where} \\ &D_{it,TA}(E_t) = D_{it,T0} e^{\frac{Et-E_C}{WTA}} ;\; D_{it,TD}(E_t) = D_{it,T0} e^{\frac{E_V-Et}{WTD}} \\ &D_{it,GA}(E_t) = D_{it,G0} e^{-\left(\frac{0.805-Et}{EGA}\right)^2} ;\; D_{it,GD}(E_t) = D_{it,G0} e^{-\left(\frac{Et-0.805}{EGD}\right)^2} \end{aligned} \tag{6}$$

As shown in [30], the current process technology can be adequately simulated by imposing in (6) $D_{it,T0} = 10^{14} cm^{-2} eV^{-1}$ and $WTA = WTD = 0.1eV$, while $D_{it,G0} = 10^{11} cm^{-2} eV^{-1}$ and $EGA = EGD = 1eV$ are chosen to make very flat the related Gaussian shapes, in order to approximate an almost constant distribution near the neutral energy level. Since our analysis considers the strong inversion operation region, which locates the Fermi level in the upper half of the band-gap, near the conduction band, the charge generated by the ionization of the donor trap states is several order of magnitude lower than that related to the acceptor-like traps. Therefore, the two Gaussian defect distributions significantly influence the device operation only in accumulation and weak inversion, so that (6) can be reduced to $D_{it}(E_t) \approx D_{it,TA}(E_t)$. The related variation of the threshold voltage, $V_{it} = -q \frac{N_{a,it}}{C_{OX}}$, is calculated in terms of the ionized acceptor traps, $N_{a,it}$:

$$N_{a,it} = \int_{E_V}^{E_C} D_{it}(E_t) f(T, E_t) dE_t \tag{7}$$

where $f(T, E_t) = \frac{1}{1 + \frac{n_i}{n_S} e^{\frac{Et-Ei}{k_B T}}}$ is the Fermi distribution of probability under the approximation of a fully depleted channel, n_S is the electron density at the insulator-semiconductor interface, and the other symbols have their usual meanings. Equation (7) makes V_{TH} strongly dependent on the Fermi level position, E_F, and hence on the surface potential and gate bias voltage, which make impossible to find an analytical, exact solution to (5). To overcome this problem, an approximate solution of (7) in three sequential steps has been found by approximating $f(T, E_t)$ to a step probability density function with

finite values in the energy range [$E_V;E_F$]. This approximation is used in (7) to calculate the ionized trap density at the beginning of the strong inversion as $N_{a,it0} = D_{it,T0} \times WTA \times e^{\frac{\Psi_{S0}-V_{G0}}{2WTA}}$, and from this the threshold voltage at the same operation conditions: $V_{TH0} = V_{FB} + \Psi_{S0} + \frac{qN_W}{C_{OX}}\sqrt{\frac{2\varepsilon_{SiC}}{q}\frac{\Psi_{S0}}{N_W}} + q\frac{N_{a,it0}}{C_{OX}}$. Once V_{TH0} has been calculated, the dependence of the electron concentration at the insulator-semiconductor interface, n_S, from V_{GS} is estimated as in [31] by assuming an exponential dependence at low voltage values which approaches to a linear dependence as the voltage increases:

$$n_S\left(V_{GS}\right) = N_W \ln\left(1 + e^{\frac{V_{GS}-V_{T0}}{C\times V_T}}\right) \tag{8}$$

In (8), $C = 1 + \frac{C_D + C_{it}}{C_{OX}}$ is the divider of the gate-channel equivalent capacitances, schematized in the inset of Fig. 1, which, under stationary conditions, involves the insulator capacitance $C_{OX} = \frac{\varepsilon_{OX}}{t_{OX}}$, the depletion layer capacitance, $C_D = \sqrt{\frac{q\varepsilon_{SiC}N_W}{4V_T\ln\left(N_W/n_i\right)}}$ and the capacitance related to the trap DOS, C_{it}.

This last contribution has been estimated as the average of the total trap density between E_V and E_F as $C_{it} = q\bar{D}_{it} = \frac{q}{E_F - E_V}\int_{E_V}^{E_F} D_{it}\left(E_t\right)dE_t \approx \frac{2qD_{it,T0}WTA}{M\left(V_{GS} - V_{TH0}\right) + V_{G0}/2}$, where M is given by the same capacitance divider except C_{it}: $M = \frac{C_{OX}}{C_D + C_{OX}}$. Finally, the ionized acceptor trap density is calculated by using (8) in the integral of (7), thus obtaining $N_{a,it} = D_{it,T0} \times WTA \times \left(\frac{n_S}{N_C}\right)^{\frac{V_T}{WTA}}$ which finally allows the recalculation of the threshold voltage $V_{TH} = V_{FB} + \Psi_{S0} + \frac{qN_W}{C_{OX}}\sqrt{\frac{2\varepsilon_{SiC}}{q}\frac{\Psi_{S0}}{N_W}} + q\frac{N_{a,it}}{C_{OX}}$.

It is worth noting that, although the band-gap narrowing and partial ionization have been considered [27], their effects on the 4H-SiC DMOSFET are negligible because of the typical doping levels employed for the channel region.

III. RESULTS AND DISCUSSIONS

The proposed model has been compared with numerical simulations of the device in Fig. 1, whose $3\times10^{15}cm^{-3}$doped, $10\mu m$ thick drift layer is consistent with 1200V blocking voltage of most diffused commercial DMOSFETs in 4H-SiC. Results of the comparisons refer to a structure having $W=1\mu m$ and L_{FET0} =$5\mu m$, so that R_{JFET} value is such as not to mask the other resistance contributions, although it is still relevant.

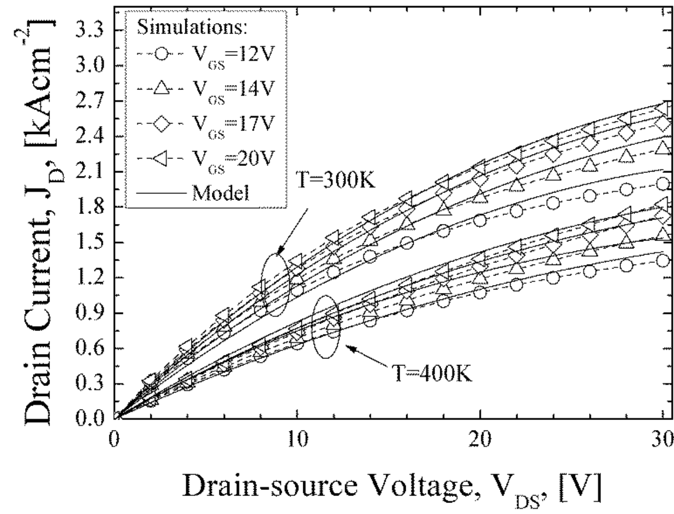

Fig. 2: Model-simulation comparisons of the output characteristics of the device of Fig. 1 at T=300K and T=400K, in absence of insulator-semiconductor interface traps.

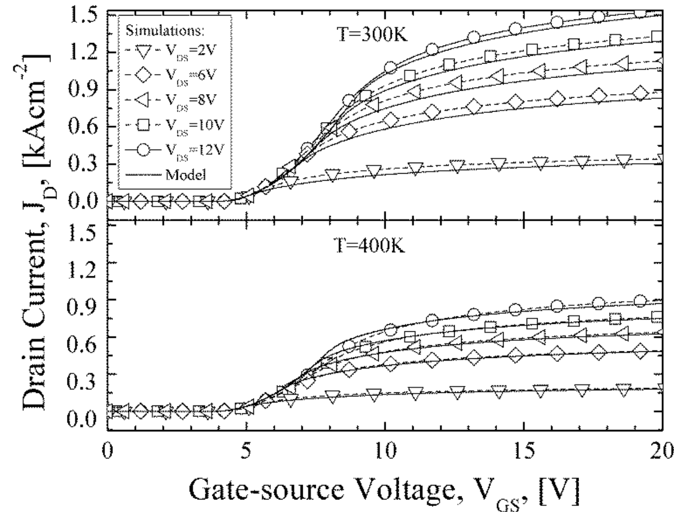

Fig. 3: Model-simulation comparisons of the transfer characteristics of the device of Fig. 1 at T=300K and T=400K, in absence of insulator-semiconductor interface traps.

With the purpose to verify (3) and (4), in Fig. 2 and 3 model and simulations of the I_D-V_{DS}, I_D-V_{GS} curves, taken at T=300K and T=400K, are compared when the interface trap density is null $\left(D_{it}\left(E_t\right)=0\right)$. It's interesting to observe in Fig. 3, the modest variation of the threshold voltage from 4.22V at 300K to 4.1V at 400K, as well as the reduced variation of the I_D-V_{GS} slopes. On the contrary, the effects on the curves of the parasitic series resistance becomes evident suddenly as the device operates in triode region, which also justifies the low slopes of the output curves observed in Fig. 2. In Fig. 4, the comparison of I_D-V_{GS} curves of Fig. 3, taken at V_{DS}=2V and V_{DS}=12V, reveals an intersection points located in the saturation region at ($5V$, $37.2Acm^{-2}$), coincident for both V_{DS} values. The negative temperature coefficient shown by the transfer characteristics at such very low current and voltage values verifies that, in presence of gate oxide of good quality, DMOSFETs exhibit a very high forward electro-thermal stability, thanks to the favorable temperature dependence of the channel resistance, ensured by trade-off between the reduction with the temperature of threshold voltage and the mobility.

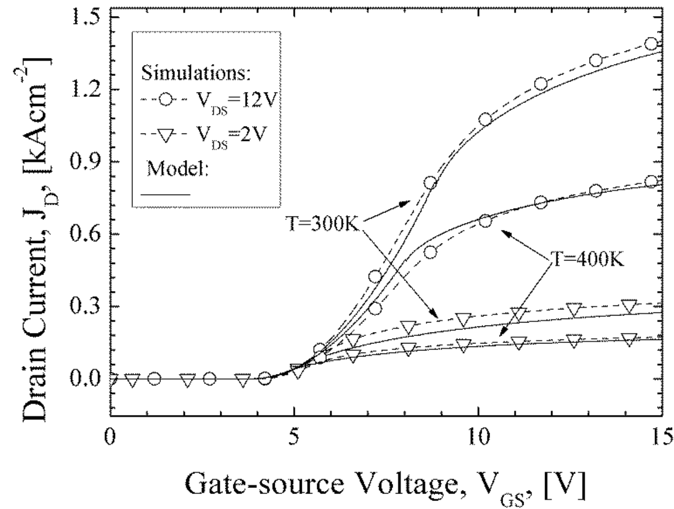

Fig. 4: Comparisons of the transfer characteristics taken at T=300K and T=400K when V_{DS}=2V and V_{DS}=6V. In absence of interface traps the intersection points is at very low voltage and current values.

The accuracy of (7) to calculate the ionized interface trap density at ambient temperature is shown in Fig. 5, where $N_{a,it}$ as a function of the gate voltage is reported, at T=300K, when $D_{it,T0}=10^{13}cm^{-2}eV^{-1}$ and $D_{it,T0}=10^{14}cm^{-2}eV^{-1}$. The effect of $N_{a,it}$ on the threshold voltage is shown in

Fig. 6, where model-simulation comparisons of I_D-V_{GS} curves show the skews of the transfer characteristics when $D_{it,T0}$ is increased to 10^{13} and $10^{14} cm^{-2}eV^{-1}$. Comparison of the curves in Fig. 3 and 6 shows that, at T=300K, a trap density of $D_{it,T0} = 10^{13} cm^{-2}eV^{-1}$ induces a very small V_{TH} variation ($\Delta V_{TH} = 0.5V$), while the increase of the trap density to $D_{it,T0} = 10^{14} cm^{-2}eV^{-1}$, and hence of the corresponding $N_{a,it}$ in Fig. 5, shifts V_{TH} up to $9V$ ($\Delta V_{TH} = 4.78V$).

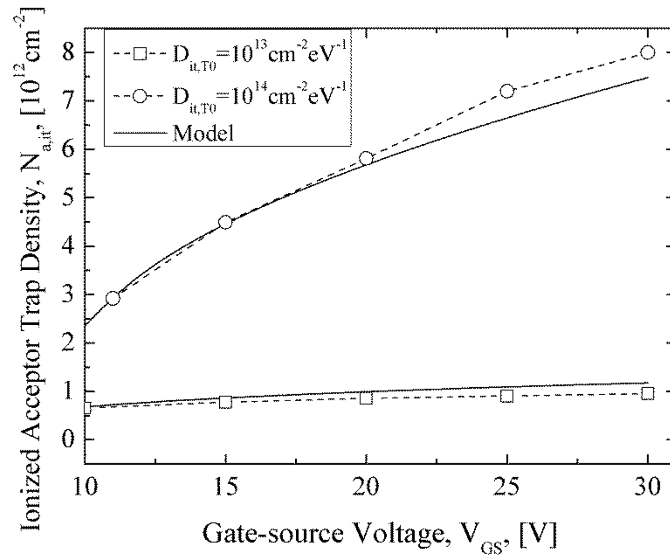

Fig. 5: Model-simulation comparisons of the ionized interface traps Na,it when the trap DOS varies from 10^{13} and 10^{14} $cm^{-2}eV^{-1}$

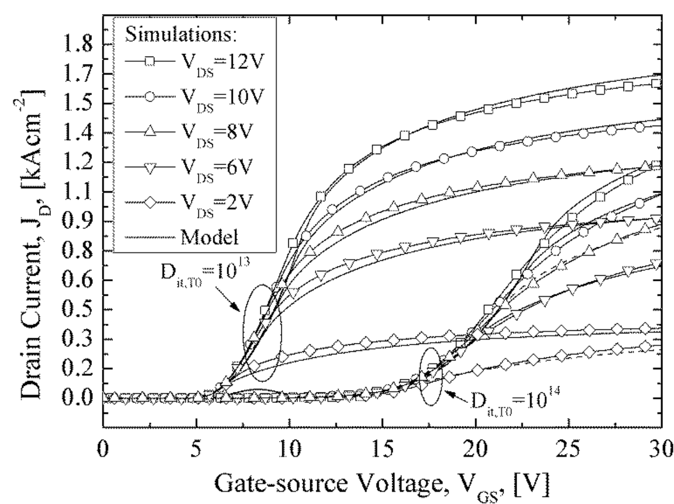

Fig. 6: Model-simulation comparisons of the transfer characteristics when the trap DOS varies from 10^{13} and 10^{14} $cm^{-2}eV^{-1}$

The accuracy of the model in describing the temperature dependence of the characteristics is verified in Fig. 7-9, where model-simulation comparisons of the I_D-V_{GS}, I_D-V_{DS}, and $N_{a,it}$ are shown when $D_{it,T0} = 10^{14} cm^{-2} eV^{-1}$ and the temperature increases from T=300K of the previous figures to 400K and 500K, thus involving a temperature range $\Delta T = 200K$ which, for the base of our knowledge, is the largest safe range reported for commercial 4H-SiC DMOSFET [32]. In spite of the simplifications stated in the previous section to analytically solve (7), it is particularly relevant the accuracy of the model in Fig. 6, 7 to describe the negative temperature coefficient of V_{TH}, caused by the reduction of the ionized trap density, modeled in Fig. 9, when the temperature increases. The slight differences of the simulated output characteristics with respect to the model in Fig. 8, in correspondence to the saturation-triode transitions, are due to the piece-wise current-voltage model (4) as typically observable in Spice simulations using the same model Level.

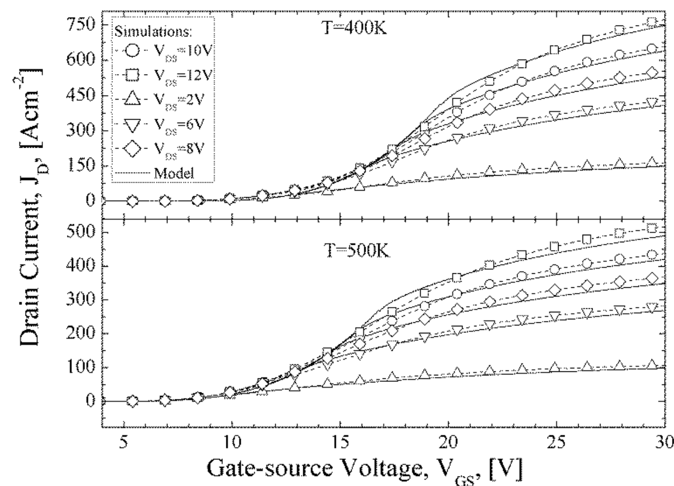

Fig. 7: Model-simulation comparisons of the transfer characteristics of the device of Fig. 1 at T=400K and T=500K, when the

trap DOS is 10^{14} $cm^{-2}eV^{-1}$

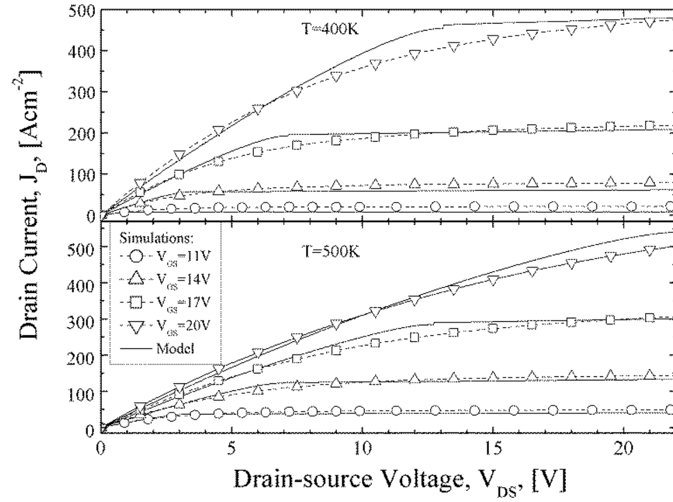

Fig. 8: Model-simulation comparisons of the output characteristics of the device of Fig. 1 at T=400K and T=500K, when the trap DOS is 10^{14} cm^{-2}eV^{-1}

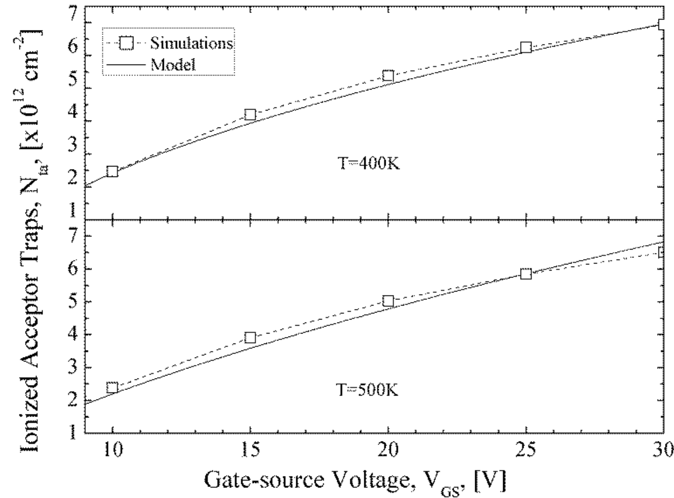

Fig. 9: Model-simulation comparisons of the ionized interface traps Na,it when the trap DOS is 10^{14} cm^{-2}eV^{-1} and the temperature varies from T=400K to T=500K.

In order to better show the peculiar behavior of the 4H-SiC DMOSFET, in Fig. 10 the same I_D-V_{GS} curves of Fig. 6, 7 at T=300K and T=500K, taken at V_{DS}=2V and V_{DS}=12V, are compared. Because of the low quality of the insulator-semiconductor interface, the curves intersect at much higher voltage and current values with respect to the ideal condition of Fig. 4. The above figures show that stable operations of the SiC devices require an adequate dimensioning for the fundamental role played by the parasitic series resistance in determining the current-voltage points where the currents begin to exhibit a negative temperature coefficient and avoid thermal runaways.

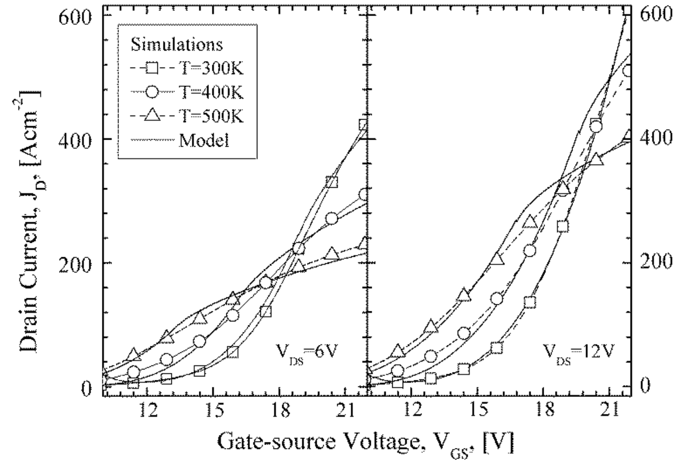

Fig. 10: Intersection of the transfer characteristics at T=300, 400 and 500K at V_{DS}=6V and V_{DS}=12V.

Curves in Fig. 10 also show that the locations of the intersection points are both bias and temperature dependent, so that both the saturation and the triode region of operations can be interested. This is shown, for example, by the curves at $V_{DS}=12V$ and T=400K, whose intersection point with the curve at T=500K is at ($19V$, $330Acm^{-2}$), corresponding to a saturation point for the curve at T=400K and to a triode operation point for the curve at T=500K; as well as the curves at $V_{DS}=6V$ and T=300K and 400K which intersect in ($19V$, $220Acm^{-2}$), namely the saturation and triode operation point for the curve at lower and higher temperature, respectively. The aforementioned substantial differences of 4H-SiC operations with respect to the silicon counterpart suggest the re-calculation of the current temperature coefficient, $\alpha_T = \frac{\partial I_D}{\partial T}$, in order to include the trap-induced effects and the parasitic resistance contribution.

Since the device surely operates in stable conditions when the current decreases with the temperature increment, the intrinsic forward stability limit can be determined by imposing $\alpha_T \leq 0$. By using (4), the thermal coefficient α_T can be calculated as:

$$\alpha_T = \frac{\partial I_D}{\partial T} = \begin{cases} 0 \quad \text{for } V_{GS} < V_{TH} \\ \dfrac{\left[-\dfrac{m}{T} - K_n\left(V_{GS} - V_{TH} - V_{DS}\right)\times\dfrac{\partial R_{TOT}}{\partial T}\right]\times I_D - V_{DS}\times\dfrac{\partial V_{TH}}{\partial T}}{1 + K_n\left(V_{GS} - V_{TH} - V_{DS}\right)R_{TOT}} \quad \text{for } V_{DS} \le V_{GS} - V_{TH} \\ \dfrac{-\dfrac{m}{T}I_D - \sqrt{2K_n I_D\left(1+\lambda V_{DS}\right)}\times\dfrac{\partial V_{TH}}{\partial T} - I_D^2\dfrac{\lambda}{1+\lambda V_{DS}}\times\dfrac{\partial R_{TOT}}{\partial T}}{1 + \dfrac{K_n}{2}\left(V_{GS} - V_{TH}\right)^2\lambda R_{TOT}} \quad \text{for } V_{DS} > V_{GS} - V_{TH} \end{cases} \tag{9}$$

with $\frac{\partial K_n}{\partial T} = -K_n\frac{m}{T}$ where m=1.5 governs the temperature dependence of the transconductance parameter; $\frac{\partial R_{TOT}}{\partial T}$ has been calculated by differentiating the four components of (3) and the temperature derivative of the threshold voltage has been calculated, by neglecting the band-gap narrowing effect, in terms of $\frac{\partial V_{FB}}{\partial T} = -\frac{V_T}{T}\ln\left(\frac{N_W}{n_i}\right) + \frac{V_T}{2T}\left(3 + \frac{V_{G0}}{V_T}\right)$, $\frac{\partial \psi_{S0}}{\partial T} = \frac{n_i}{T}\left(3 + \frac{V_{G0}}{V_T}\right)$, $\frac{\partial N_{a,it}}{\partial T} = N_{a,it}\times\left[\frac{V_{th}}{WTA\times T}\ln\left(\frac{n_S}{N_C}\right) - \frac{V_{th}}{V_{GS}-V_{T0}}\left(\frac{V_{GS}-V_{T0}}{T} + \frac{\partial V_{T0}}{\partial T}\right)\right]$.

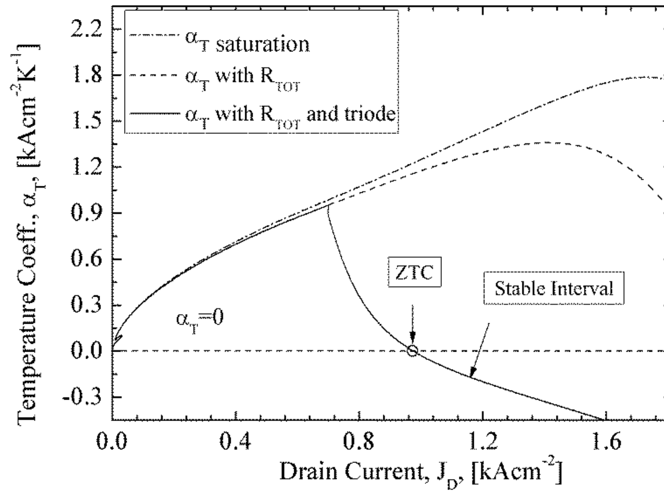

Fig. 11: Comparisons of α_T calculated by ignoring the triode region of operations and the parasitic ohmic drop, with that accounting only for the ohmic drop in the saturation region and the complete model (9), when V_{DS}=12V.

Fig. 11 shows the comparison between the proposed model (9), and the α_T curve as usually calculated for the analysis silicon devices, namely by considering the saturation region only and

neglecting the ohmic contribution [8], [11]. For completeness, also an intermediate α_T curve has been reported, calculated by (9) by accounting for the saturation current only. Considering that the curves in Fig. 6, at V_{DS}=12V and $D_{it,T0}=10^{14}cm^{-2}eV^{-1}$, shows that the drain current increases to J_D=1.21$kAcm^{-2}$ when V_{GS}=30V, it is evident that only the model (9) returns a realistic electro-thermal stability point, placed at $J_D^*=966Acm^{-2}$. The comparisons in Fig. 11 also show that the pronounced ohmic drop in triode region, observed in the transfer characteristics of Fig. 6, 7, 10, returns a stability interval much larger than that estimated by the other coefficients. This result demonstrates the significance of the parasitic ohmic drop in the electro-thermal stability analysis and, substantially, confirms what supposed by the authors in [18] about the capability of the series resistance to vary and, eventually, completely mask the channel resistance variation with the temperature. It is worth noting that, for the capability to describe the aforementioned dependences, (9) can be usefully employed also as a design instrument, by which it is possible to tune, for example, the epitaxial layer geometries and doping to improve the thermally stable operation range.

In order to experimentally validate the model, in Fig. 12, 13 the I_D-V_{GS}, I_D-V_{DS} curves are compared with those of the device [24]. The axis ranges of Fig. 12, 13 have been chosen according to those reported in the datasheet.

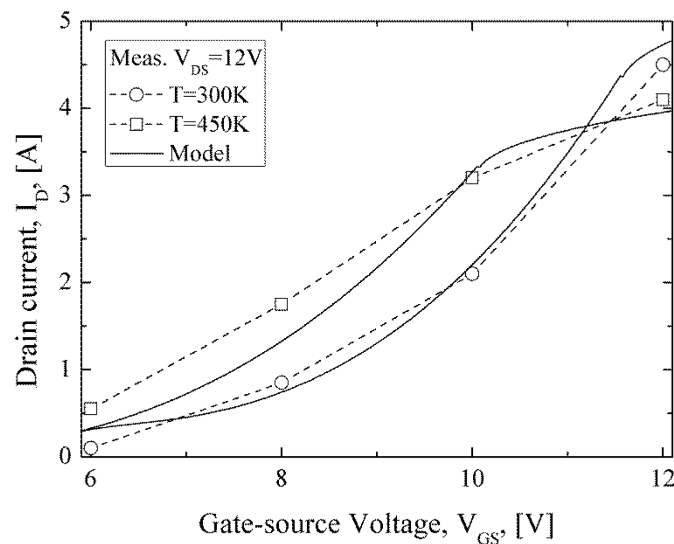

Fig. 12: Comparison of the model with the experimental transfer characteristics of the commercial device [24], at V_{DS}=12V and T=300K and T=400K.

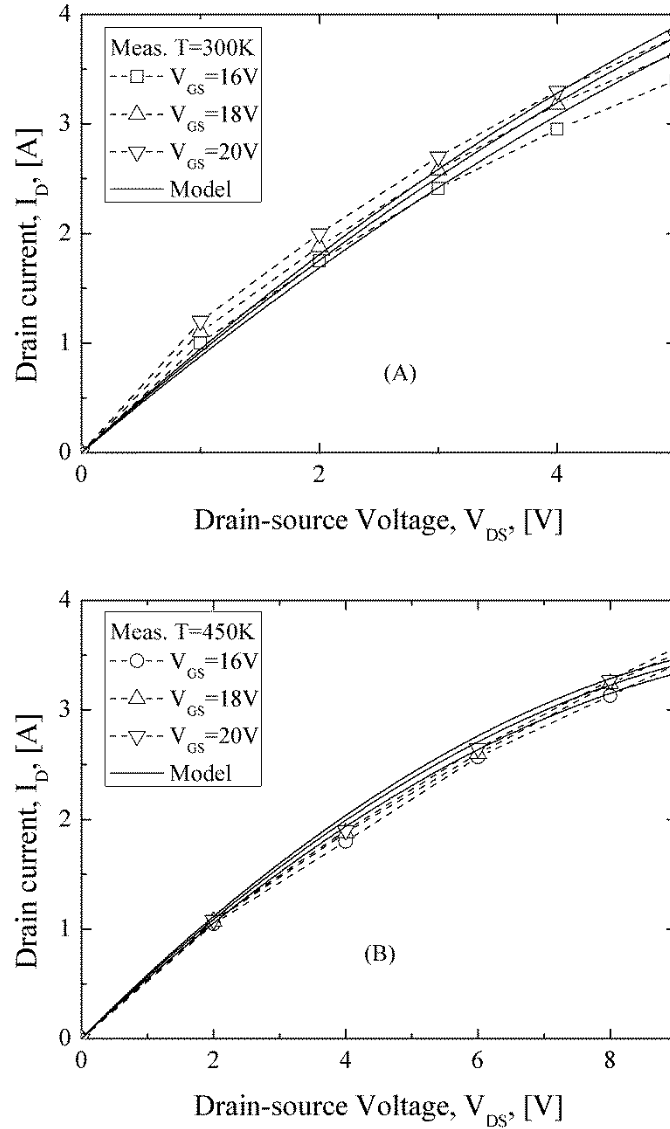

Fig. 13: Comparison of the model with the experimental output characteristics of the commercial device [24], at T=300K and T=400K.

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For the lack of information about the geometries and doping levels of the commercial device, with respect to the simulated device, some parameters have been adjusted to match those from the datasheet, while others have been assumed similar to those published in the related literature [21]: in order to meet the transconductance and threshold voltage, the oxide thickness has been reduced to 30*nm*; the doping of the drift layer has been left equal to those of the previously simulated structure ($N_{DRIFT} = 3 \times 10^{15} cm^{-3}$), while its depth has been enlarged to 17μm in order to match $BV = 1.7kV$. The

geometrical parameters have been left unchanged, except for $W = 20cm$ and $L_{FET0} = 3\mu m$. The substantial agreement between model and experimental curves of both the output and the trans-conductance characteristics, in the safe operating temperature range of the device, $\Delta T = 150K$, confirm the correctness of the model in describing the forward device behavior. As a final note it's worth observing that, although in the datasheet the V_{DS} value of the transfer characteristics is not reported, in Fig. 12 the model seems to fit well with $V_{DS} = 12V$, both in the saturation and in the ohmic region of operations at the two temperatures reported in the figure. The discrepancies at lower voltages can be justified by recalling that the sub-threshold current has been neglected in (4).

IV. CONCLUSION

In this paper an analytical model of the 4H-SiC vertical DMOSFET is presented which is able to express with closed form equations the forward DC current-voltage characteristics of the device, including the parasitic resistance and the effects of the insulator-semiconductor interface traps on the threshold voltage in a wide range of voltages and temperatures. Simple formula are, also, derived for the analysis of the intrinsic stability of 4H-SiC DMOSFETs, when the device is forward biased, which can reveal a useful instrument to both analyze and design the 4H-SiC DMOSFETs and to a more accurate definition of the Safe Operating Area of the device.

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