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Nanostructured materials for a new generation of electronic devices

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Introduction

In the last century we have witnessed an unstoppable technological advance. Since the invention of the first transistor, which resulted in that of the first microprocessor, it has been clear that reducing the size of the devices is essential to obtain greater computing power and, therefore, better performance. In 1965 Gordon Moore, cofounder of Intel, surmised that the number of transistors in microprocessors would double every 12 months. In 1975 this prediction turned out to be correct and before the end of the decade the times were extended to two years, a period that will remain valid throughout the 1980s. The law, which will be extended throughout the nineties and will remain valid until today, was reformulated at the end of the eighties and elaborated in its final form, that is, that the number of transistors in the processors doubles every 18 months. The limitations of Moore's law began to emerge around 2000, when it became clear that further reduction in the size of transistors would have led to the generation of unwanted quantum parasitic effects in electronic circuits. This drawback has meant that in the last 20 years the performance of microprocessors has not significantly improved except for the implementation of new architectural structures, like multicore technology.

In this framework, the exfoliation of graphene, a single layer of carbon atoms, in 2004 marked an epochal turning point. Its intrinsic two-dimensional (2D) nature, indeed, allows to continue the process of miniaturization of electronic components, without incurring in the so-called short-channel effects that limit the electrical performance of the devices at the nanoscale. Moreover, graphene extremely interesting peculiarities, such as high mobility and current carrying capability, chemical stability, and mechanical robustness, make it a material of great interest also for fundamental research. The main drawback, which has so far prevented graphene from replacing silicon in modern technology, is the absence of a bandgap which makes it unsuitable as material for

the realization of transistors' channel.

However, the discovery of graphene was just a starting point and, from that moment, the research on 2D materials and their possible use in electronics has received a great boost. Indeed, new classes of 2D materials have emerged day after day and have been the subject of countless studies. Among these, transition metal dichalcogenides (TMDs) have certainly played a fundamental role. Its members have proven unique properties of sizeable and non-zero bandgaps, high ON-OFF ratios, quasi-ideal subthreshold swings, mechanical flexibility, thermal and chemical stability that could enable the needed extreme channel length scaling and open the way to the improvement of existing electronic, optoelectronic and sensing applications and inventing new ones.

Despite the worldwide effort, researchers are still confronting with common challenges in material fabrication and device performance and many studies are still needed to discover the fascinating properties of these materials and to be able to exploit them for the fabrication of real devices.

This PhD project fits into this scenario and its principal aim is to investigate the electrical transport properties of different 2D materials and to test their performance when used as channel of field-effect transistors. The electrical response under various external stimuli, such as light and gas exposure and temperature and pressure variation was investigated trying to shed some light on the intrinsic transport properties of these 2D materials. The research was also extended to other types of nanostructured materials, such as nanopillars and nanotubes. Their basic electrical properties were investigated, and the high aspect ratio of these nanostructures was exploited to realize field-emitting devices.

This thesis work is divided in 3 chapters, and it is organized as follows:

Chapter 1 starts with a brief summary of the state of the art of modern CMOS technology. Then, it introduces the discovery of graphene and describes its possible technological applications and its

limits. The last paragraph focusses on the properties of new 2D materials beyond graphene and on their possible exploitation in electronic devices. Chapters 2 and 3 are a collection of selected papers published during the 3 years of PhD that better highlight the main results achieved in this PhD project on 2D materials for electronic applications. Specifically, Chapter 2 reports the results obtained from the study of three different 2D materials (tungsten diselenide, black phosphorus and germanium arsenide) used as field-effect transistors channel. The electrical transport properties of these materials were investigated as function of temperature and pressure revealing peculiar and unknown physical properties. The response to light was also analysed revealing the presence of unusual phenomena, such as of the negative photoconductivity. In the last part of Chapter 2, the importance of metallic contacts on the properties of 2D materials is highlighted and a model is proposed to describe and evaluate the main parameters in double Schottky barrier devices. Finally, Chapter 3 describes the field emission properties of nanostructured materials, such as nanotubes and nanopillars. The response to external stimuli, such as electrical and mechanical stress, has been investigated and new intrinsic properties of these nanostructured devices have been reported.

Chapter 1: MOSFET TECHNOLOGY: STATE OF THE ART AND FUTURE PERSPECTIVES

1.1 Field-effect transistor: working principles

The transistor is one of the basic building blocks of modern electronics. It is based on semiconductor materials, and it is mainly used to amplify or switch electronic signals and electrical power. The first idea of a transistor was proposed by Julius Edgar Lilienfeld in 1926, but the actual realization of a working device was not possible with the technology of the time. Later, in 1947, American physicists John Bardeen and Walter Brattain realized the first working point-contact transistor while working under William Shockley at Bell Labs. Finally, in 1959, Mohamed Atalla and Dawon Kahng working in the same laboratory, invented the metal–oxide–semiconductor field-effect transistor (MOSFET). The MOSFET, also known as MOS transistor, revolutionized the field of electronics and, nowadays, is by far the most widely used transistor. Its applications range from computers and electronics to communications technology and, most importantly, it paved the way for the birth of the digital age, becoming a fundamental building block of modern digital electronics.

The field-effect transistor (FET) is an active device composed of three terminals referred as source, drain and gate. The current flows in a semiconductor region, called the channel, between the drain and the source, and it is modulated by the gate electrode, under the application of an electric field (i.e. gate voltage potential) orthogonal to the channel direction. An insulating layer is set between the conductive channel and the gate electrode to prevent current losses through the gate (gate leakage phenomenon). There are four basic MOSFET device types. The typical structure of n-channel enhancement mode MOSFET is reported in Figure (1.1 a). It is formed by a p-type silicon slice, heavily n-type doped under the source and drain contacts. The term enhancement refers to the idea that

the semiconductor substrate is not inverted directly under the oxide when zero gate voltage is applied. The principle of operation of the FET is based on the reversal of the channel region doping, from the p-type of the silicon substrate to the n-type of the counter doped areas under the contacts.

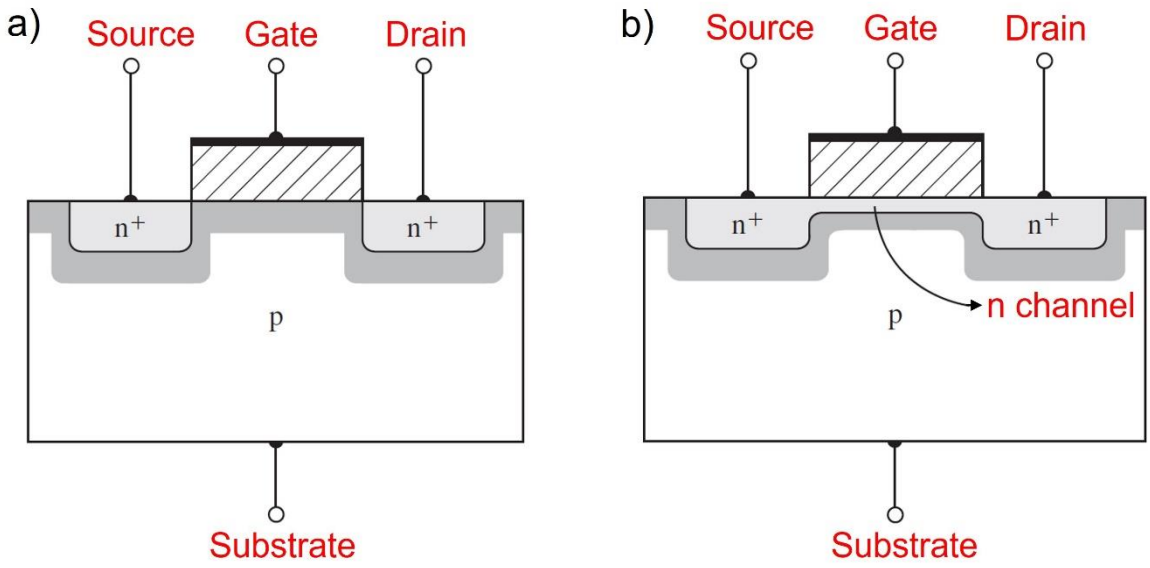


Figure 1.1 – Cross section of an n channel enhancement a) and depletion b) mode MOSFET

The physics of the MOSFET structure can be explained thinking at this structure as a parallel-plane capacitor. When a negative voltage is applied to the gate the Si-substrate behaves as a capacitance and the free holes, attracted by the gate, accumulate at the semiconductor-insulator interface. In this case the source and drain are isolated from each other, and no current can flow; the transistor is said to be in the OFF state. Conversely, when a positive potential is applied to the gate electrode the major charge carriers of the p-type silicon substrate are swept away, leaving electrons at the oxide interface. If the potential is high enough, $V_{gs} = V_{th}$ (threshold voltage), the region under the gate has attracted so many negative charges to achieve a doping reversal from p- to n-type. The

accumulated electrons originate a channel that defines a link between the source and drain electrodes, doped of the same kind, so that the application of a voltage bias (V_{ds}) gives rise to a current flow. In this situation, called threshold inversion point, the transistor is considered turned ON. The source terminal is the source of carriers that flow through the channel to the drain terminal. Hence, for this device, electrons flow from the source to the drain so the conventional current will enter the source and leave the drain. The MOS channel is covered by an insulator layer, typically silicon dioxide (SiO_2), contacted by the gate electrode. Figure (1.1 b) shows an n-channel depletion mode MOSFET. In this case, an n-channel exists under the oxide also when a $V_{gs} = 0$ potential is applied to the gate. This is due to the fact that the threshold voltage of a MOS device with a p-type substrate may be negative; for this reason, an electron inversion layer can already exist with zero gate voltage applied. Such a device is considered to be a depletion mode device. The n-channel can be an electron inversion layer or an intentionally doped n region. Analogous considerations can be made about p-channel enhancement mode MOSFET and p-channel depletion mode MOSFET. In the p-channel enhancement mode device, a negative gate voltage is needed to attract holes in the channel region and create an inversion layer to connect the p-type source and drain regions. The carriers, i.e. holes, flow from the source to the drain, so the conventional current will enter the drain and leave the source. In the depletion mode device, instead, a p-channel region already exists when no gate voltage is applied.

1.2 Current-voltage characteristic

The first configuration we consider is an n-channel enhancement mode MOSFET to which it is applied a gate voltage V_{gs} that is less than the threshold voltage V_{th} and with only a very small drain-to-source V_{ds} voltage. The source and substrate, also called body, terminals are held at ground potential. In this configuration, it is not possible to form the inversion layer and the drain and the

substrate act like a reverse biased p-n junction. The drain current is zero, if we do not consider p-n junction leakage currents. Now, if a positive gate potential such that $V_{gs} > V_{th}$ is applied to the gate electrode, an electron inversion layer is formed so that when a small drain voltage is applied, the electrons in the inversion layer will flow from the source to the positive drain terminal. In the ideal case, we do not consider current leakage through the oxide to the gate terminal and, for small V_{ds} values, the channel region behaves as a resistor, so we can write

$$I_{ds} = g_d V_{ds} \tag{1. 1}$$

where g_d is the channel conductance and it is given by:

$$g_d = \frac{W}{L}\mu_n |Q_n| \tag{1. 2}$$

where μ_n is the mobility, that for now we consider a constant, of the electrons in the inversion layer, W and L are the channel width and length and $|Q_n|$ is the magnitude of the inversion layer charge per unit area. Since, the inversion layer charge is a function of the applied gate voltage we can assert that the basic MOSFET operation is the modulation of the channel conductance by the gate voltage. Such variation of the channel conductance, in turn, determines the drain current. Figure (1.2 a) shows the I_{ds} versus V_{ds} characteristics, for small values of V_{ds}. For $V_{gs} < V_{th}$, the drain current is zero. As V_{gs}becomes larger than V_{th}, enough electrons are attracted to the channel region and current begins to flow between the source and drain. The relationship between current and voltage is linear and the slope of the curve, corresponding to the conductance of the channel, depends on the value of the potential applied on the gate. In this situation, the relative charge density is qualitatively given by the thickness of the inversion channel layer and is constant along the entire channel length.

Increasing the potential applied to the drain electrode, the voltage drop across the oxide near the drain terminal decreases, resulting in the reduction of the induced inversion charge density near the drain. In this situation, the incremental conductance of the channel at the drain as well as the slope of the I_{ds} versus V_{ds} curve decrease. When V_{ds} increases to the point where the potential drop across the oxide at the drain terminal is equal to V_{th}, the induced inversion charge density is zero at the drain terminal. At this point, the incremental conductance at the drain is zero, which means that the slope of the I_{ds} versus V_{ds} curve is zero. It is possible to write:

$$V_{ds}(sat) = V_{gs} - V_{th} \tag{1. 3}$$

where $V_{ds}(sat)$ is the drain-to-source voltage producing zero inversion charge density at the drain terminal.

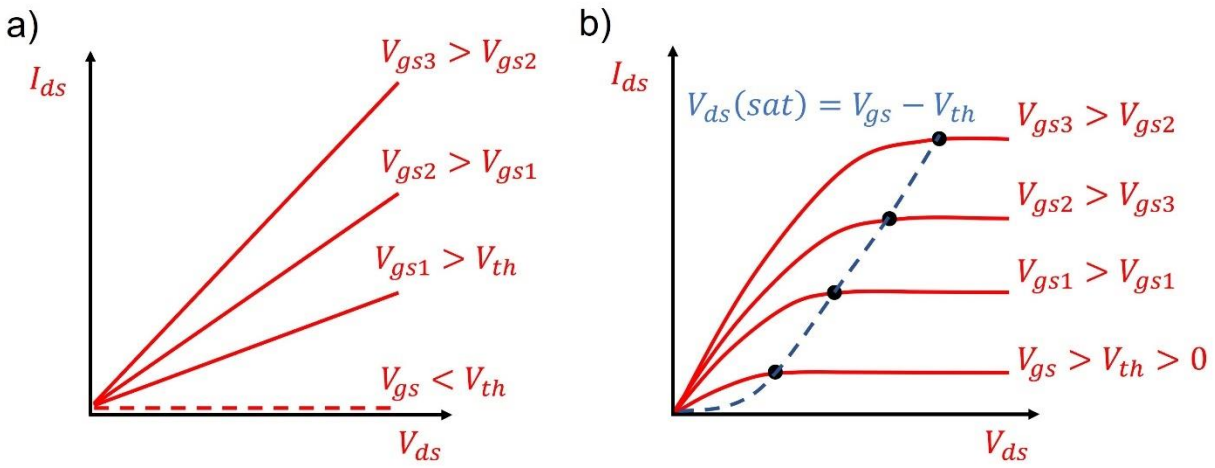


Figure 1.2 – a) I_{ds} versus V_{ds} characteristics for small values of V_{ds} at different V_{gs} voltages. b) Family of I_{ds} versus V_{ds} curves for an n-channel enhancement mode MOSFET.

If V_{ds} becomes larger than the $V_{ds}(sat)$ value, the point of the channel where the inversion charge is zero moves toward the source terminal. Electrons are injected in the channel from the source, then they travel toward the drain, and finally, at the point where the charge goes to zero, they are swept to the drain contact by the electric field. Assuming that, after this process, the new channel length is small compared to the original length, then the drain current will stay constant for $V_{ds} > V_{ds}(sat)$. The corresponding region of the I_{ds} versus V_{ds} characteristic is referred to as the saturation region. The application of a different gate potential does not only affect the initial slope of I_{ds} versus V_{ds} curves, but also changes the value of $V_{ds}(sat)$. Figure (1.2 b) shows the family of I_{ds} versus V_{ds} curves for an n-channel enhancement mode MOSFET for different values of V_{gs}.

Similar results can be obtained for the n-channel depletion mode MOSFET. Indeed, if the n-channel region is an induced electron inversion layer originated by the work function difference between the metal and the semiconductor and by fixed charge in the oxide, the current–voltage characteristic is the same as we have discussed, except that V_{th} is a negative quantity. We can also consider the case when the n-channel region is an n-type semiconductor region. In this type of device, a negative gate voltage will induce a space charge region under the oxide, reducing the thickness of the n-channel region. The reduced thickness decreases the channel conductance, which reduces the drain current. A positive gate voltage will create an electron accumulation layer, which increases the drain current. One basic requirement for this device is that the channel thickness t_c need to be less than the maximum induced space charge width in order to be able to turn the device off.

The analytic expression of the transistor current–voltage relation can be mathematically derived leading to:

$$I_{ds} = \frac{W\mu C_{ox}}{2L}\left[2\left(V_{gs} - V_{th}\right)V_{ds} - V_{ds}^2\right] \quad (1.4)$$

which can be written as:

$$I_{ds} = K\left[2\left(V_{gs} - V_{th}\right) - V_{ds}^2\right] \quad (1.5)$$

Where $K = \frac{W\mu C_{ox}}{2L}$ is a parameter called the conduction parameter for the n-channel MOSFET and has units of A/V^2. For fixed bias, Equation (1.4) describes the transfer characteristic of a transistor and for small V_{ds} it becomes:

$$I_{ds} = \frac{W\mu C_{ox}}{2L}\left(V_{gs} - V_{th}\right)V_{ds} \quad (1.6)$$

Finally, when the transistor is biased in the saturation region, the ideal current–voltage relation is given by:

$$I_{ds} = \frac{W\mu C_{ox}}{2L}\left(V_{gs} - V_{th}\right)^2 \quad (1.7)$$

The operation of a p-channel device is the same as that of the n-channel device, except the charge carrier is the hole and the conventional current direction and voltage polarities are reversed.

Equation (1.6) can be used to determine two important parameters for a transistor, i.e. the carrier mobility and the threshold voltage.

A linear fit of the linear part of the transfer characteristic ($I_{ds}\ vs\ V_{gs}$ curve) shown in Figure (1.3 a) can be used to simulate equation (1.6). From the slope of the fitting curve the carrier mobility can be written as:

$$\mu = slope \frac{L}{W C_{ox} V_{ds}} \qquad (1.8)$$

while the x-axis intercept provides the threshold voltage V_{th}.

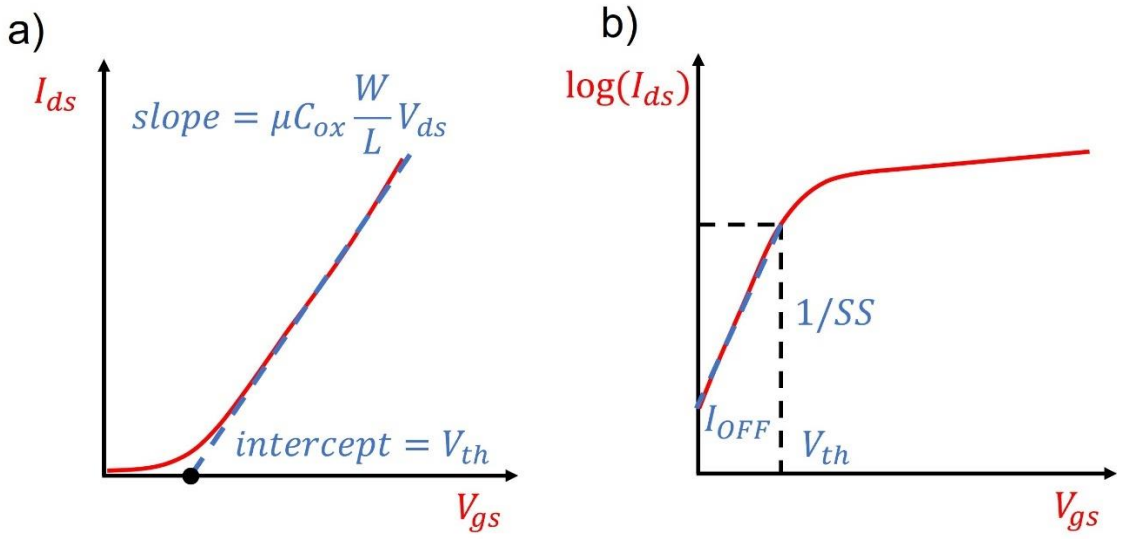


Figure 1.3 – Transfer characteristic ($I_{ds} - V_{gs}$ curve) and its main parametrs on linear a) and semilogarithmic b) scale.

For low and high values of the applied gate potential, the transfer characteristic deviates from the linear trend because of subthreshold conduction and mobility dependence on V_{gs}.

When the MOSFET is in the OFF state a small-negligible but non-zero current flows between the source and the drain. Electric circuits are designed in order to minimize the OFF-state current to reduce power dissipation when the device is in standby.

The MOSFET OFF-state current is called subthreshold current and as it has an exponential behaviour described by:

$$I_{ds,sub} = \frac{W}{L} \exp\left[\frac{q(V_{gs} - V_{th})}{\eta kT}\right] \quad (1.9)$$

Where q is the electron charge, η is a dimensionless parameter and T is the temperature. Form equation (1.9), it results that, fixed the geometrical dimension of the transistors, it is possible to reduce the off current by increasing the threshold voltage, cooling down the working temperature and decreasing the η factor. The first two options are not desirable because a high threshold voltage reduces the ON-state current and degrades the device operation while low cryogenic working temperature requires considerable costs. The reduction of the η factor is the most efficient way to optimize the working parameters and can be achieved varying the gate oxide thickness. Indeed, from capacitance considerations, it results:

$$\eta = 1 + \frac{C_{dep}}{C_{ox}} \quad (1.10)$$

A reduction of the oxide capacitance, related to the oxide thickness, allows to increase the η factor reducing the OFF-current.

Finally, the η factor is also connected to another important transistor parameter called subthreshold swing (SS) which indicates how rapidly in the subthreshold regime the transistor current is switched off:

$$SS = \eta\ 60\ mV \frac{T}{300K} \quad (1.11)$$

This parameter can be obtained performing a linear fit of the transfer characteristic on semilogarithmic scale, as shown in Figure (1.3 b). The ideal SS value, at room temperature, is $60 \frac{mV}{decade}$.

1.3 Short-channel effects

The continuous demand for more performing devices has led to a continuous reduction in the size of electronic components. As early as 1965, Gordon Moore had formulated his famous law according to which the number of transistors in a dense integrated circuit (IC) should double about every two years. This empirical prediction was respected almost strictly until 2010, when semiconductor advancement has slowed industry-wide, below the pace predicted by Moore's law. The main purpose for reducing the size of the electric components, in particular transistors, is increasing speed and reducing cost. Indeed, smaller circuits lead to a reduction of the capacitance, thereby increasing operating speed. At the same time, smaller components allow to contain more of them in the same wafer, dividing the total cost of a single wafer among more dies.

So, the reduction of transistor channel length, during the last decades, to increase the operational velocity and to accommodate a greater number of components per chip, has become the main issue for ICs developers. However, the extreme reduction of the MOSFET dimensions can lead to a series of undesirable phenomena, the so called short-channel effects, which arise from the scaling procedure. When the channel of the MOSFET becomes the same order of magnitude as the depletion layer width of source and drain, the transistors start behaving differently, impacting performance, modelling and reliability.

The channel length is defined short if it results comparable to the sum of the drain and source depletion regions, i.e. $L \sim W_s + W_d$.

The principals non-idealty effects that arise from the instauration of a short-channel regime are:

- Enhancement of the subthreshold current and drain induced barrier lowering (DIBL) effect

- Threshold voltage roll-off

- Surface scattering

- Velocity saturation

- Impact ionization

- Hot electron injection

As shown in equation (1.9), for gate voltages lower than V_{th}, a transistor is OFF, but a non-zero current flows across the device. Such subthreshold current is a function of the channel length. Particularly, reducing L leads to an increase of the $I_{ds,sub}$ which is an unwanted effect, since higher subthreshold currents mean more power consume when the IC is in standby. As explained before, one method to overcome this issue is increasing the oxide capacitance, thinning the oxide thickness, or using high-k dielectrics.

Another issue, related to the short-channel length, that affect the subthreshold current is the punch-through. When the channel is shrunk, the drain and source depletion regions are extended in proximity of each other, forming a unique region where the punch-through phenomenon occurs. Basically, the punch-through is the flow of drain to source current thought the new depletion region, that causing an increase of the device current with the V_{ds} could lead to the breakdown of the device. A way to reduce this effect is to increase the bulk doping level, resulting in smaller drain/source junctions and in the reduction of parasitic currents. However, high bulk doping increases the subthreshold swing which results in higher subthreshold currents. Another way to reduce the punch-through effect is the construction of shallow-high doped source-drain regions. The side effect of this method is that it contributes to a degradation of the channel mobility due to additional scattering centres.

An effect similar to punch-through is the DIBL. This effect can be understood considering the

potential barrier profile that an electron has to overcome to go from source to drain. When no bias is applied to source and gate electrodes ($V_{ds} = 0$ and $V_{gs} = 0$), there is a potential barrier that prevents electrons from flowing from source to drain. The application of a gate voltage lowers this barrier down until electrons have enough energy to flow. In the ideal case, V_{gs}would be the only potential that would affect the barrier. However, as the channel becomes shorter, a larger V_{ds} widens the drain depletion region to a point that reduces the potential barrier. For this reason, this effect is called drain induced barrier lowering. When the barrier is decreased, electrons move more freely into the channel region, requiring less gate voltage to deplete the substrate. So, the main effect of the DIBL is that even for $V_{gs} < V_{th}$ current can flow, contributing to the subthreshold current. Since a lower gate voltage is needed to invert the channel, the threshold voltage expression modifies and can be written as:

$$V_{th} = V_{th,long-channel} - (V_{ds} + V_{bi}) \exp\left(-\frac{L}{l_d}\right) \qquad (1.12)$$

that testify a reduction of V_{th} also known as threshold voltage roll-off.

$V_{th,long-channel}$ is the threshold voltage for the long channel device and L and l_d are the channel length and DIBL characteristic length, a parameter which is related to device characteristics:

$$l_d \approx \sqrt[3]{t_{ox} W_{dep} X_j} \qquad (1.13)$$

where t_{ox} and W_{dep} are the oxide thickness and depletion region width, while X_j is the junction depth. From equation (1.13) it derives that a first approach to reduce the DIBL effect can be to decrease the thickness of the gate oxide, thus improving the gate control of the channel. By the way, this method even if desirable for a better channel control and reduction of DIBL effect, can generate additional problems. Indeed, when the oxide is very thin, the charge carrier can tunnel

through the gate insulator increasing the leakage current and potentially damaging the entire device. Moreover, the formation of fixed charge inside the oxide, give rise to the shift of the threshold voltage. A way to avoid the inconveniences deriving from extreme reduction of oxide thickness is to replace typical gate oxides, like SiO_2, with high-k dielectrics (such as ZrO_2 and HfO_2), that have a higher gate control at greater thicknesses. This solution has been tested in the last years, but it has led to some further drawbacks mostly related to the occurrence of chemical reaction between the high-k dielectric and the Si substrate. Other possible approaches to avoid the DIBL effect can be reducing the junction depth (through the fabrication of shallow drain-source junctions) or thinning the vertical dimension of the channel.

The next non-ideality effect due to the short length of the channel is the surface scattering. This effect is due to the fact that while the carriers travel along the channel, they are attracted to the surface by the electric field created by the gate voltage. As a result, they keep scatter against the surface, following a zig-zag path. Surface scattering reduces the surface mobility of the carriers, in comparison with their bulk mobility impacting the current-voltage relationship of the transistor. Obviously, this effect is also present in traditional transistors, but reducing the size of the channel amplifies it considerably. Indeed, as the length of the channel becomes shorter, the lateral electric field created by V_{ds} becomes stronger. To compensate that, the vertical electric field originated by the gate voltage needs to increase proportionally, which can be achieved by reducing the oxide thickness. As a side effect, surface scattering becomes predominant, reducing the effective mobility of the carriers. Moreover, surface scattering can lead to velocity saturation of the carriers, modifying the current-voltage characteristic of the transistor that become approximately linear with V_{gs}. The velocity of charge carriers is usually proportional to the applied electric field, but this assumption is true only for small fields. Indeed, as the field gets stronger such as in the case of short-channel

transistors, the carrier's velocity tends to saturate, meaning that above a certain critical electric field, they tend to stabilize their speed and eventually cannot flow faster.

The common model used to describe the mobility dependence on the electric field dependence is the following

$$\mu = \frac{\mu_{eff}}{\left[1 + \left(\frac{\mu_{eff} E}{v_{sat}}\right)^2\right]^{1/2}} \qquad (1.14)$$

where μ_{eff} is the mobility not affected by the high electric field and v_{sat} is the saturation velocity. The velocity saturates when $E \gg E_c$ (critical field) and in silicon it results $\sim 10^7\ cm/s$ for electrons and $\sim 0.6 \cdot 10^7\ cm/s$ for holes.

Impact ionization is another non-ideality effect that could arise from the presence of intense electric field. Indeed, the strong lateral field typical of short-channel transistors endows the charge carriers with high velocity, and therefore, high energy. Such carriers can randomly collide with silicon atoms of the substrate leading an electron out of the valence band to the conduction band. This process originates electron-hole pairs and while the electrons are swept to the drain, enhancing the ideal transistor current, holes are attracted to the ground, contributing to a parasitic current. When electron-hole pairs generate at high rate, the holes flowing through the bulk, can cause a voltage drop at the parasitic resistance of the bulk itself. In this situation, the parasitic bipolar transistor that is formed by the junctions between source-bulk-drain, that is normally turned off because the bulk is biased at the lowest voltage of the circuit, can activate. Electrons can flow to the bulk and drain by the BJT instead of the channel created by the MOSFET creating anomalies in the current-voltage characteristic. Either most catastrophic effects can happen when the newly generated electrons become themselves hot carriers and knock out other atoms of the lattice. An avalanche effect can

lead to an overrun current that the gate voltage cannot control.

Finally, these hot carriers can follow a different path contributing to the so-called hot carrier injection. Indeed, the energy they contain may be sufficient to enter the oxide and get trapped in it. There, they accumulate and form new charged traps, which degrade the performance of the transistor increasing the threshold voltage and affecting the gate control on the channel. Over time, the accumulation of electrons in the oxide causes the so-called ageing of transistors. To reduce the formation of "hot" carriers and their negative effects, the electric field can be artificially weakened through the implantation of lightly doped drains, beside the heavily doped drains. The electric field only needs to be weakened at the drain, but since the drain terminal is only defined by the operating point, the implant needs to be added at both terminals of the MOSFET. The implantation allows to have wider depletion regions that leads to larger distance between different potentials, reducing the electric field. On the other hand, this method drastically increases the parasitic resistances through source and drain. Another option to try to avoid these short-channel effects is to shrink all the device dimensions, including the channel width/thick and the oxide/insulator thickness.

1.4 Graphene FETs

The short-channel effects discussed in the previous paragraph represent the main obstacle to the continuation of the astounding technological development that characterized the entire 20th century. Complementary metal oxide semiconductor (CMOS) technology, principally using silicon based MOSFETs, pushed the miniaturization of electronic components to its limit. As for 2019, the number of transistors on commercially available microprocessors could reach up to 39.54 billion, and Samsung and TSMC have been fabricated 10 nm and 7 nm MOSFETs. The International Technology Roadmap for Semiconductors predicts that after the year 2021, downscaling transistors

will no longer be economically viable and semiconductor industries are already considering alternative materials and technologies for extending Moore's law in a post-silicon world. In this framework, the discovery of graphene marked the beginning of an era based on the possibility of exploiting the incredible properties of two-dimensional (2D) materials to overcome the short-channel effects and continue to extend the possibility of miniaturizing transistors to improve their performance. Indeed, the intrinsic 2D nature, i.e. thickness negligible respect to the in-plane dimensions, is beneficial for suppressing short-channel effects and length scaling, since it satisfies the condition

$$L > a \cdot l_d \qquad (1.15)$$

where a is a constant. Moreover, the benefits of 2D materials are related to the extraordinary and innovative properties, like the possibility to tune the bandgap through the number of layers and the intrinsic p- or n-type doping, which does not require additional dopants, cause of mobility degradation.

Graphene is a single atom-thick planar allotrope of carbon. It is closely related to graphite, which is another allotrope of carbon.[1] The structure of three-dimensional graphite can be thought as a layered stack of graphene sheets held together by van der Waals forces and it was determined and studied in 1916 using powder diffraction.[2] The difference in the structure of 2D graphene and three-dimensional graphite is shown in Figure (1.4 a). In 1947, Wallace was the first to study the electronic structure of graphene, in order to better understand the electronic properties of three-dimensional graphite.[3]After that, Mermin-Wagner theorem and the Landau-Peierls arguments concerning thermal fluctuations at nonzero temperatures that would lead to thermodynamically unstable two dimensional crystals[4] have significantly slowed down experimental research on

graphene. The turning point came in 2004 when Geim and Novoselov demonstrated the first experimental evidence of the existence of graphene by exfoliating crystalline graphite using scotch tape and transferring the graphene layers onto a thin silicon dioxide over silicon,[5] a technique now referred to as mechanical exfoliation. Since then, intense efforts by the scientific community have been made to obtain a complete understanding of the graphene structural and electrical properties.

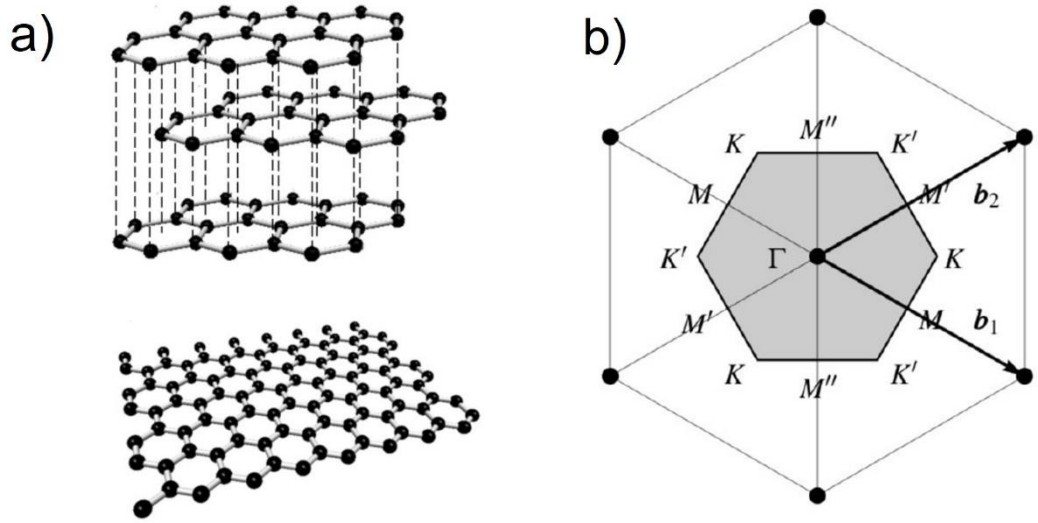


Figure 1.4 – a) Crystal structure of graphite (top) and graphene (bottom). Graphite is made of several layers of graphene sheet stacked on top of each other and held together via weak van der Waals forces. b) The reciprocal lattice of graphene (in k space). The shaded region is the first Brillouin zone. By convention, Γ denotes the point k = 0.

Graphene has a honeycomb lattice of sp^2 bonded carbon atoms separated by an interatomic distance $a \approx 1.42\,\dot{A}$. The $2s$, $2p_x$, and $2p_y$ states mix to form three sp^2 hybrid orbitals for each carbon atom separated by 120°. These sp^2 hybrid states originate three strong covalent σ bonds between each carbon atoms and neighbouring carbon atoms, leading to the geometry of the lattice. Electrons in $2p_z$ orbitals are located above and below the plane of graphene, participating in weaker

π bonds. The electrons participating in the σ bonds lead to the high strength and other novel mechanical properties of graphene but play no role in its electronic properties. On the other hand, π electrons, being highly mobile give a fundamental contribution to graphene electronic response. The crystal lattice of graphene is formed by two triangular lattice (A and B) shifted respect to each other, defining the hexagonal honeycomb array. Different atoms in the lattice are not equivalent, making the honeycomb lattice a non-Bravais lattice. Figure (1.4 b) shows the first Brillouin zone for graphene in reciprocal space. The center of the first Brillouin zone is usually labelled as Γ and corresponds to the origin $k = 0$, where $k = (k_x; k_y)$ is the wave vector associated with electronic states in the lattice, with k_x and k_y representing the wavenumbers along $\hat{e}_1$ and $\hat{e}_2$, respectively. The first Brillouin zone is hexagonal and has six points labelled as K and K', collectively referred to as Dirac points. These Dirac points are the main responsible for the exceptional electronic properties of graphene. Indeed, the plot of the graphene band structure reported in Figure (1.5) reveals that the valence and conduction bands of graphene coincide at six points (exactly the Dirac points of the reciprocal lattice), showing a zero bandgap and thus displaying the semimetallic nature of graphene. A tight binding approach reveals a linear-like behaviour of the energy-momentum relation, testifying the fact that the charge carriers behave like relativistic particles with high Fermi velocity $v_F \sim 10^6\ m/s$.

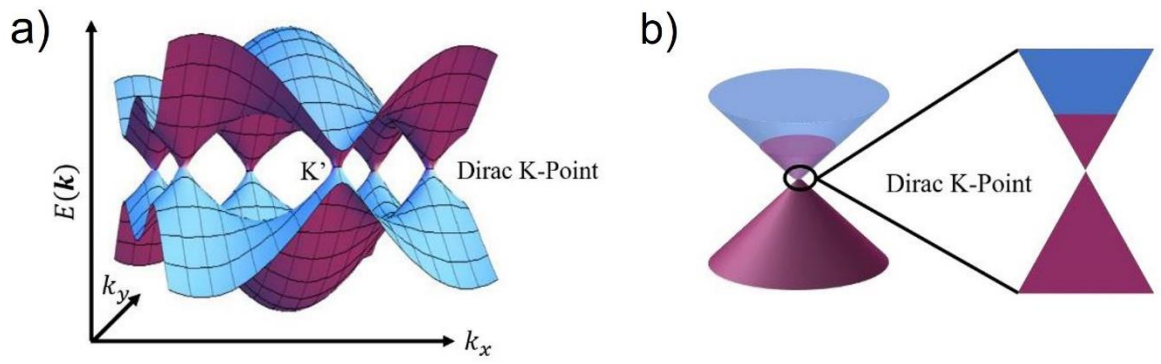


Figure 1.5 – a) 3D plot of graphene band structure. b) Magnification of the band structure at the K-point

As regards the possible technological applications of graphene, one of its most interesting properties is certainly the possibility of changing the position of the Fermi level, and therefore the doping, simply through the application of a gate potential. Moreover, as already mentioned, the intrinsic 2D nature of graphene allows to realize devices, in particular FETs, with a thickness of only 3 Å (graphene single layer), which allow to avoid the short-channel effects discussed in the previous paragraph. The constrain of the electrons and holes moving in the plane gives rise to extraordinary transport properties. However, despite these interesting premises, the realization of the first devices based on graphene showed that it is also responsible of numerous drawbacks.

To start, in real devices it is practically impossible to obtain the perfect crystalline structure predicted theoretically. Indeed, intrinsic lattice defects, impurities, the graphene-substrate interaction, and thermal phonon affections can modify both the morphology and the ideal graphene band structure, altering device properties. Phonons are a typical example of an intrinsic scattering source, which strongly limit the mobility at finite temperature. Extrinsic impurities and/or carbon vacancies can give rise to the same effect through Coulomb scattering because they act as charged scatter centers, modifying the lattice period potential. To avoid these effects, several techniques

have been implemented to tune the graphene conductivity and boost the performance of graphene transistors. The fabrication technique, indeed, is another main key-point for the good quality/high-mobility graphene.

Another undesirable effect is the reduction of mobility mainly due to grain boundaries,[6] doping defects,[7] gate control[8] and graphene sheet resistance,[9] i.e. the resistivity at zero gate voltage. Moreover, a no less important contribution to the limitation of mobility is given by the interaction of graphene with the substrate. The use of BN (boron nitride) as substrate, defined by a smooth surface and lattice constant equivalent to the graphene one, instead of the typical SiO_2, resulted in a mobility about three times higher. Unfortunately, graphene on BN devices are difficult to realize and thus not ideal for large-scale fabrication and applications. Another proposed solution is based on the realization of suspended graphene devices.[10] Such FETs have shown impressive transport properties, with field effect mobility up to $2 \cdot 10^5\ cm^2V^{-1}s^{-1}$, but also the suspended device fabrication imposes many practical problems.

Another major problem is related to the suppression of device on-current caused by the graphene/contact resistance.[11] Indeed, ohmic and low resistance contacts are important figures of merit for high frequency devices and the realization of stable and low-resistance contacts is still under intensive study.[12] The variation of the contact resistance is attributed to many different causes, related to graphene growth and number of layers, metal type and deposition process, quality of the metal graphene/interface, measurement conditions, etc. It has been found that the contact resistance can vary greatly depending on the used metal, ranging from few hundreds to thousands $\Omega \cdot \mu m$. Several studies have focused on the optimization of metal/graphene interfaces showing that the best contact resistances can be achieved with Ni and Cu contacts yielding contact resistance as low as $\sim 300\ \Omega$.[13,14] Besides the choice of metal, another recently developed

technique to reduce the contract resistance is to modify the contact area in order to increase charge injection through the graphene edges and the graphene etching under the contacts to favour the formation of dangling carbon-to-metal bonds. Recent studies have reported contact resistances down to $100\ \Omega\ \cdot \mu m$ using this method.[15] A low contact resistance enables the study of intrinsic graphene properties and increases the performance of graphene devices.

The previous problems are almost exclusively related to the manufacture of the devices. Once the fabrication techniques have been optimized, it is, at least in theory, possible to realize FETs with graphene channel. Due to its peculiar band structure, with zero bandgap at the Dirac points, graphene FETs originate ambipolar V-shaped transfer characteristics, reported in Figure (1.6), dominated by a p-type and n-type conduction at negative and positive gate voltage, respectively,[16] with carrier mobilities estimated up to $200.000\ cm^2V^{-1}\ s^{-1}$. If on one hand, the ambipolar conduction can be exploited as feature for complementary logic applications, on the other hand, the limited ON-OFF ratio caused by the absence of intrinsic bandgap is a significant obstacle and requires deep material engineering for real applications.[17]

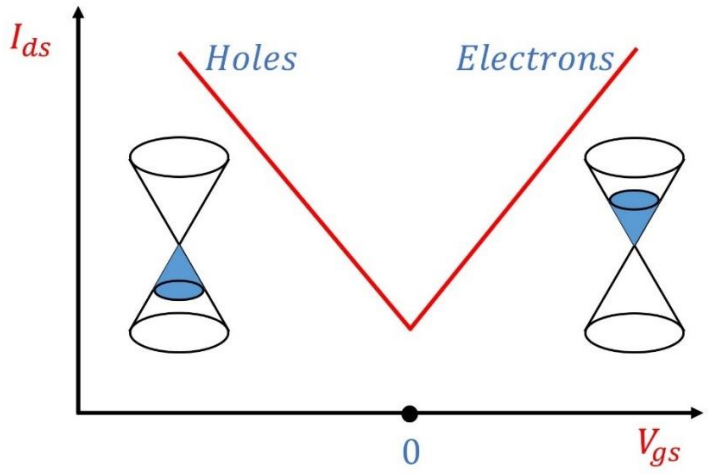


Figure 1.6 – Ideal graphene FETs transfer characteristic. Negative (positive) V_{gs} induces holes (electrons) transport.

Until now, such absence of bandgap is resulted an almost insurmountable problem. Indeed, the ON-OFF ratio (i.e. the ratio between the transistor current in the ON and OFF states) constitutes one of the main figures of merit of the transistor, and in modern applications it is required to be at least on the order of 10^4. Unfortunately, for monolayer graphene FETs the typical ON-Off ratio is about 10 making them practically unusable for digital electronics. Despite this, graphene FETs are an excellent alternative for high frequency applications (in the order of terahertz), where conventional silicon-based CMOS devices are not suitable and high ON-OFF ratio is not required.

To overcome this intrinsic limit, several techniques have been introduced to open a gap and modulate the ON-OFF ratio. A first attempt was made through external doping that allowed to obtain, with a certain precision, a desired gap value and reasonable ratios.[18] Other ways to open a gap in the graphene band structure are based on the exploit of the symmetry breaking, under transversal electric field, of bilayer sheets[19] or to substitute the flat graphene with a graphene tubular structure, as nanowires and nanoribbons.[20] While promising, these methods have the drawback of leading to devices with much lower mobility than monolayer graphene.

In conclusion, although graphene exhibits remarkable electronic properties that make it a suitable candidate for replacing silicon and extending the lifetime of Moore's law, there remains a lot of research to be conducted around overcoming the challenges associated with realizing graphene FETs for industrial purposes. To date, scalable and least costly technique for synthesizing graphene layers in industry, as chemical vapour deposition, results in samples with relatively low mobilities, making it difficult to harness the potential of graphene as a high-mobility alternative to silicon. Moreover, the research of bandgap engineering techniques to open a bandgap in graphene inevitably results in FETs with much lower mobilities than monolayer graphene FETs. Overall, it is difficult to establish whether graphene technology will be able to replace that silicon-based in the

near future. Fortunately, graphene is no longer the only known 2D material, as we will see in the next paragraph, and large research efforts are being made to find new 2D materials beyond graphene that can compete with modern silicon technology.

1.5 TMDs and other layered materials

After the revolutionary discovery of graphene, scientific research has focused on the possibility of isolating new 2D materials. Transition metal dichalcogenides (TMDs) are an emerging class of materials with properties that make them highly attractive for fundamental studies of novel physical phenomena and for technological applications ranging from nanoelectronics and nanophotonic to sensing and actuation at the nanoscale. The intense research efforts of the past years led to the demonstration of the first high performance TMD-based transistor in 2011 consisting of a single MoS_2 layer.[21] Radisavljevic et al. uses a hafnium oxide gate dielectric to demonstrate a room-temperature working transistor achieving mobility of $200\ cm^2V^{-1}s^{-1}$ and ON-OFF ratio in the order of 10^8.

TMDs' structure was first determined by Dickinson and Pauling in 1923[22] and the first reports on the use of adhesive tapes for producing ultrathin MoS_2 layers date back to 1963.[23] Certainly, the real boost occurred after the discovery of graphene in 2004 which marked the beginning of a deep research on the methods of production and characterization of 2D TMDs.

The TMDs family members can be described by the chemical formula MX_2, where M is a transition metal (Mo, W, V, Nb, Ti, Pt, Pd etc.) and X a chalcogen (S, Se, Te). TMDs exist in several structural phases resulting from different coordination spheres of the transition metal atoms.

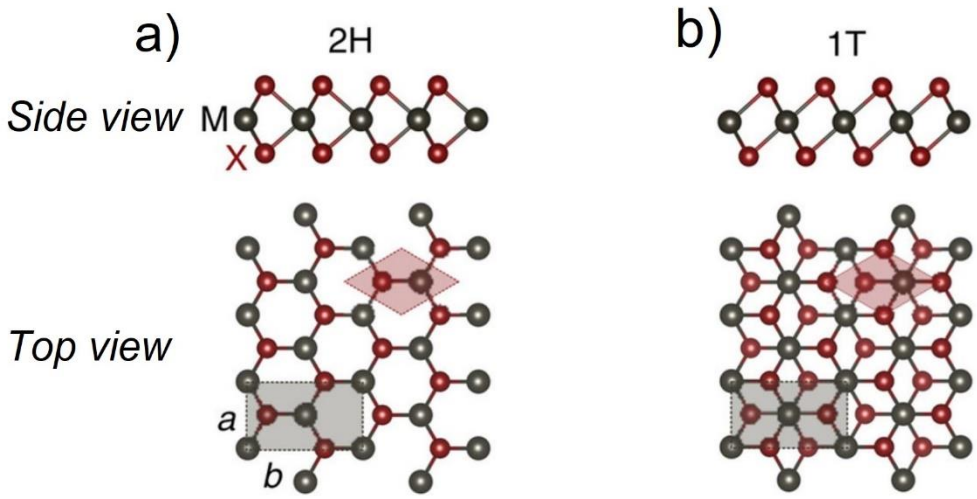


Figure 1.7 – Crystal structure of monolayer TMDs, where M indicates the transition metal and X the chalcogenide. The semiconducting 2H phase a) has trigonal prismatic structure, while the metallic 1T phase b) have octahedral structure.

Figure (1.7) shows the two common structural phases are characterized by either trigonal prismatic (2H) or octahedral (1T) coordination of metal atoms. These structural phases can also be viewed in terms of different stacking orders of the three atomic planes (chalcogen–metal–chalcogen) forming the individual layers of these materials. The 2H phases correspond to an ABA stacking in which chalcogen atoms in different atomic planes occupy the same position A and are located on top of each other in the direction perpendicular to the layer. By contrast, the 1T phases are characterized by an ABC stacking order.[24] The thermodynamically stable phase mainly depends on the particular combination of the transition metal and the chalcogen, but the other can often be obtained as a metastable phase. Each layer is bonded to another by van der Waals forces, which permits an easy exfoliation of the bulk material, while the X-M-X atoms are covalently bonded.

The two structural phases deeply affect the physical properties of the material, i.e. the band diagram, the electrical conduction, the optical properties and the metal or semiconducting nature. For example, monolayer MoS_2, in the 2H-tetrahedral phase, is a n-type semiconductor with a direct

tunable bandgap, while its 1T-octahedral structure leads to a metallic phase. Moreover, transition between 2H- and 1T-phase, for example under laser irradiation, have been demonstrated leading to very intriguing perspectives for the device realization. One of the main peculiarities of TMDs is the possibility of tuning the bandgap by varying the number of layers. Typically, the positions of the valence and conduction band edges change with decreasing thickness. As example, for $2H - MoS_2$ the indirect bandgap semiconductor bulk material turns into a direct bandgap semiconductor when reduced to monolayer.[25]

Moreover, other structures have then been discovered. An example is produced by $PdSe_2$, the first isolated noble TMD with 2D pentagonal structure.[26] Monolayer $PdSe_2$ has a puckered configuration where the Pd atoms are set in the middle and covalently bonded to four Se atoms, two of which are located respectively at the top and at the bottom of palladium layer.

The presence of a finished bandgap prompted research to attempt to use 2D TMDs in several technological applications. TMDs FETs operating at room temperature have shown encouraging results regarding typical figures of merit. Indeed, high ON-OFF ratio, up to 10^6, and current densities up to $250\ mA/mm$ have been reported. A negative point, however, is constituted by the mobility which is almost always very limited. This is mainly due to unavoidable structural defects due to manufacturing processes and to the interaction of TMDs with substrates. Continuous efforts have been made to improve the quality of the devices by optimizing the fabrication processes, but the highest mobilities obtained are in the order of a few hundred $cm^2V^{-1}s^{-1}$. [27] Besides excellent electrical transport, TMDs are mechanically flexible and strong, similar to graphene. An exceptionally high Young's modulus $T{\sim}0.33\ TPa$ has been reported in suspended few-layer MoS_2 nanosheets.[28]

A good compromise between the very high mobility typical of graphene combined with its absence of bandgap and the low mobility of TMDs, compensated by a large and tuneable bandgap, is constituted by black phosphorus (BP). This material, consisting of a single layer of phosphorus atoms represents a promise with reported transistor mobility as high as $1000\ cm^2V^{-1}s^{-1}$, approaching that of CVD graphene, and ON-OFF ratios typically $> 10^2 - 10^3$ at room temperature.[29] A big drawback of the BP is its great instability in the air. Indeed, monolayer BP has been shown to degrade within hours when directly exposed to air. Various encapsulation techniques have been attempted to prevent this effect, which although effective, make its industrial production much more difficult.

Another interesting emerging class of 2D materials is that of binary compounds of the IV and V groups. Theoretical calculations have indicated that MX coumpounds, with $M = Si, Ge, Sn$ or Pb and $X = P, As, Sb$ or Bi, might have crystalline layered structures with orthorhombic ($Cmc2_1$ for SiP and $Pbam$ for SiP_2 and $GeAs_2$) or monoclinic ($C2/m$ for $GeP, GeAs$, and $SiAs$) symmetries[30–33]. Several studies have investigated the bandgap[34], lattice structure[30], thermoelectric performances[35] and the Hall mobility[36] of such materials as bulk crystals, but there have been only few reports on their electrical properties in the form of ultra-thin or monolayer flakes[37,38]. We will delve into the electrical properties of one of its members, germanium arsenide, in the next chapter.

Finally, a special mention is needed for insulating 2D layered materials. These materials are characterized by a large bandgap (greater than $3\ eV$) and poor conduction, some examples are $h-BN$ (hexagonal-boron nitride)[39] and transition metal oxides (TMOs).[40] The usual large bandgap and high dielectric constant make 2D insulating materials desirable as gate dielectric to enhance the gate control on transistor channel and reach better performances. Another important property is

the possibility to tune the TMOs bandgap by varying the number of layers. As example, thin MoO_3 (around 10 layers) presents a gap of $3.3\ eV$ which becomes $4.3\ eV$ in bulk MoO_3, enabling its application as UV-light detector. Furthermore, 2D insulating materials possess high light transmittance, strong mechanical strength, excellent thermal/chemical stability and a dangling-bond-free surface.[41] Therefore, they can be excellently used as transparent protective layer for 2D devices.[42]

Chapter 2: FIELD-EFFECT TRANSISTORS WITH 2D CHANNEL

In this chapter the results of three experimental studies concerning the electrical properties of different 2D materials, used as FETs' channels, are reported. The aim of these works was to investigate the intrinsic transport properties of these materials under different conditions, such as temperature and pressure variations and light or electron irradiation. Even if referring to a specific 2D materials, most of the results are also valid when applied to other layered materials that presents similar characteristics. In the last section of the chapter an experimental study on a common problematic that affects nanostructured FETs is reported, i.e. the interaction of 2D materials with the metals used as contacts. In particular, a model that allows to describe the relationship between voltage and current in these devices is presented, in the very common case in which a double Schottky barrier is formed.

Specifically, in the first paragraph, the electrical properties of platinum diselenide, a member of the TMDs family, are investigated. The research focuses on investigating the electrical response of the material when exposed to supercontinuum white laser irradiation. It is demonstrated that the external pressure is responsible for different response to light of the material, leading to positive or negative photoconductivity in vacuum and at a room pressure, respectively. The research on the electrical properties of $PtSe_2$ was conducted in collaboration with the Tyndall National Institute of Cork and Trinity College of Dublin, which resulted in the publication of the paper "Coexistence of negative and positive photoconductivity in few-layer $PtSe_2$ field-effect transistors" by Grillo et al. published in Advanced Functional Materials in 2021.

In the second paragraph, the results regarding a study on black phosphorus FETs are presented. Non-volatile memories were realized exploiting the presence of intrinsic and BP/SiO_2 interface defects achieving devices with good endurance and retention properties. Poly (methyl

methacrylate) (PMMA) was used as covering layer to prevents the channel degradation, typical of black phosphorus devices, without affecting the electrical properties. Such results derive from a study conducted in collaboration with the University of Duisburg-Essen, which resulted in the writing of the paper "Memory effects in black phosphorus field effect transistors" by Grillo et al.

Then, in the third paragraph, an investigation on germanium arsenide FETs electrical properties as function of temperature is reported. The devices were measured over a wide temperature range revealing that the carrier density presents a broad peak around $75\,K$. Such an anomaly was explained through a temperature-dependent conductive channel thickness model that was corroborated by the observation of 3D variable range hopping conduction at lower temperatures that becomes band-type at higher temperatures. These results are the outcome of a collaboration with the Technical University of Denmark, where the devices were fabricated and characterized by the candidate during his time as a visiting PhD student. This research resulted in the publication of the paper " Observation of 2D conduction in ultrathin germanium arsenide field-effect transistors" by Grillo et al. which was published on ACS Applied Materials & Interfaces in 2020.

Finally, the fourth paragraph presents a discussion about the analysis of current-voltage measurements of 2D materials affected by the presence of Schottky barriers at both contacts. A model to analyse the transport mechanisms of these kind devices is proposed and tested on several $I-V$ curves from different nanostructures, revealing a perfect agreement between the theoretical predictions and the experimental data. This research work resulted in the publication of the paper "A current-voltage model for double Schottky barrier devices " by Grillo and Di Bartolomeo, published on Advanced Electronic Materials in 2020.

2.1 Platinum Diselenide ($PtSe_2$)

The first material studied in this PhD project is platinum diselenide ($PtSe_2$), a member of the TMDs family. In particular, $PtSe_2$ falls within the so-called noble TMDs formed by Group-10 noble elements (Pt, Pd, and so on) and chalcogens (S, Se, or Te). The main peculiarity of noble TMDs is that d-electrons completely occupy their d-orbitals, resulting in the highly hybridized P_z orbitals and strong interlayer interaction. Therefore, they present relatively small and widely tuneable bandgaps compared to traditional TMDs, which combined with high mobility and environmental stability make them of great interest for possible optoelectronic applications. For these reasons, $PtSe_2$, is currently the subject of intense research activity.[43–45] Bulk $PtSe_2$ is a gapless semimetal[46] for which theoretical studies have predicted a band gap emergence when reduced to monolayer.[47] Wang et. Al. through epitaxial growth by direct selenization of the material experimentally demonstrated that monolayer $PtSe_2$ has a band gap of $1.2\ eV$.[48] Due to its thickness-dependent semimetal-to-semiconductor transition, $PtSe_2$ is a suitable candidate for electronic[49] and optoelectronic applications.[50] Nowadays, $PtSe_2$ is attracting great research attentions due to its high carrier mobility[45], high chemical activity,[51] and low formation temperature.[52] Yim et al. have shown that $PtSe_2$ films, transferred onto silicon substrates, form diodes working as both photodetectors and photovoltaic cells.[53] Furthermore, theoretical studies have indicated that $PtSe_2$ has adsorption energy for gases like NO_2 and NH_3 lower than MoS_2 and graphene.[54] Su et al. have recently reported stable gas sensing performance of $PtSe_2$ under strains induced by different selenization temperatures.[55] $PtSe_2$ has weak chemical reactivity with oxygen that is physically adsorbed on its surface and can be removed by vacuum annealing, heating, or irradiation.[56] The interaction of O_2 with $PtSe_2$ is an important process to understand because it can deeply affect the transport properties of the material. The adsorption process does not lead to structural or chemical changes

of the material but induces p-type doping as electrons can transfer to oxygen molecules and cause hole formation inside $PtSe_2$.

The aim of this study was to investigate the effect of temperature, air pressure, and light irradiation on the transport properties of multilayer $PtSe_2$ back-gated field-effect transistors. It was found that the devices show p-type conduction and electrical conductivity that increases with the rising temperature and air pressure. The coexistence of negative and positive photoconductivity in the device has been demonstrated, and their relative contributions depend on the air pressure. Negative photoconductivity (NPC) is observed at atmospheric pressure as light irradiation by a white source reduces the $PtSe_2$ conductance. Conversely, in high vacuum, the material exhibits positive photoconductivity (PPC). The physical origin of this mechanisms is the pressure- or light-induced desorption of oxygen, which acts as a charge transfer dopant, affecting the $PtSe_2$ conductance. To provide atomistic insight, the interaction of physisorbed oxygen molecules with semiconducting $PtSe_2$ film has been studied by performing first-principles calculations, demonstrating that adsorption of oxygen on $PtSe_2$ surface induces holes in the $PtSe_2$ material, increasing its conductivity, consistently with the experimental observations.

2.1.1 Sputtering and selenization processes

Sputtering has been used to obtain a homogeneous Pt film (nominal thickness $0.7\ nm$). Pt was directly sputtered over an Si/SiO_2 substrate ($85\ nm$ thermally grown oxide on p-type silicon, $\rho \sim 0.001 - 0.005\ \Omega cm$). After that, a direct selenization process inside a two-zone furnace was performed. The upstream zone with Se pellets was heated to $220\ °C$ while the downstream zone housed the Pt film at $400\ °C$ for the selenization process.[53] The obtained Se vapor was carried to the downstream zone through an $Ar: H_2$ (90%:10%) flow at 150 sccm, where it reacted with the Pt films for 2 hours to completely convert it into a $PtSe_2$ ultrathin film. During the process, the Se

infiltrated into the Pt film causing the formation of $PtSe_2$ and a film thickness expansion by a factor of $\sim 3.5 - 4$.[57] Then, the compound was cooled down to room temperature. The final thickness of the $PtSe_2$ film, as revealed by TEM analysis, is about $3\ nm$ corresponding to 6 layers.[58]

A polymer-based process was used to transfer the obtained $PtSe_2$ film onto a fresh Si/SiO_2 substrate. Hence, SF_6-based inductively coupled plasma etching process with photoresist masking was performed to obtain the desired pattern. Standard photolithography and lift-off processes were carried out to fabricate $Ni{:}\,Au$ ($20\ nm{:}\,150\ nm$) metal contacts. The highly doped Si substrate was used as the gate electrode. An optical image of the device is shown in the inset of Figure (2.1 d).

2.1.2 Photoconductivity measurements and DFT calculation setups

For the electrical characterization, devices were measured in two- and four-probe configurations in a Janis Probe Station (Janis ST-500 probe station) equipped with four nanoprobes connected to a Keithley 4200 SCS (semiconductor characterization system), working as source-measurement unit with current sensitivity better than 1 pA. The electrical measurements were performed by lowering the pressure from $1\ bar$ (room pressure) to $10^{-5}\ mbar$ and at different temperatures from 292 K to 392 K. The air in the chamber was evacuated by a rough and a turbo pump. The photoconductivity was tested by irradiating the devices with a super-continuous white laser source (NKT Photonics, Super Compact, wavelength ranging from $450\ nm$ to $2400\ nm$, at $50\ mW/mm^2$).

First-principles calculations were performed within the framework of density functional theory (DFT) as implemented in QuantumATK.[59] Linear combination of numerical atomic-orbital (LCAO) basis set and generalised gradient approximation (GGA) with norm-conserving pseudopotentials from PseudoDojo[60] were employed in the simulations, where the semi-core 2*s*, 2*p* and 3*d* states for oxygen, 5*s*, 5*p*, 5*d*, 4*f,* 6*s* and 6*p* states for Pt, and 4*s*, 4*p*, 4*f*, and 3*d* states for Se have been

retained as valence electrons. Brillouin-zone integrations were performed over a grid of k points generated according to the Monkhorst-Pack scheme[61] with a density of approximately 12 k-points per angstrom. Energy cut-off of 125 Ha has been considered for discretized grid and all structural relaxation was performed with the maximum force of less than $0.005\,eV\,\text{Å}^{-1}$.[62] Van der Waals correction to the GGA functional[63] to correct the London dispersion is adopted for analysing the oxygen functionalization of $PtSe_2$. To analyse the effects of the oxygen adsorbate on $PtSe_2$ surface, a single oxygen molecule on a 3 × 3 × 1 bilayer $PtSe_2$ supercell, corresponding to the density of $\sim 9 \times 10^{13}\ cm^{-2}$, has been considered. The slab in the supercell is infinite and periodic in the x- and y-directions (parallel to the slab surface) and is finite along the z-direction (normal to the slab surface). The thickness of the vacuum region along z-direction is larger than $20\,\text{Å}$ to avoid any interaction between the periodic images of the neighbouring films. In the slab model calculation with adsorbate on the surface, an artificial macroscopic electrostatic field exists due to the periodic boundary conditions.[64] In order to avoid this artificial field in the $PtSe_2$ slab with oxygen molecule on the surface, we considered mixed Neumann and Dirichlet boundary conditions at the oxygen and $PtSe_2$ sides of the slab, respectively, which provides an alternative approach for the dipole correction in the slab calculations.[59]

2.1.3 Basic transistor characterization

Among the typical TMDs morphologies discussed in the first chapter, $PtSe_2$ presents a 1T crystal structure with octahedral coordination (in which six selenium atoms are bonded to a platinum atom located at the centre, as shown in Figure (2.1 a)), resulting in a Pt layer sandwiched between Se layers.[65] Transmission electron microscope (TEM) was used to collect an image of the $PtSe_2$ flake used for the electrical characterization, as shown in Figure (2.1 b), revealing a thickness of about $3\ nm$ corresponding to 6 atomic layers.[58]

The first electrical measurements were made to investigate the basic properties of the transistor at room temperature and are reported in Figure (2.1 c) and (2.1 d). The output characteristics, i.e. the $I_{ds} - V_{ds}$ curves, described in Equation (1.4), exhibit a linear behaviour, as shown in Figure (2.1 c). The application of the gate voltage affects the overall conductance of the transistor without modifying the $I_{ds} - V_{ds}$ linearity, with I_{ds} reduced by increasing V_{gs}.

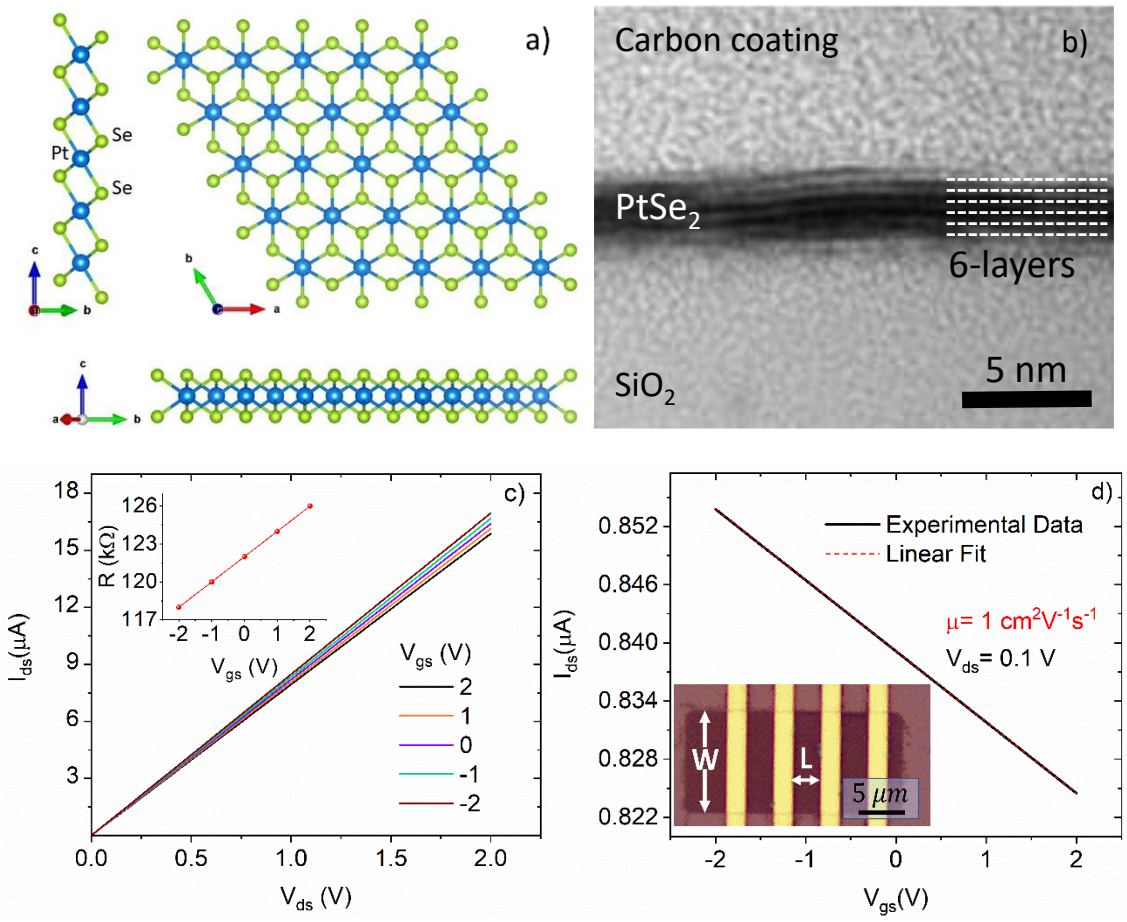


Figure 2.1 –a) Crystal structure of two-dimensional $PtSe_2$ showing an octahedral geometry with six selenium atoms bonded to a platinum atom located at the centre. b) TEM image of a $PtSe_2$ film revealing a thickness of about $3\ nm$ corresponding to 6 layers. c) Output characteristics acquired in 2-probe configuration for different gate voltages. The inset shows the channel resistance as function of the gate voltage. d) Transfer characteristic recorded at $V_{ds} = 0.1\ V$. The dashed red line shows the linear fit used to

obtain the field-effect mobility. The inset shows an optical image of the device. W and L represent the width and the length of the selected channel, respectively.

The transfer characteristic, as defined in chapter 1, was measured over a gate voltage sweep from $-2V$ to $+2V$ and it is reported in Figure (2.1 d). It shows a typical p-type behaviour with higher conductance at negative V_{gs}. The gate voltage range was intentionally limited to avoid leakage or breakdown of the $85\ nm$ gate oxide. The intrinsic p-type doping has been reported in previous works and can be attributed to Pt or Se vacancies and to the effect of oxygen adsorbates on the channel surface.[49,56,57] Furthermore, the use of Ni as the contact material facilitates hole injection as the Ni Fermi level aligns to the top of the valence band of $PtSe_2$. The field-effect mobility, defined in Equation (1.8) , has been obtained through the linear fit of the transfer curve (where $L = 4\ \mu m$ and $W = 10\ \mu m$ were channel length and width, respectively, $C_{ox} = \frac{\epsilon_0 \cdot \epsilon_{SiO_2}}{t_{SiO_2}} = 4.06 \cdot 10^{-8} \frac{F}{cm^2}$ was the capacitance per unit area of the gate dielectric with $\epsilon_0 = 8.85 \cdot 10^{-14} \frac{F}{cm}$, $\epsilon_{SiO_2} = 3.9$ and t_{SiO_2}= $85\ nm$ the vacuum permittivity, the SiO_2 relative permittivity and thickness, respectively; $V_{ds} = 0.1\ V$ is the voltage bias between drain and source). The obtained $\mu_{FE} \approx 1\ cm^2 V^{-1} s^{-1}$ is comparable with the one reported for differently fabricated $PtSe_2$ devices.[57,66]

2.1.4 Temperature and pressure dependent electrical properties

After the standard characterization of the transistor was completed, the aim of the study was to investigate how temperature and pressure influenced the $PtSe_2$ electrical transport properties. To do that, output and transfer characteristics were measured in the $292 - 392\ K$ temperature range and at different air pressures of 10^3, 1 and $10^{-5}\ mbar$. An increasing current/conductance with both rising temperature and air pressure was found, without any other apparent change in the

behaviour of the device. Figure (2.2 a) shows that the conductance G increases as the temperature rises, confirming a semiconducting behaviour. The air pressure also affects the conductance of the device. Indeed, the device is more conductive at atmospheric pressure than in vacuum. This effect is caused by oxygen that acts as a p-type dopant for the material,[67] and it will be further discussed in the next paragraphs.

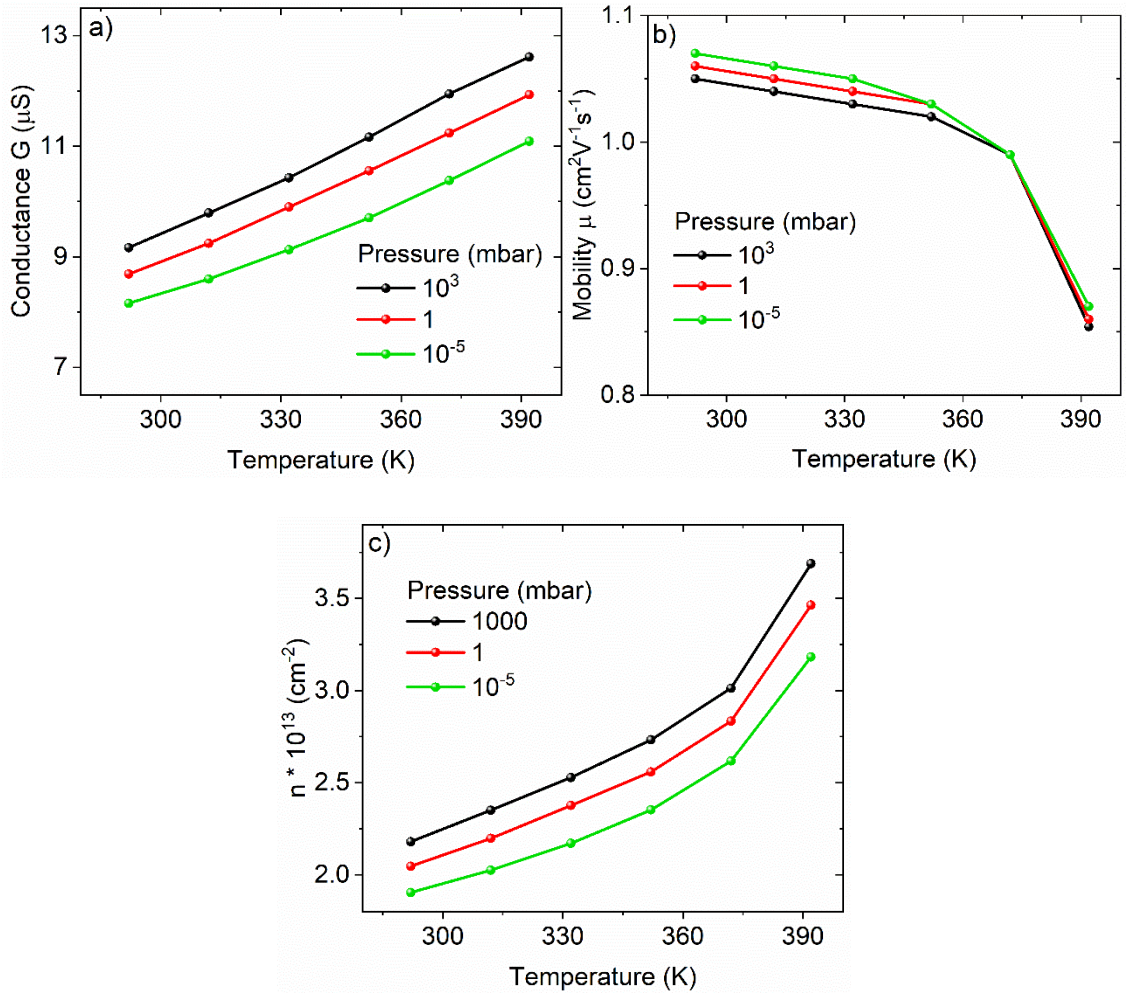


Figure 2.2 –a) Channel conductance, b) field-effect mobility and c) carrier density as a function of temperature for $1\ bar$ *(black dots),* $1\ mbar$ *(red dots),* $10^{-5}\ mbar$ *(green dots).*

Figure (2.2 b) shows that the mobility depends weakly on environmental pressure and temperature below 350 K.[68] In the device under study, ionized impurity scattering and phonon scattering balance each other with a slight predominance of phonon scattering which becomes relevant when the temperature rises beyond 350 K. Having obtained $\mu_{FE}(T)$ and $G(T)$ at each of the considered pressures, it is possible to estimate the carrier density per unit area n (in cm^{-2}) as a function of temperature for each pressure from the following equation:

$$n(T) = \frac{1}{q\rho(T)\mu(T)} \qquad (2.\ 1)$$

Figure (2.2 c) shows the typical semiconductor behaviour where the carrier density increases with the temperature. The obtained carrier concentration of about $10^{13}\ cm^{-2}$ is comparable with the one reported from Hall measurements carried out on similar devices.[49] Moreover, at atmospheric pressure the carrier density is larger than in high vacuum. This could be due to enhanced adsorption of oxygen on the channel surface at higher pressure that leads to increased p-type doping.

2.1.5 Light irradiation response: negative photoconductivity

After that, the investigation was focused on the main purpose of this work, i.e. $PtSe_2$ electrical response to light irradiation. Figure (2.3 a) shows $I_{ds} - V_{ds}$ characteristics recorded at air pressures of $1\ bar$ and $10^{-5}\ mbar$ both in dark and under white light irradiation. In high vacuum the light irradiation causes an increase in the conductivity as expected for a semiconducting material. Conversely, at atmospheric pressure, a reduction in conductivity, i.e. a negative photoconductivity, is observed under illumination. It is important to remark that the linearity of the $I_{ds} - V_{ds}$ characteristics of Figure (2.3 a) indicates that the drop in carrier concentration reported in Figure

(2.2 c) is not caused by $Ni/PtSe_2$ contacts becoming non-ohmic; otherwise stated, the current is not reduced by the formation of a Schottky barrier at metal/$PtSe_2$ interface but rather by a decrease in channel conductivity.

To further investigate the optoelectronic behaviour of $PtSe_2$, the electrical conduction of the device under light irradiation at different air pressures was measured. The super-continuous light source power was set to 20 mW/mm^2 and switched on and off every 3 minutes.

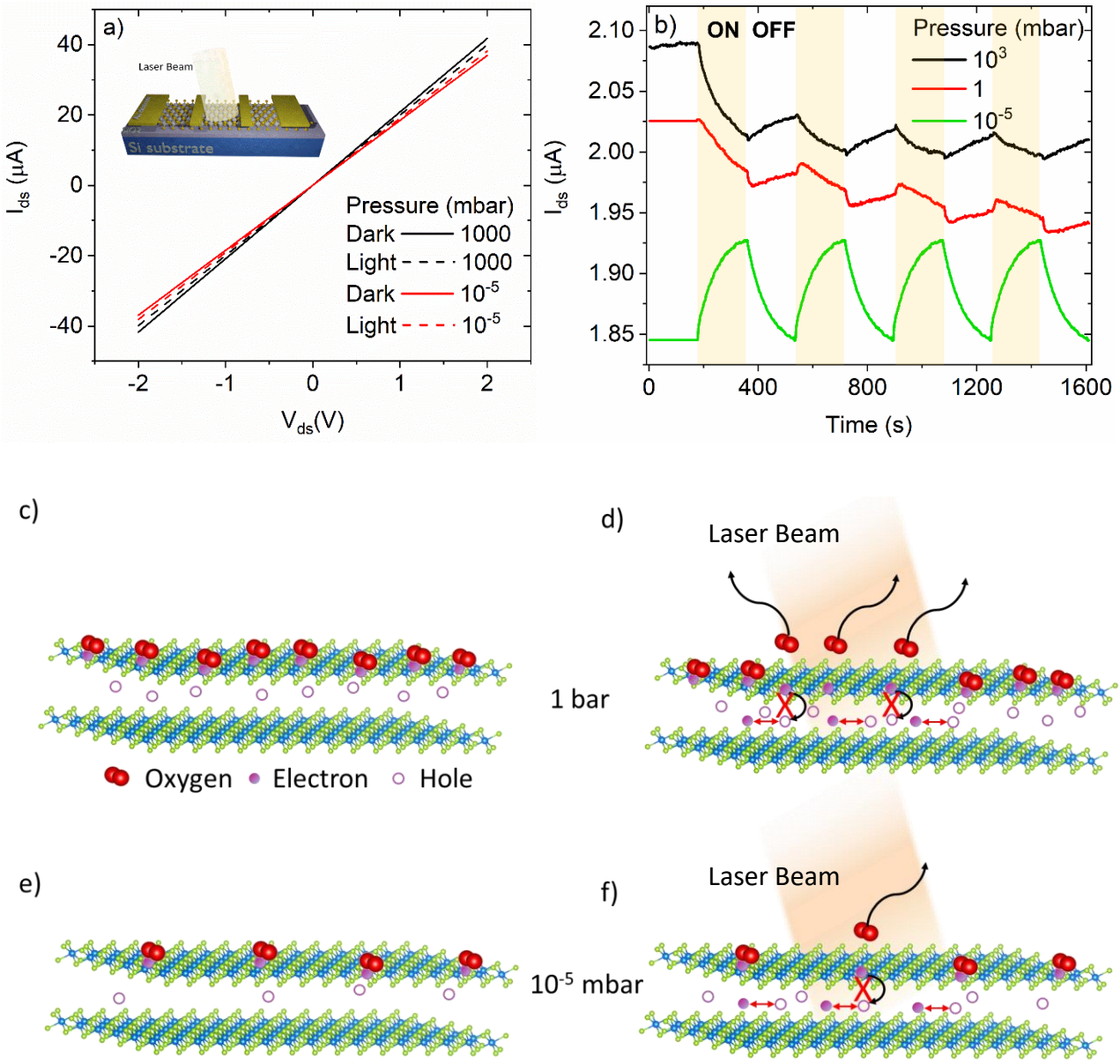


Figure 2.3 – a) $I_{ds} - V_{ds}$ *characteristics in dark (continuous lines) and under super-continuous 450-2400 nm*

light source irradiation (dashed lines), recorded at $1\ bar$ *(black lines) and* $10^{-5}\ mbar$ *(red lines). The inset shows a schematic of the device under light irradiation. The laser spot of about* $1\ mm^2$ *was located between the two contacts to completely cover the channel. b) Current vs time characteristics at* $10^3\ mbar$ *(black line),* $1\ mbar$ *(red line),* $10^{-5}\ mbar$ *(green line) under switching light. The laser was switched on (yellow zone) and off (white zone) every 3 minutes. c) At* $1\ bar$*, in dark, the large amount of oxygen adsorbed on* $PtSe_2$ *traps electrons at the surface and induces p-type doping in the material. d) When the device is exposed to light, oxygen is removed from the surface. Free electrons are trapped or recombine with holes reducing the density of available carriers and resulting in a negative photoconductivity. e) At* $10^{-5}\ mbar$ *the amount of adsorbed oxygen is limited and so is the p-type doping of the material. f) When the device is exposed to light, the photogenerated electron-hole pairs and charge-carrier detrapping increase the conduction in the material, leading to a positive photoconductivity.*

Figure (2.3 b) shows the device channel current under irradiation, measured at $V_{ds} = 0.1\ V$ and $V_{gs} = 0\ V$. At a pressure of 10^{-5} *mbar*, the dark current is $\sim 1.85\ \mu A$. When the light is turned on, the current increases, reaching a value of $\sim 1.93\ \mu A$. This behaviour is likely dominated by extrinsic photoexcitation, i.e. transitions involving deep trap states, which increase the material conductivity with a characteristic time of $72\ s$. First-principles calculations have demonstrated that the formation of deep trap states can be caused by that Se antisites at Pt sites, as well as Pt and Se vacancies.[58] Photoexcitation from deep trap states can result in long response times.[69] Indeed, photocurrent with rising and falling times of dozens seconds have been reported in similar devices with 2D materials such as MoS_2[70,71] or ReS_2.[69,72]

When the light is switched off, recombination and carrier trapping make the current to return to its initial value. The photoresponsivity R of the device was evaluated through the relation $R =$

$\frac{I_{Light}-I_{Dark}}{PS}$, where I_{Light} and I_{Dark} are the current under illumination and in dark recorded at $V_{ds} = 0.1\ V$ and $V_{gs} = 0\ V$ respectively, P is the incident laser light power and S is the irradiated area. Considering an optical power of $2 \cdot 10^{-8} \frac{W}{\mu m^2}$ and an effective area of $40\ \mu m^2$, $R{\sim}0.2 \frac{A}{W}$ was obtained. The achieved value is comparable with similar phototransistor realized with both $PtSe_2$ and different 2D materials. Wang et al.[73] reported a low photoresponsivity of $0.19 \frac{mA}{W}$ for $PtSe_2$ phototransistors measured under incident light at $1550\ nm$ and when $V_D = 5\ V$, mainly ascribed to insufficient absorption of incident light of the material. Yu et al. showed that such absorption, and thus the photoresponsivity, can be improved by hybridizing $PtSe_2$ with a photonic waveguide.[74] Another route to enhance the photoresponsivity is the use of different substrates. Indeed, Li et al.[75] reported that few-layer $PtSe_2$ on $h-BN$ substrate can reach a photoresponsivity as high as $1.56 \cdot 10^3\ A\ W^{-1}$. Similar studies, conducted on other 2D materials, have demonstrated that the photoconductivity can range from few $\frac{mA}{W}$ from graphene-based devices[76] until to $10^6 \frac{A}{W}$ for black-phosphorus photodetectors.[77] At the pressure of $1\ mbar$, a different behavior is observed. The higher dark current can be ascribed to the interaction between the material surface and the environmental oxygen. When the light is switched on, a sudden increase, appearing as a small step-up, is observed in the current. Such a step is followed by a steady decrease. When the light is switched off, the current suddenly drops with an analogous small step-down and then increases slowly, without attaining its initial value. The successive light pulses result in a further overall decrease of the current. A similar, but more dramatic behaviour is observed at atmospheric pressure. In this case, when the device is illuminated, the current decreases faster and recovers only partially when the light is switched off.

The reduction of current during illumination is known as negative photoconductivity and has been observed in other materials.[78,79] Its origin has not yet been fully understood although most studies attribute it to a photogating effect,[67] an electronic transition to the defect state levels[80] or interaction with adsorbates.[81,82]

The photogating effect is observed when electron-hole photogeneration occurs in Si or $PtSe_2$ followed by charge trapping at the interface with SiO_2. Indeed, favoured by the vertical up-bending of the Si bands, photo-generated holes can be trapped at the Si/SiO_2 interface acting as a positive gate that lowers the channel conductance.[67] However, this phenomenon should be independent of the external pressure. Since rise and fall time are quite long, the conductance modulation could be ascribed to light induced heating and cooling. Figure (2.2 a) shows that the conductivity of the device increases with the temperature independently from the external pressure, hence a thermal effect would not be able to explain the negative photoconductivity at atmospheric pressure. Although the photogating and the thermal effects could play a role, the results of Figure (2.3 b) suggest that other mechanisms take place and dominate the optoelectronic behaviour of $PtSe_2$. The dependence on pressure suggests that such mechanisms involve adsorption and desorption of air molecules.[56]

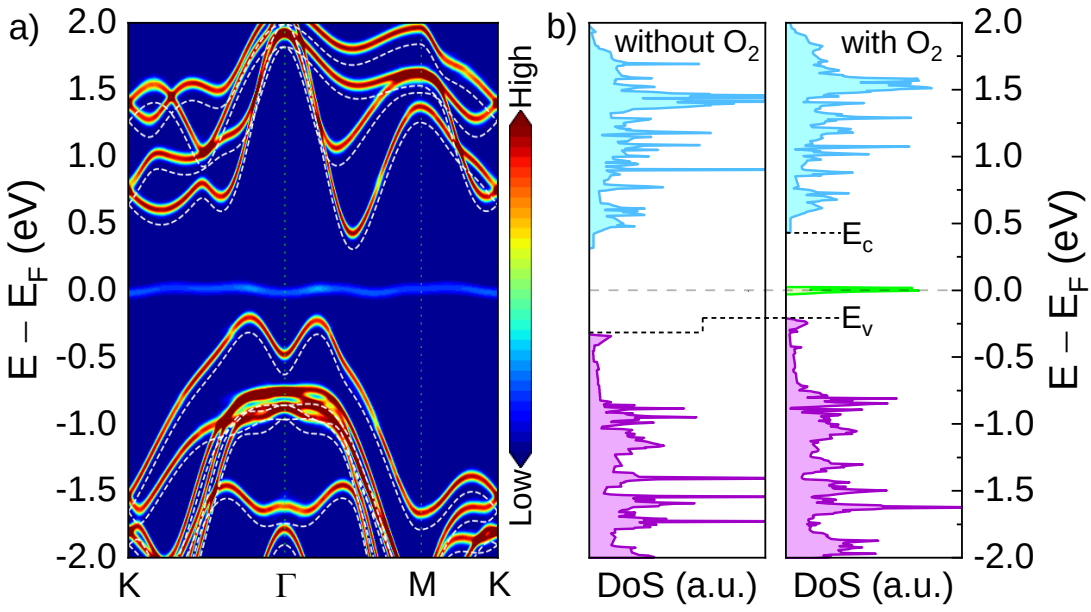
At atmospheric pressure there is a large amount of oxygen molecules adsorbed on the material surface, as shown in Figure (2.3 c). Such adsorbates attract free electrons from $PtSe_2$ leaving holes inside the material. These holes are responsible for the p-type conductivity and the higher carrier density measured at atmospheric pressure. When the material is exposed to light, oxygen is easily removed from the surface[83] and the free electrons can recombine with the holes in the material , as shown in Figure (2.3 d). A similar behaviour has been already reported for MoS_2 phototransistors.[84] Indeed, it has been shown that the use of sufficiently short wavelength light

source causes desorption of water and oxygen molecules affecting both the responsivity and the response time of the devices. Moreover, although not explicitly shown in Figure (2.3 d), the presence of environmental humidity can also affect the conductivity of the device acting as positive dopants that can be removed through light illumination.[84] The outcome of the process is a decrease in the total concentration of carriers which results in the observed decrease in the conductivity of the material. When the pressure is decreased to $10^{-5}\ mbar$, adsorbed oxygen is partially removed from the surface resulting in the reduced conductivity of the material, as shown in Figure (2.3 e). In this case, when the channel is exposed to light, the dominant process is the photogeneration of electron-hole pairs and charge detrapping. The excess carriers increase the conductivity of the material, leading to the observed positive photoconductivity (Figure (2.3 f)). At the intermediate pressure of $1\ mbar$ both processes coexist. Indeed, when the light is first turned on, a step-up in conductivity is observed due to the photogeneration of electron-hole pairs, which is a fast process. Then, the neutralization and desorption of oxygen, which is a slower process, induces a slow decrease of current. When the light is switched off, a step-down in the current is caused by excess electron-hole recombination, followed by a slower current increase due to oxygen re-adsorption on the $PtSe_2$ surface.

2.1.6 DFT calculations: the effect of physisorbed oxygen

In this paragraph, the results from DFT calculations that were used to clarify the impact of physisorbed oxygen molecules on the semiconducting $PtSe_2$ surface are reported. A single oxygen molecule on a bilayer $PtSe_2$ supercell has been considered. Although the experimental film is composed by 6-layers, the DFT calculations was performed on bilayer $PtSe_2$ because of the well-known underestimation of the bandgap in DFT-based calculations.[49] Thinner (bilayer) $PtSe_2$ was considered in the DFT calculations to be consistent with the experiments in achieving

semiconducting film with comparable bandgap values. As the size of the supercell is larger than the primitive cell, the corresponding first Brillouin zone is smaller. Hence, the $PtSe_2$ slab plus oxygen molecule band structure (supercell structure) is "folded" into the first Brillouin zone. Consequently, to be able to directly compare the folded bands with the reference band structure of the $PtSe_2$ primitive cell, i.e. $PtSe_2$ unit cell without oxygen adsorbate, a procedure known as "unfolding" has been employed to unfold the primitive cell Bloch character hidden in the supercell eigenstates.[85,86] The unfolded band structure of the $PtSe_2$ slab plus oxygen molecule is displayed as a contour plot in Figure (2.4 a). The primitive $PtSe_2$ band structure is shown by white dashed lines as reference in this figure and the energies are referenced to the Fermi energy (E_F). As can be conspicuously seen by comparing the two band structures, the unfolding method reveals a rather remarkable shift of the E_F towards lower energies, i.e. p-type characteristic, due to the presence of the oxygen adsorbate, while the band structure of the $PtSe_2$ is rather unperturbed.



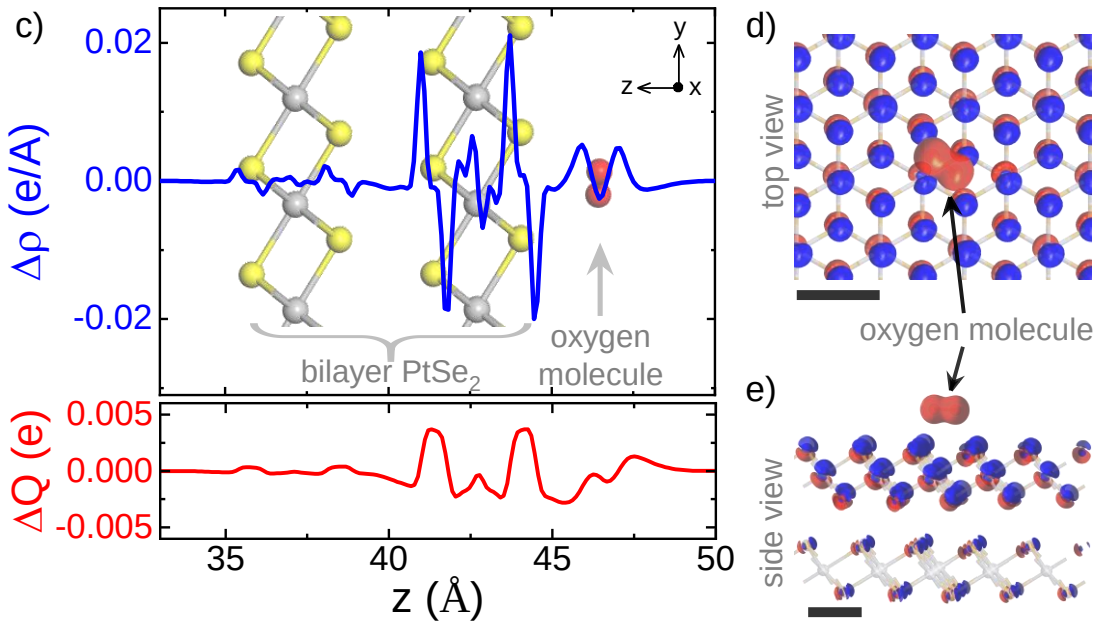


Figure 2.4 –a) Unfolded band structure of the semiconducting $PtSe_2$ with a physisorbed oxygen molecule on the surface using a contour plot of total weight intensity as a function of wave vector in the two-dimensional Brillouin zone. Red (blue) represents high (low) spectral weights. The band structure of the $PtSe_2$ without an oxygen molecule is shown using white dashed lines. Energies are referenced to the Fermi energy. b) DoS of the $PtSe_2$ film with and without oxygen adsorbate on the surface. The Fermi level is at the zero of energy as shown by the grey dashed line. The p-type character of the system with an oxygen molecule is evident. The energy states illustrated in green correspond to the oxygen molecule. c) Plane-averaged charge difference density ($\Delta\rho$) superimposed on the $PtSe_2$ atomic structure with an oxygen molecule, aligned to the z-direction (x-axis) (upper panel in blue) and charge transfer (ΔQ) (lower panel in red) of the structure referenced to the $PtSe_2$ supercell without oxygen molecule. d) and e) Top-view and side-view of the $0.07\ e/\text{Å}^3$ CDD isosurface, demonstrating the effects of oxygen adsorbate on the charge distribution in the lateral direction (x-y plane) and along the z-direction, respectively. Red (blue) represents accumulation (depletion) of electrons referenced to the $PtSe_2$ supercell without oxygen molecule. Scale bars in d) and e) are 3.78 Å.

Figure (2.4 a) also shows the oxygen molecule-induced states are created near the E_F closer to the $PtSe_2$ valence band edge. The nature of these states can be identified through the unfolded band structure, where these states exhibit expected almost dispersionless energy states in the band structure. The density of states (DoS) at the same energy window, with and without the oxygen molecule on the $PtSe_2$ surface, are presented in Figure (2.4 b), illustrating the band alignment of the two structures. The occupied double states shown in green are associated with the physisorbed oxygen molecule.

To quantify the charge transfer to/from the molecule, plane-averaged charge difference density (CDD), $\Delta\rho(z)$, along the z-direction is calculated by integrating $\Delta\rho(r)$ within the x-y plane. Accordingly, for a plane located at distance z normal to the $PtSe_2$ plane, the amount of charge transfer is obtained using $\Delta Q(z) = \int_{-\infty}^{z} \Delta\rho\,(z')\,\mathrm{d}z'$. To analyse the charge interaction between the oxygen adsorbate and the semiconducting $PtSe_2$ film, the plane-averaged $\Delta\rho(z)$ referenced to the $PtSe_2$ supercell without oxygen adsorbate, is plotted together with the amount of charge transfer $\Delta Q(z)$ in the upper and lower panel of Figure (2.4 c), respectively. As can be seen, the oxygen molecule acts as an electron acceptor by gaining ~0.004 e at the interface from $PtSe_2$ (e is the elementary charge of an electron). The top-view and side-view of the isosurface of the CDD referenced to the $PtSe_2$ supercell without oxygen adsorbate are depicted in Figure (2.4 d) and (2.4 e), respectively, where red (blue) represents accumulation (depletion) of electrons. Notably, although the lateral redistribution of charges upon oxygen adsorption is quite negligible (see top-view image in Figure (2.4 d), there is a distinct charge redistribution, particularly between the oxygen molecule and the top layer of the bilayer $PtSe_2$ as can be seen in the side-view (Figure (2.4 e)).

2.2 Black Phosphorus (BP)

The second 2D material that has been investigate as FET channel is black phosphorus (BP). As mentioned in Chapter 1, it is a layered material in which, similarly to graphite, individual atomic layers are held together by van der Waals interactions.[87] In the single-layer limit, BP is also known as phosphorene and has a numerically predicted direct band gap of $\sim 2\ eV$ at the Γ point of the first Brillouin zone.[88] With the increasing number of layers, the interlayer interactions reduce the bandgap to a minimum of $0.3\ eV$ for bulk BP[89] moving the direct gap to the Z point.[90]

Commonly, BP presents an orthorhombic crystal structure with puckered layers[87] in which each phosphorus atom is connected with the nearest three atoms through covalent bonds, thus forming layers with a corrugated shape. According to theoretical studies BP could also have different structures such as simple cubic, diamond, orthogonal and nanorod, but the orthorhombic structure is the thermodynamically most stable allotrope at $0\ K$.[91]

The distance between two neighbouring layers is approximately $0.5\ nm$, slightly larger than the interlayer distance in graphite ($0.36\ nm$). Hence, BP can store charged ions better than graphite and has been proposed for energy storage applications.[92]

As discussed in Chapter 1, BP represents a good alternative to graphene thanks to its high mobility combined with the presence of a finite bandgap that makes it suitable for the realization of FETs. Moreover, BP thickness-dependent direct bandgap could lead to applications in optoelectronics, especially in the infrared region. Several devices have already been proposed and studied; Li et al.[29] reported reliable transistor performance with five orders of magnitude drain current modulation and charge-carrier mobility up to $\sim 1000\ cm^2\ V^{-1}\ s^{-1}$ obtained from $10\ nm$ thick samples. Ren et al.[93] used BP nanosheets to realize self-powered photodetectors with superior photoresponse activity under light irradiation and environmental robustness, showing that BP is a promising

building block for optoelectronic devices. Moreover, BP has been also proposed for solar cells,[94] as humidity sensor,[95] or for live cell imaging[96]. A remarkable application of BP has been in the field of memory devices. Common non-volatile FET-based memories use a charge-trapping layer to accumulate and retain the electric charge induced by a gate pulse. Similar devices, with channel based on several 2D-materials, including BP, have been already proposed and demonstrated. In particular, Feng et al.[97] reported that few-layer BP channel FETs with a $Al_2O_3/HfO_2/Al_2O_3$ charge-trapping gate stack enable memory devices with programming window exceeding $12\ V$, due to the extraordinary trapping ability of high-k HfO_2, and endurance exceeding 120 cycles. Tian et al.[98] used a similar structure, where the charge trapping layer consisted only of Al_2O_3, to demonstrate an ambipolar BP charge-trap memory device with dynamically reconfigurable and polarity-reversible memory behaviour. In such a device, the polarity of the carriers in the BP channel can be reversibly switched between electron- and hole-dominated conductions allowing four different memory states and, hence, two-bit per cell data. Finally, Lee et al.[99] showed that gold nanoparticles as charge trapping layer for mechanically-exfoliated few-layered BP FETs enable large memory window ($58.2\ V$), stable retention ($10^4\ s$), and cyclic endurance (1000 cycles).

However, the practical implementation of these promising devices is hindered by the intrinsic instability of mono- and few-layer BP. While bulk crystals are quite stable in air, BP flakes thinner than $10\ nm$ degrade in few days, or even in few hours if the thickness is reduced to the single layer.[87] Indeed, when exposed to oxygen, devices obtained through mechanical exfoliation[100] or solvent exfoliation[101] of bulk crystals are affected by fast oxidative degradation.[102,103] Moreover, the degradation process can be enhanced by exposure to light through photo-oxidation.[104] To tackle with this issue, different stabilization processes have been tried. As first attempt, BP has been functionalized through TiO_2, Al_2O_3, titanium sulfonate ligand (TiL_4), polyimide, or aryl

diazonium.[105–109] Encapsulation with other 2D materials, such as graphene and boron nitride, has been considered as well.[110] Furthermore, it has been reported that the use of ionic liquids can suppress BP degradations for months.[111]

Although these first approaches have provided encouraging results, an efficient stabilization of BP, also compatible with standard fabrication processes of high performance devices remains still an ongoing challenge.

In the following sections, the fabrication and the electrical characterization of back-gated BP FETs is reported. The presence of intrinsic and BP/SiO_2 interface defects was exploited to realize non-volatile memories with good endurance and retention properties. By comparing samples exposed directly to the air with others covered by poly (methyl methacrylate) (PMMA), it was possible to demonstrate that PMMA does not affect the electrical properties of the devices but prevents the channel degradation at least for one month.

2.2.1 Exfoliation and devices' fabrication

To obtain few-layers BP flakes a standard mechanical exfoliation method by adhesive tape was used. The starting point was a bulk BP single crystals (Smart Elements) from which the flakes were exfoliated and then transferred onto degenerately doped p-type silicon substrates, covered by $90\ nm$-thick SiO_2, on which they were located through optical microscopy. Figure (2.5 a) shows the typical crystal structure of few-layer BP. To obtain typical FETs configuration, a standard photolithography process followed by electron beam evaporation was used to deposit $10\ nm\ Cr/100\ nm\ Au$ electrodes, as shown in Figure (2.5 b). A back-gate contact was formed covering the scratched area of the Si substrate with silver paste.

Electrical measurements were carried out using the same experimental setup described in the previous paragraph, for $PtSe_2$ characterization.

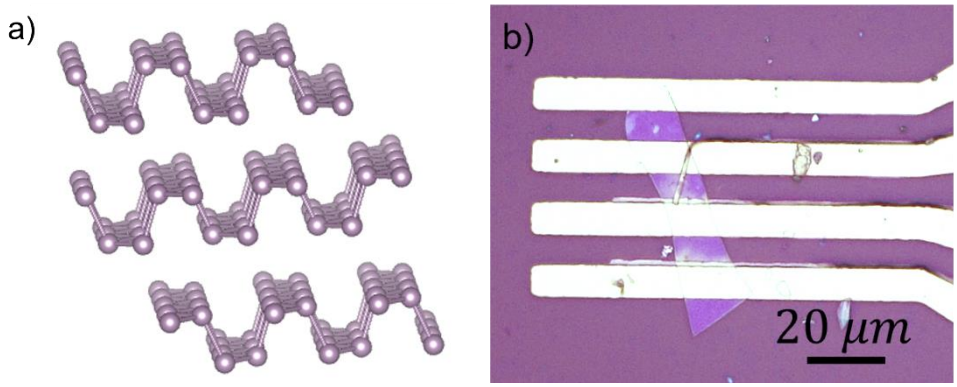


Figure 2.5 – a) Crystal structure of few-layer BP. b) Optical image of the device showing a BP flake covered by four Cr/Au contacts.

2.2.2 Room temperature transistor characterization

As in the case of $PtSe_2$, the first approach was always to carry out a standard characterization of the transistor at room temperature, in order to evaluate its basic properties. To avoid considering the contact resistance and isolate the intrinsic transport mechanism of the material, a standard four-probe measurement was carried out. Figure (2.6 a) shows a schematic of the experimental setup. The current (I_{xx}) is forced between the outer contacts while the voltage drop (V_{ds}) is measured between the inner contacts. Figure (2.6 b) shows the characteristics for both 4-probe ($I_{xx} - V_{ds}$) and 2-probe ($I_{ds} - V_{ds}$) configurations resulting in a channel resistance of $3.5\,k\Omega$ and $3.6\,k\Omega$, respectively. Since the difference between the two methods is less than 3%, indicating that the contacts are ohmic with low contact resistance[112,113], in the following the 2-probe configuration has been used for easier measurements. The electrical characterization of the BP transistor at room temperature is reported in Figure (2.6 c) and (2.6 d).

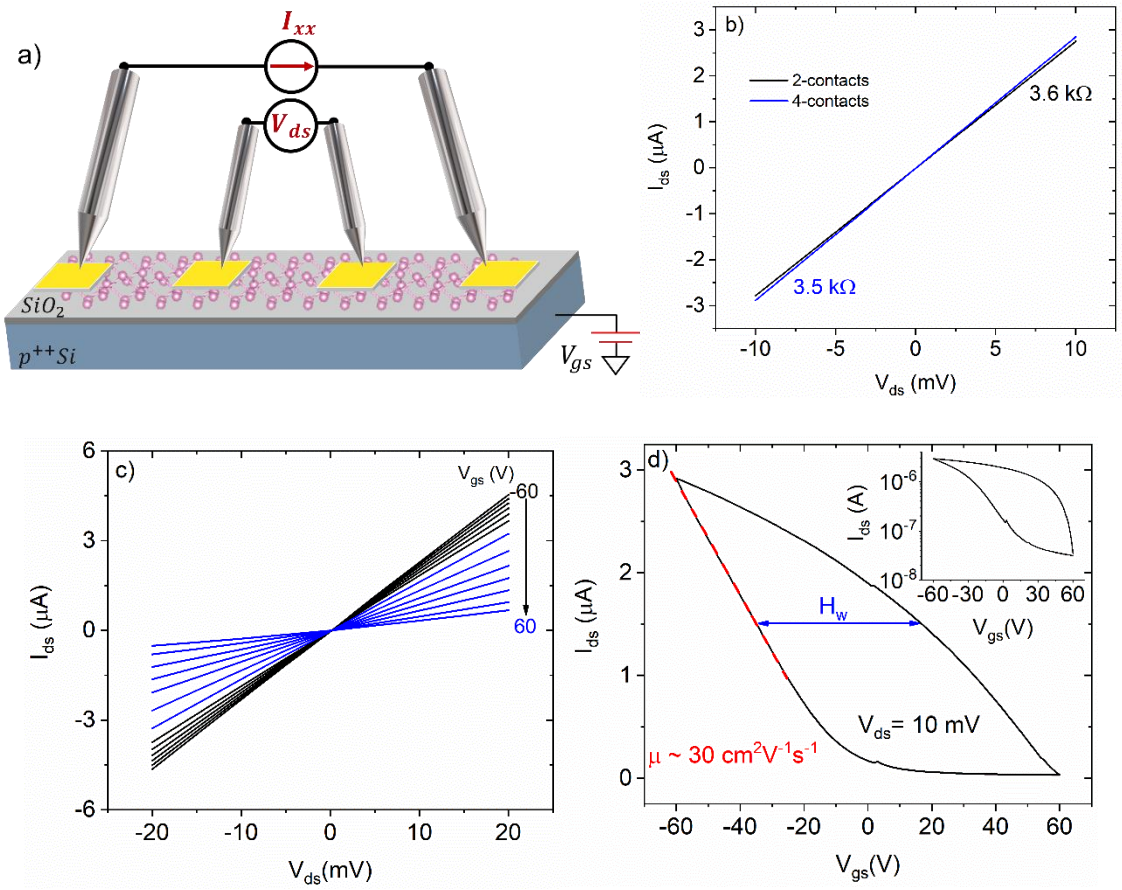


Figure 2.6 – a) Schematic of the setup used for the four-probe electrical characterization. The current (I_{xx}) is forced between the outer contacts while the voltage drop (V_{ds}) is measured between the inner contacts. b) $I_{ds} - V_{ds}$ characteristics measured in two- and four- probe configuration. c) Output characteristic of the device recorded in two-probe configuration with the gate voltage ranging from $-60\ V$ to $60\ V$ (blue lines are referred to positive gate voltages). d) Transfer characteristic measured over a loop of the gate voltage between -60 V and 60 V. The dashed red line represents the linear fit used to estimate the field effect mobility. The inset shows the transfer curve with the current on a logarithmic scale.

The output characteristics exhibit a linear behaviour. The application of a negative gate bias leads to an increase of the channel current, typical of a p-type device, and does not affect the linearity of the $I_{ds} - V_{ds}$ characteristics.[113] The transfer characteristic, measured at fixed $V_{ds} = 10\ mV$ over a

loop of the gate voltage is reported in Figure (2.6 d), confirming the p-type behaviour, with a modulation of about two orders of magnitude. The OFF state of the transistor was not reached in the applied voltage range, which was intentionally limited to avoid the breakdown of the gate dielectric. Considering the non-linear behaviour of the transfer characteristics, the channel current can be expressed through Equation (1.6).

Following the procedure reported in the previous paragraph, imposing $W = 10\ \mu m$ and $L = 5\ \mu m$ and $C_{ox} = 3.84 \cdot 10^{-8}\ \frac{F}{cm^2}$, and using Equation (1.8) it was possible to obtain a relative high mobility $\mu_{FE} \sim 30\ cm^2 V^{-1} s^{-1}$, considering that the sample was not subjected to any functionalization, that is slightly below both the theoretically predicted[114,115] and the experimentally measured mobilities in similar devices.[116,117] Such a mobility is higher or comparable with the one obtained in SiO_2 back-gate FETs fabricated with other 2D materials.[118–121]

The large hysteresis width, $H_w \sim 60\ V$, here defined as the V_{gs} difference corresponding to the current of $1.5\ \mu A$, is mainly due to charge trapping impurities and has already been reported for similar devices.[122–125] Gate-induced hysteresis can be ascribed to charge transfer from/to intrinsic and extrinsic trap states. Intrinsic traps correspond mostly to BP crystal defects such as phosphor vacancies,[126] or grain boundaries,[127] while extrinsic traps are related to environmental adsorbates, like water and oxygen molecules, defects located at the metal/BP interface, and at the BP/SiO_2 interface.[122]

2.2.3 The role of trap states on transfer characteristic hysteresis

The hysteresis of the transfer characteristic reported in the previous section is typical of most of 2D FETs and it is usually ascribed to both intrinsic and extrinsic defects. One of the aims of this study was to investigate the origin of this hysteresis and try to exploit it for the realization of practical devices, as it will be discussed in detail in the follow. In the case of BP, oxygen adsorbates are a

common source of extrinsic defects, but although it is well known that oxidation of the surface involves the dissociative chemisorption of oxygen that can cause the decomposition of BP and the decrease in FET performance, it is expected that water and oxygen play a marginal role in the formation of hysteresis in the reported study because the electrical measurements were carried out in high vacuum to remove the surface adsorbates. Thus, traps at the BP/SiO_2 interface, intrinsic BP defects and border traps in SiO_2 as well as mobile charge in the SiO_2 layer are most likely responsible for the device hysteresis.

To better understand the origin of hysteresis the transfer characteristics were measured at different sweeping times. Figure (2.7 a) shows several transfer characteristics with H_w increasing as function of the voltage sweep duration in the range $12 - 322\ min$. The exponential fit, showed in Figure (2.7 c), reveals a RC- growth with a single time constant $\tau = 191\ min$. Such a long characteristic time reduces the probability that BP/SiO_2 interface traps contribute to the hysteresis since it has already been reported that interface traps are fast traps.[128]

Then, slow trap states can be ascribed to both BP and SiO_2 trap states. Particularly, slow border traps in SiO_2 have already been reported and attributed to trivalent silicon dangling bonds or hydrogenic defects.[129] From the time constant τ, it is possible to evaluate the involved capacitance as $C = R/\tau$, where R is the inverse of transconductance $g_m = \frac{\partial I_{ds}}{\partial V_{gs}} \sim 0.3\ nS$. $C \sim 3\mu F$ was obtained, which is higher than gate oxide capacitance, in the order of the pF, implying that the trap-related capacitance is the dominant one.

Such a capacitance can also be obtained through the sub-threshold swing SS that is the gate voltage change corresponding to one-decade increase of the transistor current. Indeed, as described in Equation (1.11) SS is a function of the charge trap capacitance and the depletion layer capacitance and it can be rewritten as:

$$SS = \frac{dV_{gs}}{dLog(I_{ds})} \approx \log(10)\frac{kT}{q}\left(1 + \frac{C_T + C_{DL}}{C_{OX}}\right) \quad (2.\ 2)$$

where, k is the Boltzmann constant, $T = 300\ K$ is the temperature and q is the electric charge. By neglecting the depletion layer capacitance, C_{DL}, with respect to the charge trap capacitance, C_T, (a reasonable assumption considering the low modulation of the current) and, having obtained $SS \sim 30\ V/dec$, a trap capacitance, $C_T \sim 20\ \mu F$ was estimated, that is consistent with the one previously obtained.

To corroborate the hypothesis that slow trap states contribute to hysteresis the transfer characteristic was measured while irradiating the device with a super-continuous white laser source at $50\ mW/mm^2$; after that, the measurements were repeated in dark every 10 minutes. Figure (2.7 b) shows that under illumination (black line) the device conductance and the hysteresis width are enhanced. This result is expected as the illumination causes both the generation of electron-hole pairs and excitation of trapped charges, which increase the carrier concentration in the material. Charged traps, emptied of free carriers, induce an enlargement of the hysteresis. By repeating the measurements in the dark, the conductance as well as the hysteresis decrease until they stabilize after about an hour. Figure (2.7 d) shows how H_w varies after light irradiation. The best fit is obtained through a double decreasing exponential, one with a small time constant ($\sim 5\ s$) and a predominant one with a long characteristic time ($\sim 42\ min$). The fast time constant is related to electron-hole pair recombination, while the longer one supports the conclusion that hysteresis is dominated by intrinsic deep slow traps.

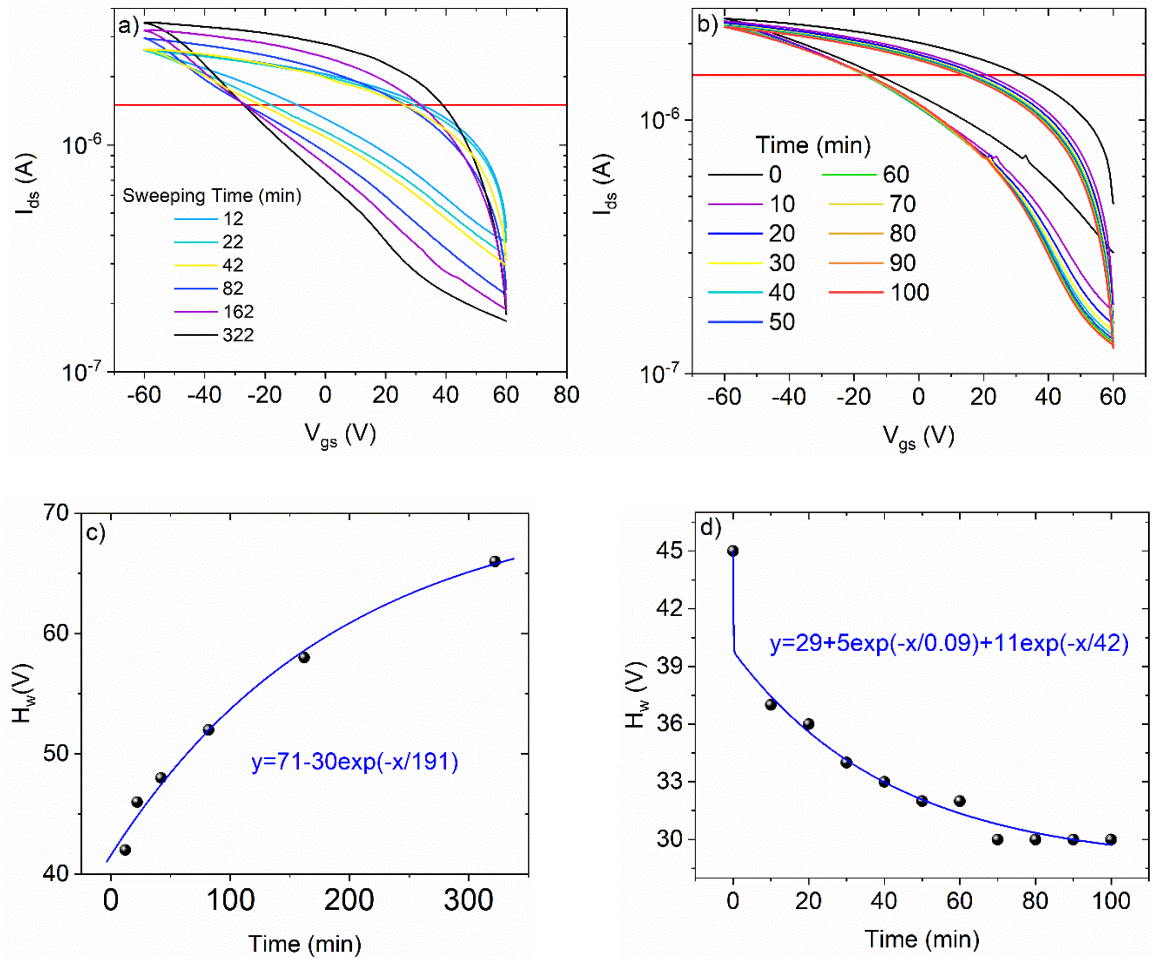


Figure 2.7 – a) Transfer characteristics recorded at different sweeping times ranging from 12 min to 322 min. The horizontal red line indicates the current value used to evaluate the hysteresis width. b) Transfer characteristics measured under supercontinuous white laser illumination (black line) and in dark every 10 minutes after the laser was switched off. c) Exponential fit of the hysteresis width as function of the gate voltage sweeping time, revealing a time constant of $191\ min$. *d) Double exponential fit of the hysteresis width obtained from figure b revealing a fast characteristic time of* $5\ s$ *and a long one of* $42\ min$.

2.2.3 Non-volatile memory devices realization

The results of the previous section revealed the origin of hysteresis in the transfer characteristic of BP FETs. In the following, the research efforts to find a way to exploit the unavoidable presence of

such hysteresis to create practical devices are reported. Usually, the presence of trap states is detrimental to FET performance, and the hysteresis is considered a negative feature for a FET, but it is possible to show that the charge trapping can be exploited to realize memory devices. In such a way, non-volatile memory devices with good performance were realized without using an additional charge-trapping layer, but just exploiting the presence of BP and SiO_2 defects.

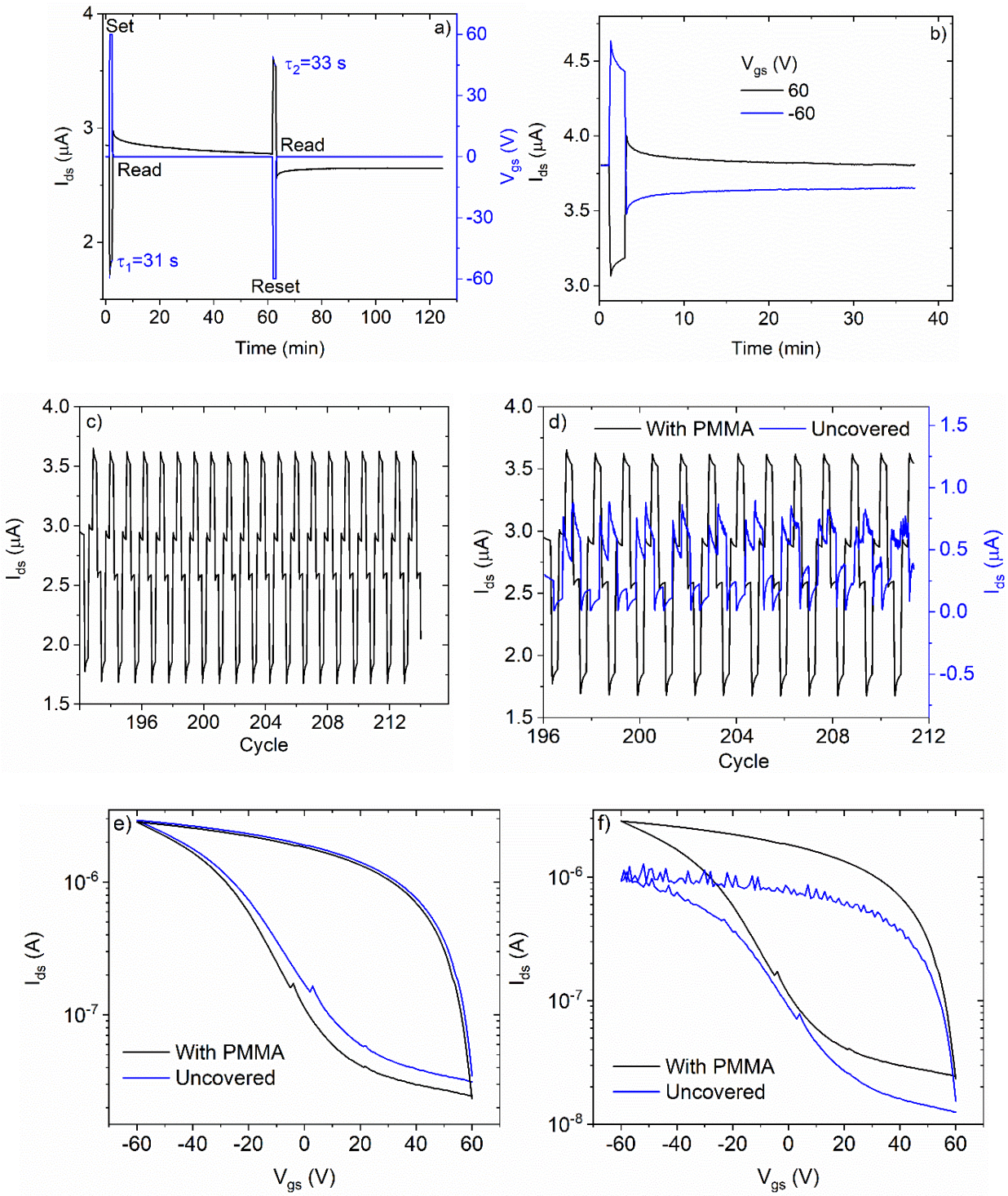


Figure 2.8 – a) Channel current (black line) recorded under gate pulses (blue line) at $\pm$ 60 V *showing single set-read-reset-read cycles of the non-volatile memory. b) Transient behaviour of the channel current after the gate pulses at* $\pm$ 60 V *revealing a retention time longer than 30 minutes. c) Repeated set-read-reset-read cycles of the memory device showing an endurance over 200 cycles. d) Repeated set-read-reset-read*

cycles measured after a month air exposure of a device covered with PMMA (black line) and an uncovered one (blue line). e) Transfer characteristics of two BP FETs, one covered with PMMA (black line) and the other exposed to air (blue line), recorded immediately after the device fabrication. f) Transfer characteristics of the same devices of e), measured after one-month exposure to air.

Figure (2.8 a) shows the transient behaviour of the device, investigated through a series of $V_{gs} = \pm 60\ V$ pulses while the I_{ds} current is monitored over time. While the gate pulse is in the high positive or negative state the channel current is not constant, but it increases/decreases in an exponential way. This is due to trapping/detrapping of charge inside the trap states. When the gate voltage is set to $0\ V$, the current tends to return to its initial value. However, the transient behaviour after a positive and a negative gate pulse shows that I_{ds} stabilizes at two different values, distinct from the initial one (Figure (2.8 b)). This separation is retained for a time longer than 30 minutes, which is comparable with the retention time observed in non-volatile BP memories with charge trapping layers[97–99]. Then, we tested the endurance of the device by continuously applying pulses of 1 min width at $V_{gs} = \pm 60\ V$. Figure (2.8 c) shows that the device response is stable after 200 cycles, consistently with similar non-volatile memories realized with other 2D materials.[119]

Finally, since the main obstacle to the realization of BP-based devices is the lack of stability in the air, several BP devices were covered with a PMMA layer. Then, endurance tests were performed on two similar devices, with and without PMMA. Initially, the devices have similar behaviour but, after exposure to air for a month, the PMMA protected device maintains its current while the unprotected device shows evident signs of current deterioration (Figure (2.8 d)). Figure (2.8 e) compares the transfer characteristics of the PMMA covered and uncovered devices immediately after the fabrication process. The similarity of the two curves confirms that encapsulation by PMMA

does not significantly alter the BP device. The transistor covered with PMMA has a slightly larger hysteresis because PMMA can contribute to charge trapping. Figure (2.8 f) shows the same transfer characteristics recorded after that both devices were left exposed to the air for a month. The device covered with PMMA does not show any signs of deterioration while the uncovered FET exhibits an evident reduction in conductivity and a much noisier current due to surface oxidation. This result confirms that PMMA encapsulation is a simple and effective method of avoiding the deterioration of air exposed BP memory FETs.

2.3 Germanium Arsenide ($GeAs$)

The third material that has been studied in this PhD project as FET channel is germanium arsenide ($GeAs$). Among the IV–V compounds, $GeAs$ has attracted attention for possible optoelectronic applications and for its high in-plane anisotropy[37,38]. $GeAs$ bulk crystalizes in a layered structure, in the space group $C2/m$, in which each Ge atom is bonded to one Ge atom and three As atoms forming distorted $As_6@Ge_2$ octahedra[130]. As described in Chapter 1 regarding TMDs, also $GeAs$ layers, terminated by As atoms, are kept together by weak van der Waals forces and show two different types of $Ge-Ge$ bonds. One type is parallel and the other one is perpendicular to the layer plane, highlighting the anisotropic nature of the $GeAs$ crystal structure, as shown in Figure (2.9 a). Similar to TMDs, the $GeAs$ bandgap changes according to the number of layers. Numerical calculations and optical bandgap measurements, indicate that germanium arsenide indirect bandgap ranges from $\sim 0.57-0.65\ eV$ for the bulk[35,36] to $1.6-2.1\ eV$ for the monolayer.[131,132] The purpose of this research was to investigate the electrical transport properties of $GeAs$ in a wide range of temperature and to evaluate its performances when used as channel of field-effect transistors. To do that, $GeAs$ back-gate field effect transistors have been fabricated using exfoliated flakes of $12\ nm$ thickness. Output and transfer characteristics were measured in a four-probe

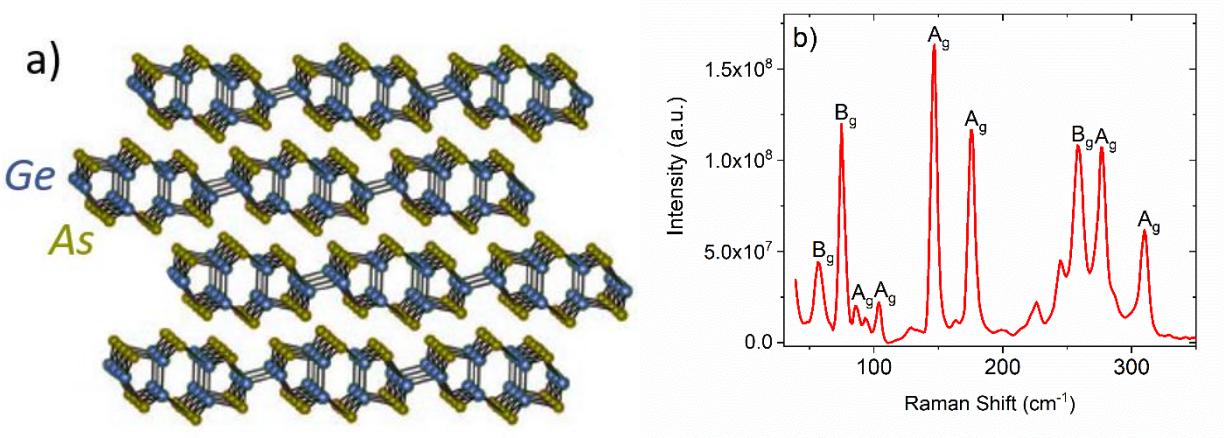
configuration highlighting the p-type nature of the $GeAs$ flakes in the vacuum. The temperature behaviour of the transistors has been investigated in a range from $20\ K$ to $280\ K$ estimating figures of merit such as the channel resistivity and the field effect mobility. The free carrier density per area, studied as a function of the temperature, showed an unexpected broad peak around $75\ K$. To explain this anomaly, a model based on the modulation of the channel thickness with the temperature has been proposed. At low temperatures, the intrinsic carrier concentration in the channel is limited and the electric field of the gate controls the whole thickness of the $GeAs$ flake. At higher temperatures, the increased carrier injection from the contacts and ionization of defects enables the formation of a 2D highly conductive channel close to the dielectric interface, which screens the gate field and confines it to the first few layers of the material. Such model was corroborated by the estimation of $\sim 0.4\ nm$ Debye screening length at room temperature. The numerical simulation of the model was compared with the experimental data obtaining an excellent agreement. To account for the temperature behaviour of the resistivity, the variable range hopping model has been used at lower temperatures and the thermally activated band-conduction mechanism at higher temperatures. At lower temperatures the $GeAs$ flake behaves like a three-dimensional system in which the main conduction mechanism is hopping among intragap states, while at higher temperatures, after the formation of the 2D channel, the conduction is dominated by thermal activation of carriers (holes) to the valence band, which leads to band-type conduction regime.

2.3.1 Mechanical exfoliation and temperature-controlled measurement setup

The same method used for the isolation of the BP, reported in the previous paragraph, was applied to exfoliate thin $GeAs$ flakes. Degenerately doped p-type silicon substrates, covered by $300\ nm$-thick SiO_2, were used as substrate and the flakes were located through optical microscopy. The

Raman spectrum of a flake (Figure 2.9 b) was measured under excitation line of 455 nm by Thermo Scientific DXR microscope and, in agreement with other studies[133], displays six Raman A_g modes at $94, 105, 147, 174, 276$ and $308\ cm^{-1}$, and three Raman B_g modes at $58, 76$ and $257\ cm^{-1}$. Atomic force microscope (AFM) was used to evaluate the flakes thickness, resulting $\sim 12\ nm$, that corresponds to about 20 layers. For this experiment the devices were shaped in a typical Hall bar structure, that allows to easily study the asymmetric electrical behaviour of the material, and intentionally oriented along one of the crystallographic axes of the material. $5\ nm\ Ni / 40\ nm\ Au$ electrodes were deposited through electron-beam evaporation as shown in Figure (2.9 c). A back-gate contact was formed covering the scratched area of the Si substrate with silver paste.

Electrical measurements were carried out in an Oxford Instrument Teslatron PT cryostat electrically connected with a semiconductor parameter analyser to perform a standard four-probe characterization of the devices (Figure (2.9 d)). All the measurements were carried out at a pressure of $\sim 10^{-5}\ mbar$ within the temperature range from $20\ K$ to $280\ K$.



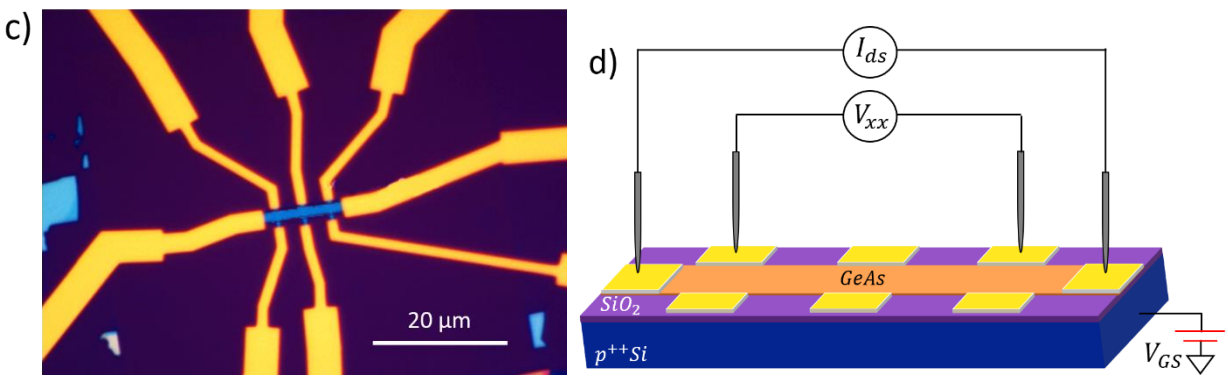


Figure 2.9 –a) Atom arrangement in $GeAs$ layers. b) Raman spectrum of a $GeAs$ flake. c) Optical image of the Hall bar device with Ni/Au electrodes. d) Four-probe measurement setup.

2.3.2 Standard four-probe transistor characterization

As explained in the previous paragraph, the standard characterization of the transistor is crucial to understand the fundamental properties of the material. Again, in order to avoid contact resistances, it was decided to carry out 4-probe measurements. The output characteristic is reported in Figure (2.10 a), revealing that the application of the gate voltage affects the overall conductance of the sample without modifying the $I_{ds} - V_{xx}$ linearity as expected for four-probe measurements that exclude the effect of the contact resistance[134–136]. The transfer characteristic was measured over a loop of the gate voltage and it is reported in Figure (2.10 b). It shows a typical p-type behaviour with a modulation that is less than one order of magnitude. The OFF-state of the transistor was not reached in the applied voltage range, which was limited to avoid the breaking of the device gate dielectric. The p-type behaviour is favoured by the low workfunction[31] of $GeAs$ ($\sim 4\ eV$) and the higher workfunction of the degenerate $p - Si$ gate ($> 5.12\ eV$) that cause the vertical band alignment shown in the inset of Figure (2.10 b). Furthermore, the Ni Fermi level (work function $5.15\ eV$) tends to align below the valence band of $GeAs$, resulting in ohmic contacts. Furthermore,

intrinsic defects such as Ge vacancies, the interaction with the SiO_2 gate dielectric and the oxidation of the topmost layers of the flake would act as p-type dopants in the material and provide intragap states[30,31]. Hole injection from the metal leads makes the area below and near the contacts more doped than the rest of the long channel, thereby originating an energy barrier E_A, which can be modulated by the gate, as shown in Figures (2.10 c) and (2.10 d).[137]

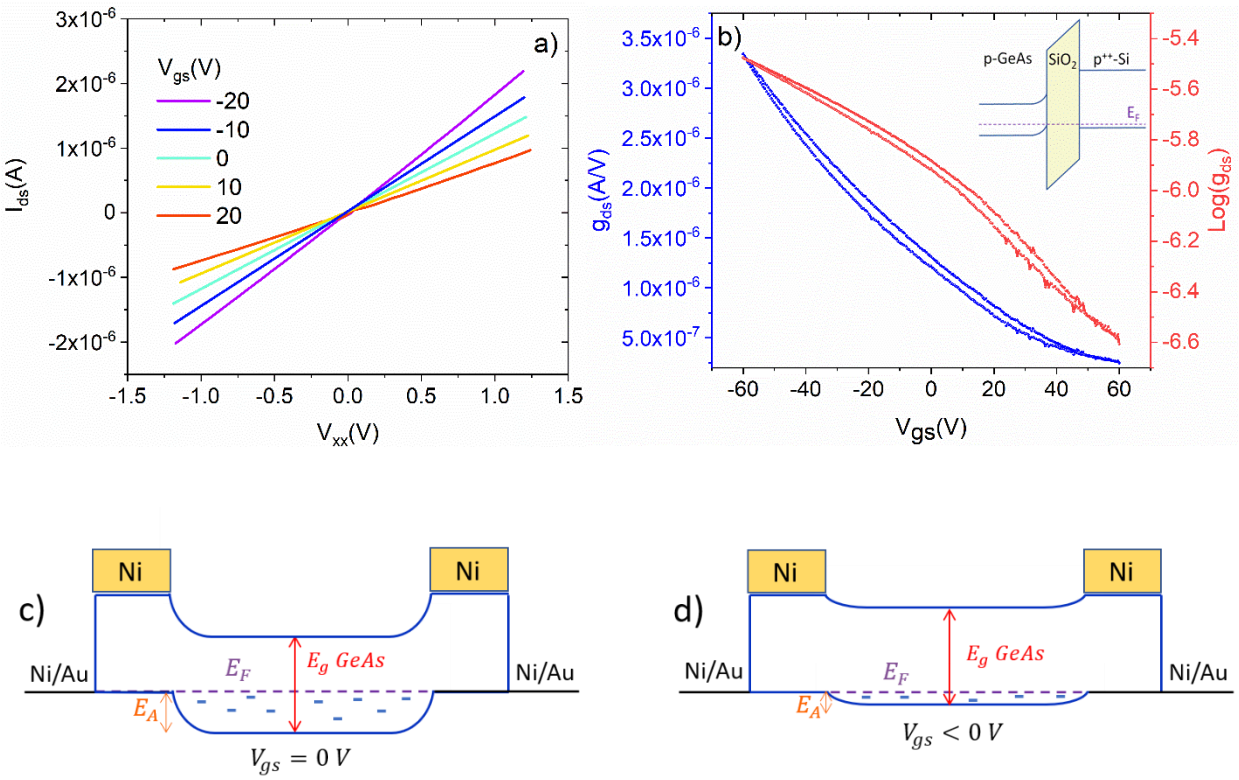


Figure 2.10 – a) Output characteristic recorded in four-probe configuration with V_{gs} bias between $-20\ V$ and $20\ V$. b) Transfer characteristic recorded in four-probe configuration showed both on linear and logarithmic scale. The inset show the band diagram in the vertical direction at zero bias clarifying that the device is a normally-on transistor. c) and d) Band diagram along the channel (horizontal) direction showing alignment between Ni/Au contacts and $GeAs$ at $V_{gs} = 0\ V$ and $V_{gs} < 0\ V$, respectively. The small blue dashes represent (mostly empty) trap states for holes. The contact region is more doped than the channel (not on scale) thus originating an energy barrier E_A, which is modulated by the gate.

Differently from typical few-layer TMD-based transistors[138–142] and from what has been reported for $PtSe_2$ and BP in the previous paragraphs, the transfer characteristic exhibits negligible hysteresis indicating limited charge trapping during a gate voltage loop.

2.3.3 Electrical conduction temperature dependence

As anticipated, the main purpose of this work was to study how temperature influenced the electrical transport properties of $GeAs$. To do that, output and transfer characteristics were measured every $20\ K$ in the $20 - \ 280\ K$ temperature range, as reported in Figure (2.11 a) and (2.11 b). It has been found that lowering temperature leads to a decrease in the current and the conductance without any other apparent change in the behaviour of the device. From the linear fit of the $I_{ds} - V_{xx}$ curves, recorded at $V_{gs} = -20V$, the resistivity ρ of the sample was estimated as a function of the temperature ($\rho = \frac{RW}{L}$, where R is the resistance evaluated from the fit and $L = 6\ \mu m$ and $W = 2.7\ \mu m$ are the channel length and width, respectively). Figure (2.11 c) shows a typical semiconducting behaviour where ρ decreases for increasing temperature.

Using the transfer characteristics, and exploiting Equations (1.4) and (1.8) it was possible to obtain the field-effect mobility μ_{FE}, where it was considered $C_{ox} = \frac{\epsilon_0 \cdot \epsilon_{SiO_2}}{t_{SiO_2}} = 1.15 \cdot 10^{-8}\ \frac{F}{cm^2}$ and t_{SiO_2}= $300\ nm$. In order to have a fair comparison with the values of ρ obtained from $g_{ds} - V_{xx}$ curves at $V_{gs} = -20\ V$, the linear fit of the transfer characteristics has been performed in a small interval around $V_{gs} = -20\ V$. Repeating this procedure for the transfer collected at each temperature the μ_{FE} as function of the temperature T plot was obtained, as reported in Figure (2.3 c). The quadratic dependence, $\mu_{FE} \sim T^2$, reveals a mobility dominated by Coulomb scattering due to ionized impurities[143]. Indeed, it is well known that the mobility is affected by two competitive mechanisms, i.e. the ionized impurity scattering and the phonon scattering[143]. The first mechanism dominates

at lower temperatures and yields an increasing mobility with raising temperature, while phonon scattering becomes the prevailing mechanism at higher temperatures and causes a decreasing mobility. As already mentioned, charged impurities leading to Coulomb scattering and increasing μ_{FE} are due to intrinsic defects of the $GeAs$, SiO_2 interface states and oxidation of the topmost layers of the flake.

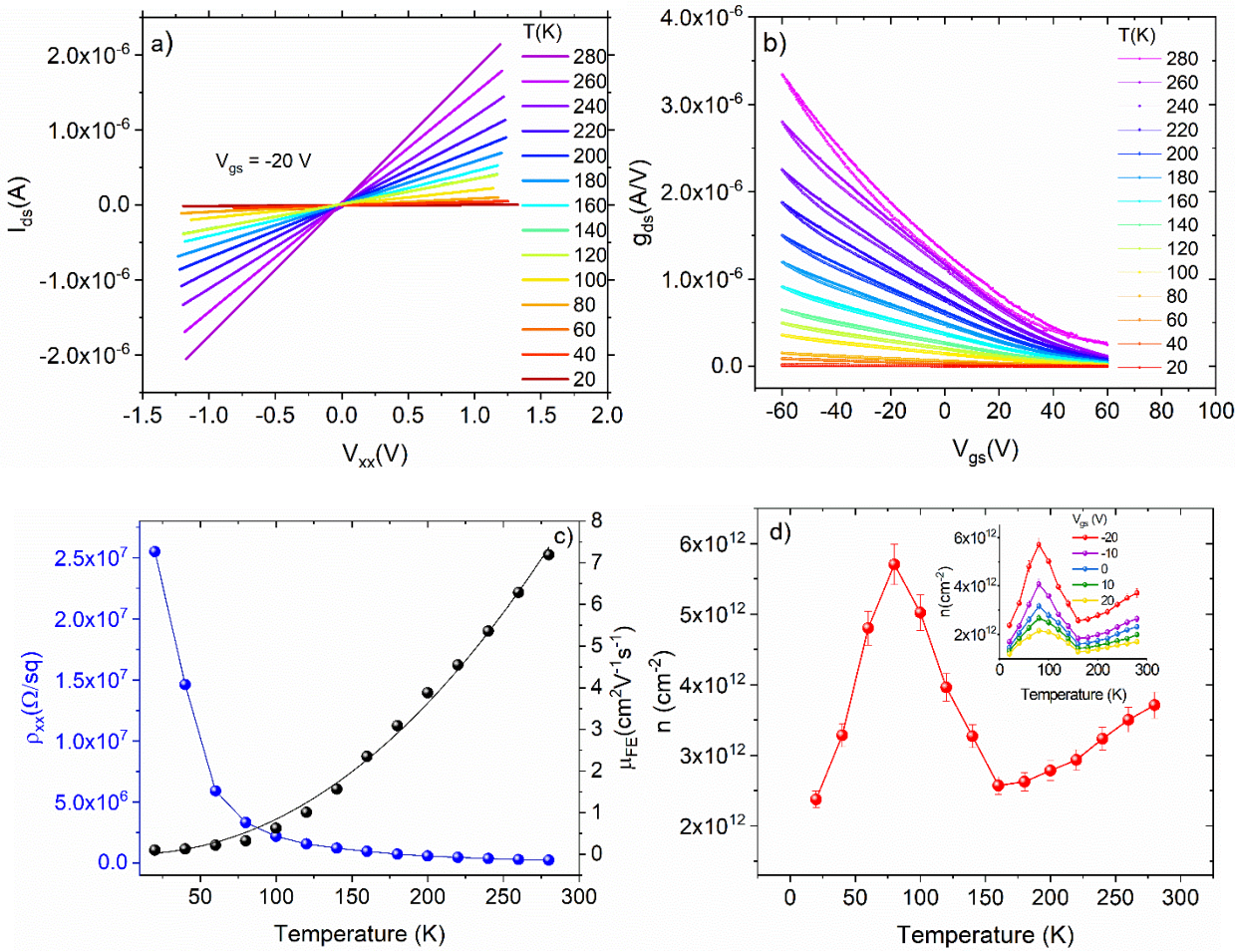


Figure 2.11 – a) I_{ds} versus V_{xx} curves at different temperatures. b) Transfer characteristics recorded for a loop of the voltage bias at different temperatures. c) Channel resistivity (blue dots) and field effect mobility (black dots) as function of the temperature. The superposed red line is the quadratic fit. d) Carrier density n versus temperature at $V_{GS} = -20\ V$. The inset shows n as function of the temperature at several gate biases. The uncertainties are obtained from the standard error propagation.

2.3.4 Carrier density and effective conduction channel

Having computed $\mu_{FE}(T)$ and $\rho(T)$ at each of the considered temperatures, the carrier density per unit area n (in cm^{-2}) as a function of temperature was evaluated from Equation (2.1). Figure (2.11 d) shows that $n(T)$ exhibits an unexpected and pronounced peak at $T{\sim}75\ K$, followed by a smoother increase for $T > 150\ K$. Such behaviour is quite different from that typical of doped three-dimensional semiconductors [143]. Indeed, usually, an initial rapid increase due to the ionization of dopant atoms by thermal energy (freeze-out region, up to ~150 K for medium-doped Si) is followed by a plateau over a wide temperature range when complete ionization is reached (extrinsic region, ~150-500 K for medium-doped Si) and would finally evolve in an exponential increase at higher temperatures due to intrinsic generation of electron-hole pairs (intrinsic region).

In this case, some different phenomenon occurs, and for this reason a model that considers a temperature dependent thickness of the channel in which most of the conduction occurs has been proposed. The 2D carrier density per unit area can be expressed as $n(T) = \varphi(T)\tau(T)$ where φ is the carrier density per unit volume in cm^{-3} and τ is the thickness of the conducting channel. The current in the $GeAs$ flake is due to carriers injected from the Ni contacts that overcome the E_A barrier, as shown in Figure (2.10 c) and (2.10 d). Therefore, $\varphi(T)$ in the region between the inner contacts (Figure (2.12 a) and (2.12 b)) can be expressed as[144]:

$$\varphi(T) = A \exp\left[-\frac{E_A}{kT}\right] \qquad (2.\ 3)$$

where k is the Boltzmann constant, E_A is the barrier between contact and channel region, and A is a proportionality constant that can be considered as a fitting parameter of the model. At low temperature ($< 80\ K$), there is a limited amount of carriers as well as high intralayer resistance that

suppresses the vertical transport with respect to the in-plane one[137,145]. In this regime, conduction occurs mainly through the layers in closer contact with the metal leads (especially the topmost ones) and the gate electric field controls the entire flake thickness, as shown in Figure (2.12 a). With raising temperature, defect ionization and injection from the contacts increase. The new available carriers, pushed by the applied gate voltage and the favourable vertical band bending (see inset of Figure (2.10 b)) toward the interface with the gate dielectric, form a 2D channel, which becomes more and more conductive with the rising temperature. This channel now screens the gate field, and any variation of the gate voltage affects mainly the bottommost layers of the flake. In this regime, the conduction is dominated by few atomic $GeAs$ layers closer to the gate, i.e. the effective conducting thickness $\tau(T)$ controlled by the gate is reduced, as shown in Figure (2.12 b).

To corroborate this model, $n(T)$ was measured at various gate biases, shown in the inset of Figure (2.11 d). Indeed, the 2D channel at the interfacial region between the gate dielectric and the flake is hampered at positive gate voltages by the opposing gate field. Going to positive gate voltages, the 2D conductive channel is gradually suppressed and so is the carrier density n and its peak at $\sim 75\ K$.

According to the model, with an appropriate choice of $\varphi(T)$ and $\tau(T)$, $n(T)$ was computed and an excellent agreement with the experimental data was obtained, as shown in Figure (2.12 c), where $n(T)$ at $V_{gs} = -20\ V$ (continuous blue line) as well as at $V_{gs} = 20\ V$ (dashed black line) are displayed. The slight deviation below $50\ K$ could be caused by additional conduction mechanisms occurring at low temperature (such as hopping, as it will be discussed later). The carrier density per volume $\varphi(T)$, given by Equation (2.3), is shown by the red lines of Figure (2.12 d), with E_A obtained as fitting parameter and displayed as a function of V_{gs} in the inset of Figure (2.12 c). For $\tau(T)$, a step-like function was used, $\tau(T) = \frac{A}{1+\exp(B*T)} + C$, represented by the blue curves shown in Figure (2.12 d), in which A is the initial thickness of the whole flake, i.e. $\sim 12\ nm$, C is the thickness of a single

$GeAs$ layer ($0.6\ nm$), and B is a fitting parameter used to simulate a smooth transition in the $70 - 150\ K$ range.

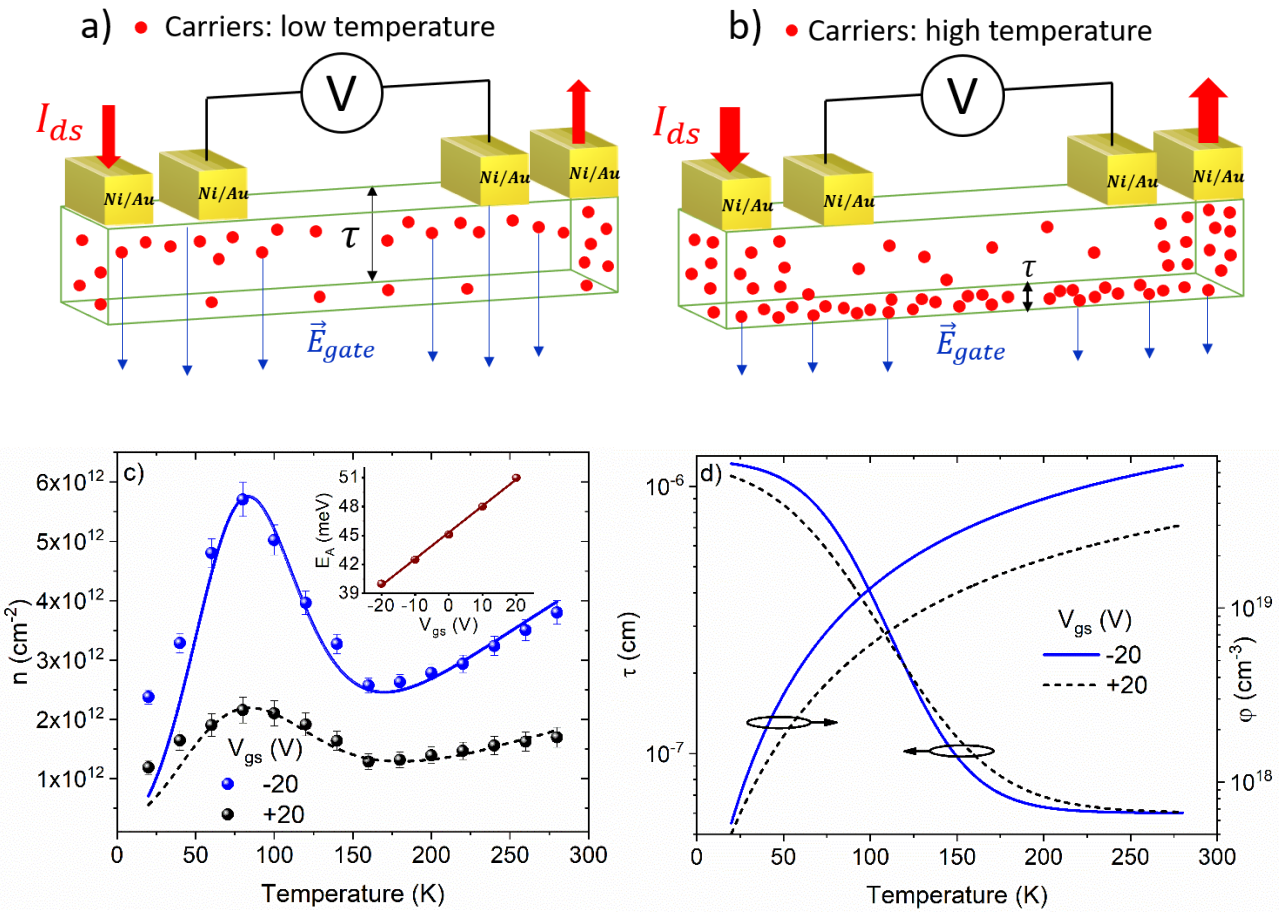


Figure 2.12 – a) Schematic of the GeAs flake at low temperatures with low carrier density and the electric field of the gate at $V_{GS} < 0\ V$ (blue arrows) controlling the entire thickness. b) Schematic of the GeAs flake at high temperatures with the formation of a highly conductive channel confined to a thin interfacial layer, which screens the electric field of the gate (blue arrows). The drawings are not on scale. c) Numerical simulation of the 2D carrier density as function of the temperature for $V_{gs} = \mp 20\ V$ (fitting lines superposed to the experimental data). The insect shows E_a as function of the applied gate potential. d) Effective thickness of the channel (blue lines) and three-dimensional carrier density (black lines) as function of the temperature for $V_{gs} = \mp 20\ V$

The model is further corroborated by the estimation of the Debye screening length $L_D = \sqrt{\frac{\epsilon\epsilon_0 kT}{q^2\varphi}}$, that gives the length over which the electric field strength drops by a factor $1/e$ (here $\epsilon = 8$ is the dielectric constant at room temperature of the material[146]). From the experimental data, $L_D \sim 0.4\ nm$ was estimated at room temperature, confirming that the gate electric field is substantially screened in the layer closer to the gate.

2.3.5 Variable range hopping and band conduction

In the last section of this paragraph, the conduction mechanisms at different temperatures are studied, revealing a good agreement with the model proposed previously.

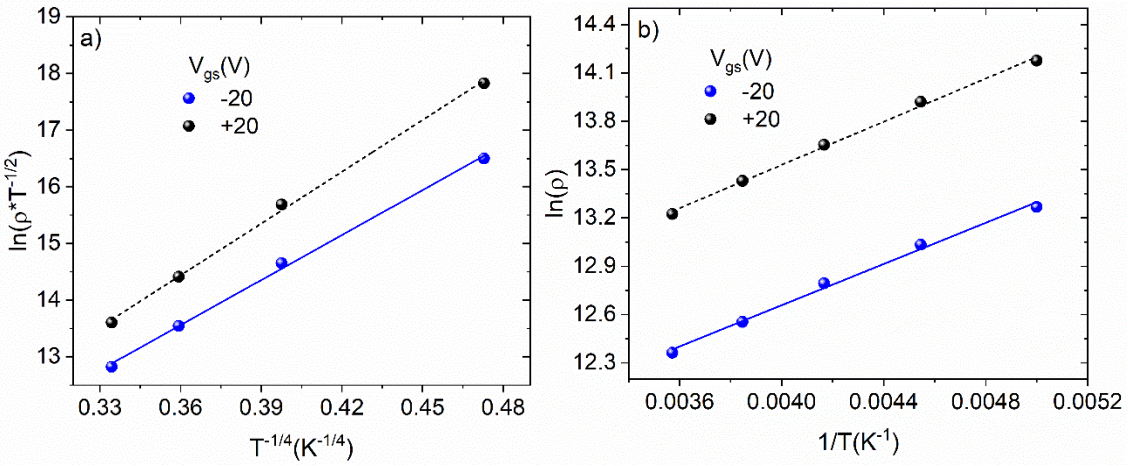


Figure 2.13 – a) Experimental data and linear fit of $ln\ (\rho * T^{-1/2})$ at $V_{gs} = \mp 20\ V$ as function of $T^{-\frac{1}{4}}$ at low temperature indicating the three-dimensional nature of the investigated system. b) Experimental data and linear fit of $ln\ (\rho)$) at $V_{gs} = \mp 20\ V$ as function of T^{-1} at high temperature indicating the band conduction regime of the investigated system.

To obtain this result the resistivity ρ as function of T has been investigated. The best fitting of the experimental data at low temperature is obtained using the variable range hopping conduction

(VRH). VRH is usually observed at low temperature in systems with defects and has been reported for several two-dimensional materials[147,148]. According to VRH theory the relation between ρ and T can be expressed as[149]:

$$\rho(T) = \rho_0 \exp\left(\frac{T_0}{T}\right)^{\frac{1}{n+1}} \qquad (2.4)$$

where ρ_0 depends on the square root of T, T_0 is a constant and n indicates the dimensionality of the system[150]. Figure (2.13 a) shows $\ln(\rho * T^{-\frac{1}{2}})$ as function of $T^{-\frac{1}{4}}$ in the range $20\ K$ to $80\ K$. The linearity demonstrates that the conduction is bulk type (3D) for $T < 80\ K$, i.e. it occurs through the entire flake constituted of ~ 20 atomic layers, as assumed in the proposed model. For $T > 180\ K$, ρ shows an exponential increase with the inverse of temperature, as shown in Figure (2.5 b). This indicates that the thermal excitation of carriers (holes) to the valence band leads to a band conduction regime, $\rho \propto \exp\left(\frac{E_A}{kT}\right)$, as expected after the formation of a highly conductive 2D channel in the $GeAs$ transitor.

2.4 A practical issue: the realization of ohmic contacts

To conclude this chapter concerning the use of 2D materials as FETs channel, one of the main problems that must be faced both during the fabrication and the electrical characterization of the devices is reported, i.e. the interaction between the semiconductive material and the metal electrode. This is one of the most underestimated aspects in evaluating the electrical properties of 2D semiconductors even if it deeply affects the devices' performance. As matter of fact, it cannot be taken for granted, and it is actually very rare, that the junction between a metal and a semiconductor gives life to an ohmic contact, that can be described as a low-resistance junction

providing current conduction in both directions. Indeed, in the most general case, when a metal is placed on a semiconductor a so called Schottky junction is formed. It is a rectifying junction in which a potential barrier, that in the ideal case is given by the difference between the metal workfunction and the semiconductor electron affinity, limits the current flow through the device. Although the physics of Schottky junctions is well known, its impact on the current-voltage characteristics of 2D materials has been frequently neglected or misunderstood. Furthermore, in typical electronic devices, there are at least two metal-semiconductor junctions (such as the junctions between the source and drain electrodes and the 2D materials that are formed in FETs, as described in Chapter 1), which complicates the physics behind the electrical transport processes. A simple and effective method to derive fundamental parameters, such as the Schottky barrier (SB) height and the contact resistance for 2D materials presenting two Schottky junctions had never been fully developed. For this reason, during this PhD project, a research study has been conducted to elaborate a single equation to describe the current-voltage characteristics of two-terminal semiconductor devices with Schottky contacts. The aim was to obtain a model that could be used to directly estimate the Schottky barrier height and the junction ideality factor and that could be applied it to perfectly reproduce the experimental current-voltage characteristics of 2D devices.

The starting point was the consideration that current-voltage measurements have resulted to be the most efficient way for evaluating the quality of metal contacts and for the extraction of fundamental parameters such as the SB height and the contact resistance. To study the I-V characteristic of two terminal devices with SBs, the classic equation of the Schottky diode is often used. This equation considers that charge carriers cross an energy barrier by thermionic emission. In this approach, it is implicitly assumed that there is a Schottky junction at the forced contact while the other contact is ohmic. Moreover, in such an approach, only the dominant current, occurring

either at positive or negative voltages, is commonly used to evaluate the barrier parameters. Nevertheless, in most devices both contacts have a rectifying nature and the simplistic assumption of a single SB leads to the wrong results, such as very large ideality factors ($n \gg 1$) or unrealistic SB height and Richardson constant.

Oldham and Milnes highlighted the need to consider two barriers to describe the electric conduction based on thermionic emission in n-n heterojunctions.[151] Then, Ramirez et al.[152] and Nagano et al.[153] applied the model to study the electric transport in SnO_2 nanowires and in C_{60} films with Au contacts. In both works, the authors did not consider that barriers with different heights could form at the contacts. Such a possibility might easily occur as the SB height is related to interfacial chemistry and local defects. Nouchi proposed a single equation[154] to study the Schottky barrier of a device formed by a metal-semiconductor junction, in which a second electrode necessary to perform the electrical measurement forms a metal-semiconductor-metal structure. This model does not consider the possibility that the two Schottky barriers formed with the contacts may have different ideality factors and requires the use of the first and second derivative of the I-V characteristic of the device that can limit its applicability. A model with two different barriers at the contacts was proposed by Chiquito et al. who limited their study to the analysis of metal/SnO_2/metal devices.[155] A model based on SBs with different heights was used by Di Bartolomeo et al. to account for the rectifying electrical characteristics observed in field effect transistors with ultrathin transition-metal dichalcogenide channel[134,156] or in metal/insulator/semiconductor structures.[157]

In the follow, it is reported the derivation and the application of a simple model, elaborated during this PhD project, used to describe the conduction in a two-terminal device in which two rectifying contacts are present. The model allows to obtain both SB heights simultaneously. First, the model

is used to make numerical simulations of the I-V curves for different combination of junction parameters such as barrier height, area and ideality factor.[143] Then, the model is tested fitting the symmetric or asymmetric I-V curves of two-terminal nanodevices made of MoS_2 or WSe_2 nanosheets and WS_2 nanotubes. Although demonstrated for nanostructured semiconductors, the model can be applied to any devices with two SBs.

2.4.1 Ideal Schottky junction theory

In this first section, the classical theory of Schottky junctions is presented. The SB height is defined as:

$$\phi_{SB-n} = \phi_m - \chi_s \qquad \phi_{SB-p} = E_g + \chi_s - \phi_m \tag{2. 5}$$

where ϕ_{SB-n} and ϕ_{SB-p} are the SB heights for electron and hole injection, respectively, ϕ_m is the metal work function, χ_s is the semiconductor electron affinity and E_g is the bandgap of the semiconductor, as shown in Figure (2.14 a). According to Equations (2.5), a low work function metal with the Fermi level close or above the bottom of the conduction band of the semiconducting material facilitates electron injection whereas a high work function metal with the Fermi level close or below the valence band of the material favours hole injection. However, Equations (2.5) give only qualitative indications of the SB heights and are rarely in quantitative agreement with the experimental data. This is mainly because the metal Fermi level can be pinned at a semiconductor interface state, ϕ_{IS}, if a high-density of interface states is formed within the semiconductor bandgap during the fabrication process, as shown in Figure (2.14 b). In this case, the equation for ϕ_{SB-n} is replaced by:[158]

$$\phi_{SB-n} = (S \cdot \phi_m - \chi_s) + (1 - S)\phi_{IS} \qquad (2.6)$$

where $S = \frac{\partial \phi_{SB-n}}{\partial \phi_M}$ is the Schottky pinning factor (a similar expression is used for ϕ_{SB-p}). If $S = 0$, the pinning is maximum, the SB turns out to be independent of the metal work function and the so-called Bardeen limit is reached. Conversely, when $S = 1$, the Bardeen limit converges to the Schottky limit, represented by Equation (2.5).

Since the evaluation of the Schottky pinning factor and the semiconductor interface state energy, ϕ_{IS}, is complicated by variability of the fabrication process, the extraction of the SB height by means of electrical measurements is one of the most efficient techniques of investigation.

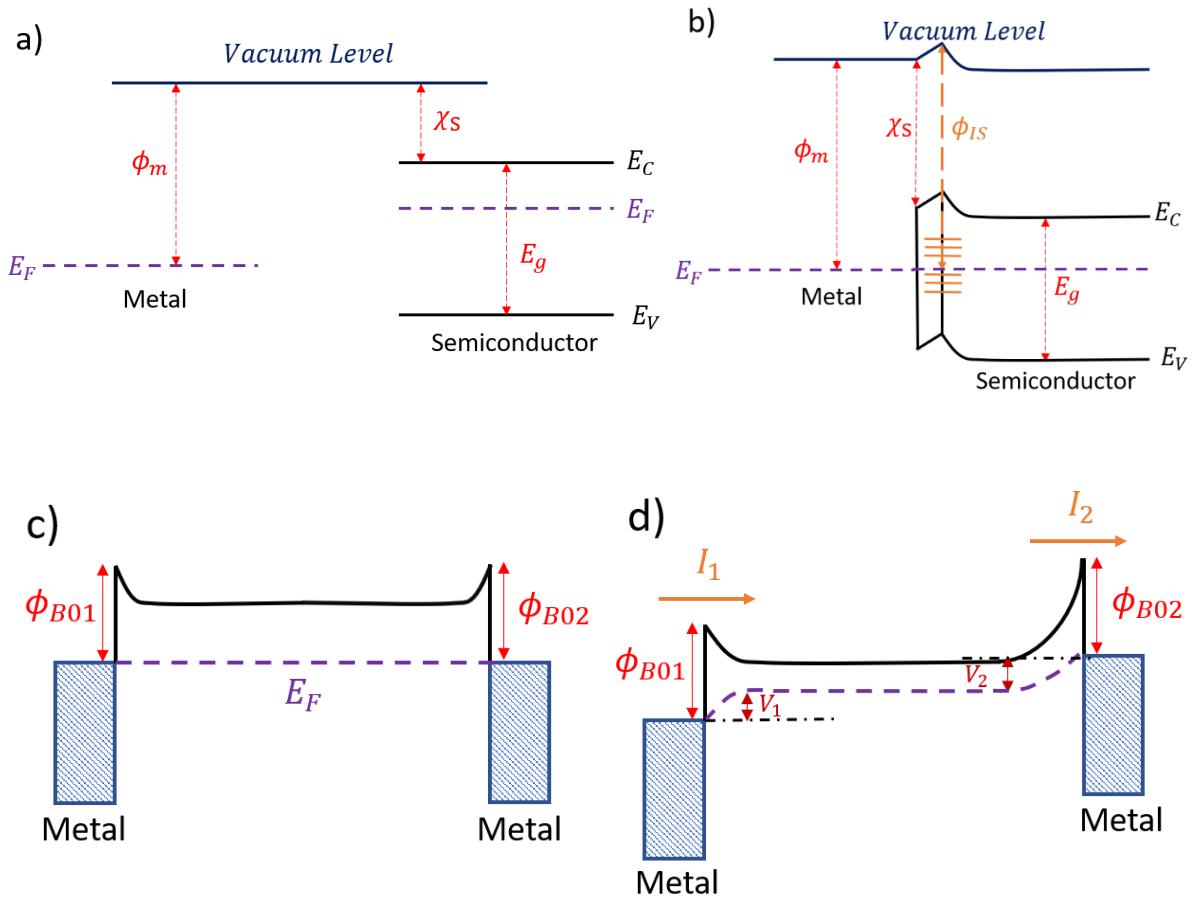


Figure 2.14 – a) Typical band diagram of a metal and an n-type semiconductor before they are brought into contact. b) Band diagram of a metal in contact with a semiconductor where a high-density of interface states is present. The Fermi level is pinned at the semiconductor interface state, ϕ_{IS}, and the SB height is independent of the metal work function. c) Energy diagram of a semiconductor with two Schottky junctions at the contacts for unbiased condition. d) Energy diagram of the same device when an external potential V is applied to the left contact. I_1 and I_2 represent the current through the two barriers, while V_1 and V_2 are the potential drops at the junctions ($V = V_1 + V_2$). The dashed violet line represents the quasi-Fermi level.

Usually, when a semiconductor material is measured in standard two-probe configuration, the grounded contact is assumed ohmic while the other contact can form a Schottky junction regulated by a potential barrier. This assumption is unrealistic because Schottky junctions can be formed at both contacts. Hence, to approach the problem in a more general way, the presence of SBs at both metal contacts with the semiconductor is assumed.

If no external potential is applied, the band diagram of the device with two-Schottky contacts is shown in Figure (2.14 c) in which the two barriers are designated as ϕ_{B01} and ϕ_{B02}, respectively. When a positive potential V (bias) is applied to the left contact, the bands are bent as shown in Figure (2.14 d). $V_{1,2}$ and $I_{1,2}$ indicate the potential drop and the currents at the contacts 1 and 2, respectively.

2.4.2 Double Schottky barrier devices

In this section, the theory set out above for a single barrier is extended to the case in which a double Schottky junction is present. The semiconductor with SBs at both contacts can be modelled with two back-to-back Schottky diodes separated by a series resistance. When a sufficiently high external voltage is applied, whether positive or negative, one Schottky junction is forward-biased while the

other one is reverse-biased. The reverse saturation current of the reverse-biased diode always limits the current. Based on thermionic emission, the current at the two contacts can be written as:[143]

$$I_1 = I_{s1}\left[e^{\frac{qV_1}{kT}} - 1\right] \quad (2.\ 7)$$

$$I_2 = -I_{s2}\left[e^{-\frac{qV_2}{kT}} - 1\right] \quad (2.\ 8)$$

Where

$$I_{s1,s2} = S_{1,2}\, A^* T^2\, exp\left(-\frac{\phi_{B01,2}}{kT}\right) \quad (2.\ 9)$$

are the reverse saturation currents, A^* is the Richardson constant, T is the temperature, k is the Boltzmann constant and $S_{1,2}$ are the areas of the junctions. For the continuity of the current the total current I_T can be expressed as $I_T = I_1 = I_2$, while the applied potential is $V = V_1 + V_2$. Starting from $I_T = I_1$ it is possible to write:

$$I_T = I_{s1}\left[e^{\frac{qV_1}{kT}} - 1\right] \quad (2.\ 10)$$

And substituting $V_1 = V - V_2$:

$$I_T = I_{s1}\left[e^{\frac{qV}{kT}} e^{-\frac{qV_2}{kT}} - 1\right] \quad (2.\ 11)$$

Using Equation (2.8), the term $e^{-\frac{qV_2}{kT}}$ can be expressed as

$$e^{-\frac{qV_2}{kT}} = 1 - \frac{I_2}{I_{s2}} = 1 - \frac{I_T}{I_{s2}} \qquad (2.12)$$

since $I_2 = I_T$. Then, substituting Equation (2.12) into Equation (2.11), it results:

$$I_T = I_{s1}\left[e^{\frac{qV}{kT}}\left(1 - \frac{I_T}{I_{s2}}\right) - 1\right] \qquad (2.13)$$

Executing all the products and isolating I_T we get:

$$I_T = \frac{I_{s1}\left(e^{\frac{qV}{kT}} - 1\right)}{1 + \frac{I_{s1}}{I_{s2}}e^{\frac{qV}{kT}}} \qquad (2.14)$$

Finally, multiplying numerator and denominator by $2I_{s2}e^{-\frac{qV}{2kT}}$, it is possible to obtain

$$I_T = \frac{2I_{s1}I_{s2}sinh\left(\frac{qV}{2kT}\right)}{(I_{s1}e^{\frac{qV}{2kT}} + I_{s2}e^{-\frac{qV}{2kT}})} \qquad (2.15)$$

As it should be expected, Equation (2.15) is transformed into the single SB equation for a configuration with a SB and an ohmic contact, for instance, when $\phi_{B01} \neq \phi_{B02} = 0$. This can be immediately understood considering, for example, that when $\phi_{B02} = 0$ and $S_1 \approx S_2$, it results that

$$I_{s1}e^{\frac{qV}{2kT}} = S_1 A^* T^2 e^{-\frac{\phi_{B01,2}}{kT}} e^{\frac{qV}{2kT}} < I_{s2}e^{-\frac{qV}{2kT}} = S_2 A^* T^2 e^{-\frac{qV}{2kT}} \quad (2.16)$$

for the low voltages typical of the forward biased Schottky diode ($V < \phi_{B01}$). Therefore, $I_{s1}e^{\frac{qV}{2kT}}$ can be neglected in the denominator of Equation (2.15), that reduces to the single SB equation:

$$I_T \approx \frac{2I_{s1}I_{s2}sinh\left(\frac{qV}{2kT}\right)}{I_{s2}e^{-\frac{qV}{2kT}}} = I_{s1}\left(e^{\frac{qV}{kT}} - 1\right) \quad (2.17)$$

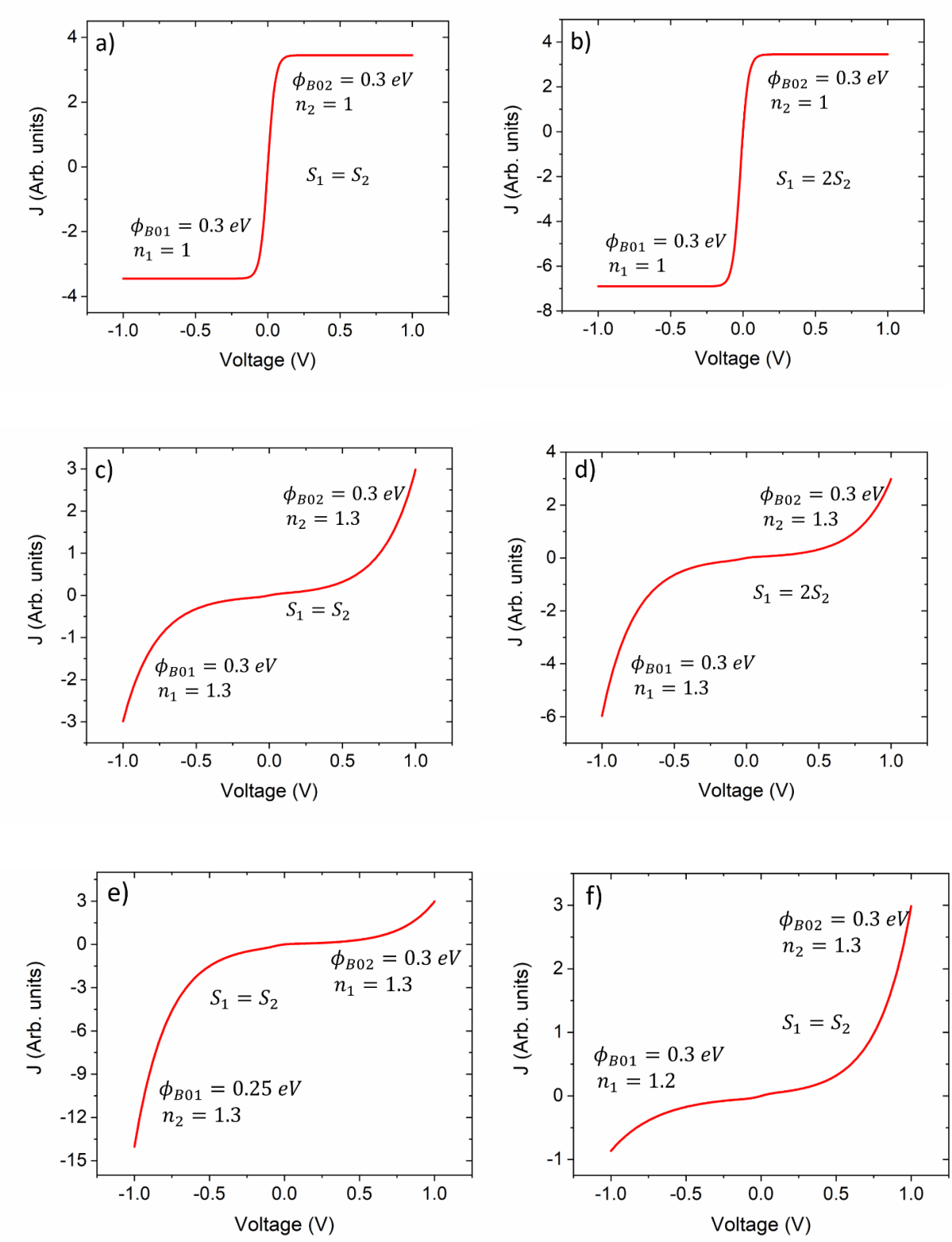
The presence of two equally rectifying junctions is rarely found, especially in small-size devices, where there can be various effects that introduce deviation from the thermionic emission, taken into account by introducing an ideality factor n in the exponential term of Equation (2.7) and Equation (2.8). Deviation from the ideality is caused by defects, inadvertent oxide layers and image-force lowering that make the SB height dependent on the applied external voltage. In such a case, the effective SBs $\phi_{B1,B2}(V)$ in Equation (2.9) can be written as[143,159]:

$$\phi_{B1,B2}(V) = \phi_{B01,B02} \pm eV_{1,2}\left(1 - \frac{1}{n_{1,2}}\right) \quad (2.18)$$

Where $\phi_{B01,B02}$ are the ideal SBs at zero bias, V_1 and V_2 are the voltage drops at the junctions and $n_{1,2}$ are the ideality factors defined as $\frac{1}{n_{1,2}} = 1 \pm \frac{\partial \phi_{B1,B2}}{e\partial V_{1,2}}$.

2.4.2 Current-voltage characteristic simulations

Having obtained a single equation to describe the relationship between voltage and current in devices with double SB, it is possible to carry out a first test of the model by carrying out a series of numerical simulations. Equation (2.15) has been used to obtain I-V curve for two junctions with the same reverse saturation current and equal barrier height, at the temperature of 300 K, as shown in Figure (2.15 a). The current saturates at the limit value set by the reverse saturation current of the reverse-biased junction for both positive and negative voltages. SB height as well as junction area are responsible for reverse saturation current value, as shown in Figure (2.15 b). Indeed, imposing $S_1 = 2S_2$, two saturation currents that are one the double of the other are obtained, yielding an asymmetric I-V characteristic.


a)
$\phi_{B02} = 0.3\ eV$
$n_2 = 1$
$S_1 = S_2$
$\phi_{B01} = 0.3\ eV$
$n_1 = 1$
b)
$\phi_{B02} = 0.3\ eV$
$n_2 = 1$
$S_1 = 2S_2$
$\phi_{B01} = 0.3\ eV$
$n_1 = 1$
c)
$\phi_{B02} = 0.3\ eV$
$n_2 = 1.3$
$S_1 = S_2$
$\phi_{B01} = 0.3\ eV$
$n_1 = 1.3$
d)
$\phi_{B02} = 0.3\ eV$
$n_2 = 1.3$
$S_1 = 2S_2$
$\phi_{B01} = 0.3\ eV$
$n_1 = 1.3$
e)
$\phi_{B02} = 0.3\ eV$
$n_1 = 1.3$
$S_1 = S_2$
$\phi_{B01} = 0.25\ eV$
$n_2 = 1.3$
f)
$\phi_{B02} = 0.3\ eV$
$n_2 = 1.3$
$S_1 = S_2$
$\phi_{B01} = 0.3\ eV$
$n_1 = 1.2$
J (Arb. units)
Voltage (V)

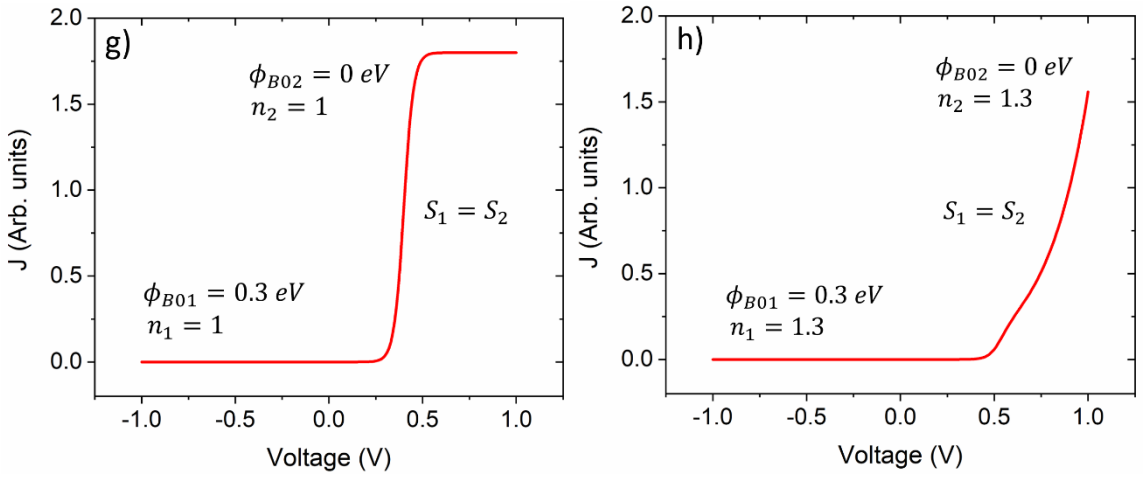


Figure 2.15 – a-h) Simulation of Equation (2.15) describing the current in two back-to-back Schottky junctions. a) I-V characteristic for contacts with the same barrier height, $\phi_{B01} = \phi_{B02} = 0.3\ eV$, the same junction area $S_1 = S_2$ and perfect ideality ($n = 1$). The current saturates to the reverse saturation current of the reverse-biased diode. b) I-V characteristic for $\phi_{B01} = \phi_{B02} = 0.3\ eV$, perfect ideality ($n = 1$), and $S_1 = 2S_2$; the saturated currents are $J_{S2} = 2J_{S1}$. c) I-V characteristic for $\phi_{B01} = \phi_{B02} = 0.3\ eV$, areas $S_1 = S_2$ and ideality factors $n_1 = n_2 = 1.3$. The ideality factor is due to the image force barrier lowering. The current does not saturate because the reverse biased diode is affected by image force barrier lowering. d) I-V characteristic for $\phi_{B01} = \phi_{B02} = 0.3\ eV$, areas $S_1 = 2S_2$ and ideality factors $n_1 = n_2 = 1.3$. We observe that the current is lower when limited by the narrower junction. e) II-V characteristic for $\phi_{B01} = 0.25\ eV$, $\phi_{B02} = 0.3\ eV$, areas $S_1 = S_2$ and ideality factors $n_1 = n_2 = 1.3$. The current results more limited at positive voltage because it is strongly limited by the higher ϕ_{B02} barrier. f) I-V characteristic for $\phi_{B01} = \phi_{B02} = 0.3\ eV$, areas $S_1 = S_2$ and ideality factor $n_1 = 1.2$ and $n_2 = 1.3$. The current is limited at negative voltage because of the higher blocking effect of ϕ_{B01}, that is closer to an ideal barrier. g) I-V characteristic for $\phi_{B01} \neq \phi_{B02} = 0\ eV$, areas $S_1 = S_2$ and perfect ideality ($n_1 = n_2 = 1$). The current of a single ideal Schottky barrier is obtained at low forward bias ($V < \phi_{B01}$). h) I-V characteristic for $\phi_{B01} \neq \phi_{B02} = 0\ eV$, areas $S_1 = S_2$ and $n_1 = n_2 = 1.3$. The negative current is still very low, but the slope of the I-V curve is voltage dependent.

Now, considering a slight deviation from the ideal case, $\phi_{B1,B2}(V)$ from Equation (2.18) has been substituted in Equation (2.15), as shown in Figures (2.15 c-f). In these plots, the simplifying assumption that $V_1 = V_2 = \frac{V}{2}$ has been made.

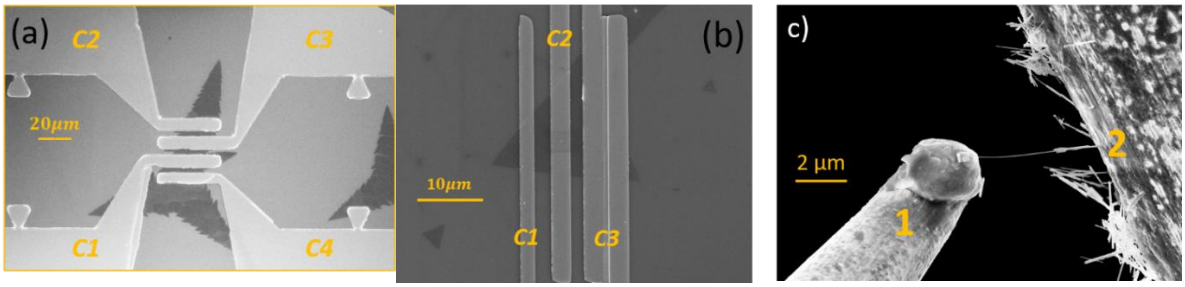
Figure (2.15 c), in particular, shows that despite the reverse-bias of one of the two junctions, the current does not saturate at positive or negative bias due to the dependence of the barrier on the applied voltage. Such behaviour is much more similar to what is usually observed in practical devices. Furthermore, considering different junction areas, the current can increase with different trends, as shown in Figure (2.15 d). In particular, the current is more limited by the junction with the narrower area. Figures (2.15 e) and (2.15 f) show the I-V curves from Equation (2.15) with different SB heights and ideality factors. In Figure (2.15 e) the current is lower at positive voltage because the current is limited by the higher ϕ_{B02} barrier (in contrast, at negative voltage the current is limited by the lower ϕ_{B01} barrier). Figure (2.15 f) shows the current behaviour in a device where the two Schottky junctions have the same barrier heights but different ideality factors. In this case, the current is lower when is limited by the junction with the lower ideality factor, i.e by the barrier closer to the ideal SB.

Figure (2.15 g) and Figure (2.15 h) show I-V curves given by Equation (2.15) setting $\phi_{B01} \neq \phi_{B02} = 0$. The classic current behaviour for a single Schottky barrier is obtained for both ideal and image-force lowered barriers.

2.4.3 Model testing on nanostructured devices

The numerical simulations of the previous section have provided a first proof of the validity of Equation (2. 15). However, to definitively confirm the goodness of the model, it needs to be tested on real experimental data. For this reason, in this section the I-V characteristics of different nanostructured materials are analysed using the proposed model. The main motivation behind this

study was that despite the huge technological progresses, the realization of reliable contacts with nanostructured materials poses substantial issues[160–162] that hamper the understanding of the intrinsic electric transport properties and the exploitation of the nanomaterials in electronic and optoelectronic applications. Contacts are the communication links between the nanomaterials and the outer world, and the fabrication of ohmic contacts with linear current-voltage characteristics and low-resistance is still an open challenge.[162–164] One of the main problems is the lack of reproducibility as contacts realized under the same conditions and using the same metals can have different electrical characteristics ranging from Schottky to ohmic behaviour.[165] Moreover, the contacts can influence the conduction mechanism inside a device contributing to the change from the typical thermally activated band conduction to variable range hopping or space charge limited current.[118,121,166]



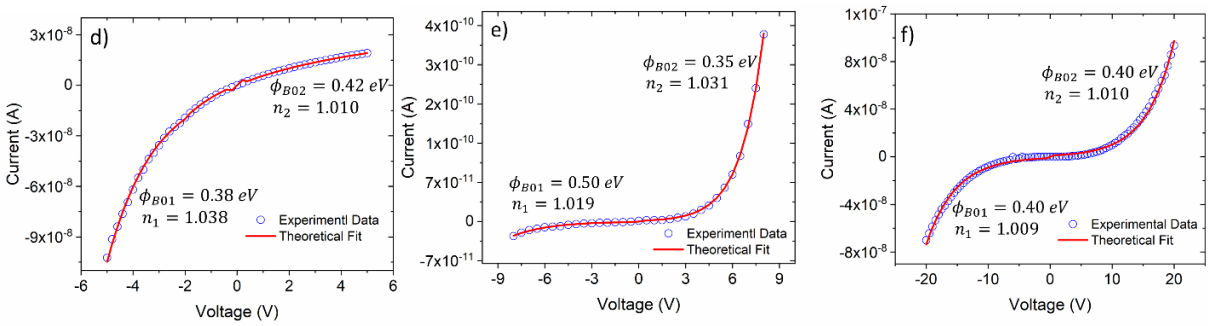


Figure 2.16 –a) SEM image of a MoS_2 flake contacted with four Ti/Au leads. b) SEM image of a WSe_2 flake covered with Ni/Au contacts. c) SEM image showing a single WS_2 nanotube contacted by two tungsten tips, marked as 1 and 2 respectively. d)-e)-f) I-V characteristic of the MoS_2, WSe_2 and WS_2 devices. The blue circles represent the experimental data, while the red lines are the fitting curves from Equation (2.15), with the SB height and the ideality factor as fitting parameters.

Figure (2.16 a-c) show the scanning electron microscope (SEM) images of three nanodevices: the first is a MoS_2 flake contacted with four Ti/Au leads,[167] the second is a WSe_2 flake covered with Ni/Au contacts[168] and the third is a single WS_2 nanotube stuck to two tungsten tips due to van der Waals interaction.[169] MoS_2 and WSe_2 flakes lay on an electrically grounded $SiO_2/p-Si$ substrate, while WS_2 nanotube is suspended between the two tungsten tips. The details of the fabrication, characterization and electrical measurements of MoS_2 and WSe_2 are subject of different studies conducted during this PhD project, while WS_2 nanotube transport properties will be discussed in detail in the next chapter .[167–169]

Figure (2.16 d) shows the I-V characteristic of the MoS_2 nanosheet with strongly asymmetric behaviour. This result confirms that contacts made simultaneously and under the same conditions can have different barrier height (the contact area is about the same). Figure (2.16 d) also shows the curve obtained from Equation (2.15), superposed to the experimental data, demonstrating the excellent fitting. The results of the fit confirm the presence of two different barriers at the contacts that occur to be $\phi_{B01} = 0.38\,eV$ and $\phi_{B02} = 0.42\,eV$ with ideality factor $n_1 = 1.038$ and $n_2 = 1.010$ respectively. From the literature the MoS_2 electron affinity ranges from $3.74\,eV$ to $4.45\,eV$,[170–172] while Ti work function is $4.33\,eV$. According to Equation (2.5), she SB height should range from $-0.12\,eV$ to $0.59\,eV$ where the negative values can be considered as the ohmic

contacts. So, Equation (2.5), also known as the Schottky-Mott rule, does not yield an accurate estimate of the barrier, especially for two-dimensional materials. Indeed, the Schottky-Mott model does not take into account the pinning of the Fermi level which may occur at both interfaces, even in an asymmetrical way. For this reason, it can only be used as a qualitative method to obtain the rough estimation of the SB. Moreover, our results are comparable with the SB height ranging from $0.31\ eV$ to $0.51\ eV$ experimentally determined in previous works.[134]

Figure (2.16 e) shows the I-V characteristic of the WSe_2 flake that presents a strong asymmetric behaviour. As expected, the fit yields two different values for the SB heights, namely $\phi_{B01} = 0.50\ eV$ and $\phi_{B02} = 0.35\ eV$ with ideality factor $n_1 = 1.019$ and $n_2 = 1.031$ respectively. In this case, considering that the Ni work function is about $5.0\ eV$ while the WSe_2 electron affinity is about $3.7\ eV$[173], the results from the fit of Equation (2.15) is not consistent with of Equation (2.5), that would give the unrealistic high barrier of $1.3\ eV$.

Figure (2.16 f) shows the I-V characteristic of the nanotube of Figure (2.16 c). The I-V curve is symmetric pointing to the presence of two equal barriers. The fit of Equation (2.15) perfectly reproduces the experimental data and allows the estimation of the SB height as $\phi_{B01} = \phi_{B02} = 0.40\ eV$ with ideality factor $n_1 = 1.009$ and $n_2 = 1.010$ respectively. In this case considering $\chi_s(WS_2) = 4.5\ eV$[174] and $\phi_M(W) = 4.32\ to\ 5.22\ eV$, the estimated barrier is within the range predicted by Equation (2.7), that is $-0.18\ eV$ to $0.72\ eV$.

2.5 Summary

In summary, in this chapter the results of four different experimental studies concerning the electrical properties of different 2D materials have been reported. In the first three paragraphs several applications of such layered materials as FETs channel have been shown. In particular, the intrinsic properties of the 2D materials were investigated focusing the interaction with various

external stimuli, such as temperature, pressure and electron or light irradiation. In the last paragraph the common problem of the presence of a double Schottky barrier at the interface between metal contacts and 2D materials is addressed, placing particular emphasis on the development of a model that allows to describe the I-V characteristic of this type of devices and to extract their typical figures of merit.

More specifically, in the first paragraph a study on back-gated field effect transistors with a channel made of ultrathin $PtSe_2$ film has been reported. The main result is that positive and negative photoconductivity can occur simultaneously and that the dominance of one over the other depends on the environmental pressure. This behaviour is explained by light-induced desorption of oxygen from the surface of the material and confirmed by DFT calculations that provided atomistic insights on the effects of physisorbed oxygen molecules on the band structure of semiconducting $PtSe_2$. The results of this work are applicable to any other 2D materials with oxygen dependent p-type doping and provides a potentially effective route for modulating their density of carriers.

In the second paragraph, the fabrication and the electrical characterization of BP field effect transistors have been reported. The main result of this research is the demonstration that the presence of a hysteresis in the FET transfer characteristic can be exploited to realize non-volatile memories with good endurance and retention time. Finally, encapsulation of BP with a PMMA protective layer has been demonstrated as a simple way to preserve the electrical properties of the memory over a month.

In the third paragraph, the fabrication of back-gate field effect transistors with ultrathin $GeAs$ films and the investigation of their electrical properties over a wide temperature range, from $20\ K$ to $280\ K$, have been reported. The most peculiar result is that the carrier density in $GeAs$ flakes depend on temperature with a pronounced and broad peak around $75\ K$. A model based on a

temperature-dependent channel thickness to explain such an anomaly has been proposed showing an excellent agreement with the experimental data. This study provides new understanding of the intrinsic properties of few-layer $GeAs$ as the channel of field effect transistors giving evidence of the formation of a 2D channel limited to a single atomic layer and could be applied to other ultrathin layered materials.

Finally, in the fourth paragraph, a simple model to describe the I-V characteristics of a generic semiconductor device with two Schottky junctions at the contacts has been proposed. The model includes non-idealities that make the barrier height dependent on the applied voltage and it can account for several experimental observation and fully reproduce both symmetric and asymmetric characteristics. The model has been tested by fitting the I-V characteristics of nanostructured devices with MoS_2 and WSe_2 nanosheets and WS_2 nanotubes. The model not only perfectly reproduces the experimental data but also allows to simultaneously extract the two contact barriers and their respective ideality factors.

Chapter 3: FIELD EMISSION FROM ONE DIMENSIONAL NANOSTRUCTURES

In this chapter, the results of two experimental studies regarding the electrical transport properties of 1D materials, such as gallium oxide (Ga_2O_3) nanopillars and tungsten disulphide (WS_2) nanotubes are reported, with particular attention to their possible use as field-emitting devices. The term field emission refers to the phenomenon of electron emission from a conductive surface, i.e. metallic or semiconductor material, under the application of an electrostatic field. This is also called cold cathodes emission, to differentiate it from the electron extraction generated by raising the sample temperature, i.e. thermionic emission. For long time this effect has not been fully understood and only in the late 1920s has received an explanation. The merit of such explanation is due to Fowler and Nordheim, who demonstrated that field emission could be described considering electron tunneling through a triangular potential barrier. To escape from a surface, an electron needs sufficient energy to overcome the surface-vacuum barrier, i.e. the workfunction of the metal. The phenomenon can also be generalized for semiconductors.

Fowler and Nordheim proposed a simple equation to describe the current-voltage relationship which regulates the field emission:

$$I = \frac{AaE_s^2}{\varphi} \exp\left(-b\frac{\varphi^{3/2}}{E_s}\right) \qquad (3.1)$$

where A is the emitting area, E_s is the local electric field, φ is the workfunction of the semiconducting material and $a = 1.54 \cdot 10^{-6}\ A\ eV\ V^{-2}$ and $b = 6.83 \cdot 10^{9}\ V\ m^{-1}\ eV^{-\frac{3}{2}}$ are constants. Even if, it was proposed for emission from flat metallic surfaces, Equation (3.1) has been successfully used to describe the field emission current of different nanostructured materials, just considering minor adjustments needed to take into account their 2D or 1D nature, as it will be

shown in the following paragraphs.

Although initially the field emission was considered an undesirable effect, as it could cause vacuum breakdown and discharge phenomena, nowadays several applications are based on this phenomenon. The most common are certainly those in the field of microscopy and spectroscopy, but there was no lack of proposals for use of field electron emitters as electron-gun sources or as active components for vacuum electronics. A great boost to research in the field of field emission was given by the discovery of 2D and 1D materials. Their large aspect ratio, indeed, allows to intensify the fields at their edges, making it easier to extract electrons from the surface. Carbon nanotubes were the first and most studied nanostructured materials proposed as field emitters, showing promising results. However, a great research effort is still needed to optimize the performance of field emitting devices and their figures of merit such as the turn on field (E_{ON}), i.e. the minimum electric field from which it is possible to extract electrons, and the max current density (J_{max}), i.e. the maximum field emission current that can be recorded without damaging the material.

In the first paragraph of this chapter, an experimental study on the field emission properties of an individual Ga_2O_3 nanopillar is reported. This material was selected because of its excellent physical and chemical properties, which combined with its ultrawide bandgap make it promising for conducting high current densities without damage. As expected, the experimental results demonstrated that Ga_2O_3 shaped in the form of nanopillars can be a performant and competitive field emitter with low turn-on field and very high current density. The results of this work derive from a collaboration with the Helmholtz-Zentrum and the Leibnniz-Institut of Berlin and they led to the publication of the paper " High field-emission current density from $\beta - Ga_2O_3$ nanopillars" by Grillo et al. published on Applied Physics Letters in 2019.

In the second paragraph, an experimental study on the electrical properties of multiwalled WS_2 NTs under electron beam (e-beam) irradiation and axial strain is reported. The obtained good figures of merit suggest that WS_2 NTs can be suitable for the realization of practical field emitting devices. Moreover, changes in resistivity for strain increasing up to 12% evidenced another possible application as piezoresistive strain sensors. The results of this study derive from a collaboration with the HIT-Holon Institute of Technology in Israel and resulted in the publication of the paper " WS_2 nanotubes: Electrical conduction and field emission under electron irradiation and mechanical stress" by Grillo et al. published on Small in 2020.

3.1 Gallium Oxide (Ga_2O_3)

The first material investigated as field emitter is Ga_2O_3. It is considered a promising candidate for high power electronics application owing to its excellent physical and chemical properties[175]. Among the five polymorphs, $\beta - Ga_2O_3$ is the thermodynamically stable phase at room temperature and atmospheric pressure [176]. It has a wide bandgap of about $4.8\ eV$[177] and a very high breakdown electric field[178] ($E_{br} \sim 8\ MVcm^{-1}$), three times larger than that of SiC and GaN, which enables handling huge switching voltages. Moreover, the Baliga figure of merit ($BFOM = \varepsilon_r \mu E_g$, where ε_r is the relative dielectric constant, μ is the electron mobility and E_g is the bandgap of the semiconductor), a parameter used to assess the suitability of a semiconductor for power device applications, is several times larger than that of SiC and GaN[179]. Hence, $\beta - Ga_2O_3$ based power devices offer a significant reduction of the current loss[180].

Due to the high mechanical strength, chemical stability, heat dissipation and charge transport capability, the patterning of nanowires or nanopillars renders $\beta - Ga_2O_3$ a good candidate for field emission applications[156,181–185]. Huang et al. reported field emission from quasi-aligned Ga_2O_3 nanowires fabricated using a brass wire mesh as the substrate and estimated a field enhancement

factor of about 880 at a cathode-anode distance of about $100\ \mu m$[186]. Lòpez et al. investigated the field emission properties of Ga_2O_3 nanowires with Sn-dopant enhanced electrical conductivity[187]. They reported a field enhancement factor of 3287 measured at a cathode-anode distance of $400\ \mu m$. Finally, Tien et al. investigated field emission from Ga_2O_3 nanobelts synthesized in different oxygen ambient and achieved a field enhancement factor as high as 2242 for 1% oxygen level[188].

So far, all field emission studies have been dealing with meshes or arrays of Ga_2O_3 nanostructures, where the field emission properties are averaged over a large number of emitters. During the present PhD project, individual $\beta - Ga_2O_3$ single crystal nanopillars were realized, purposely designed for the investigation of the field emission current. The field emission from a single β-Ga_2O_3 nanopillar was investigated demonstrating that the $\beta - Ga_2O_3$ nano-patterning, combined with the intrinsic properties of the material, enables a class of performant and competitive field emitters with low turn-on field and very high current density and field-enhancement factor.

3.1.1 Nanolithography process for nanopillars fabrication

The sample used for the experiment was a (100) $\beta - Ga_2O_3$ single crystal, which was produced using the Czochralski method[189–191]. The unit cell of $\beta - Ga_2O_3$ as well as the crystal orientation of the samples are presented in Figure (3.1 a). The size of the samples was $10x10\ mm^2$. Prior to the patterning process, the sample was cleaned in a sequence of 1-minute ultrasonic baths with ethanol, acetone and distilled water, at a temperature of 22°C. Finally, an argon plasma was applied on it for about 5 minutes at a pressure of $0.3\ mbar$ and a power of $40\ W$. A Carl Zeiss Orion NanoFab microscope was used for the fabrication and imaging of the nanopillars. The corresponding experimental setup is shown in Figure (3.1 b). The imaging of the nanopillars was realized through the collection of the sputtered secondary electrons with an Everhart-Thornley detector. The use of

a helium source results in images with a great contrast and a large depth of field, because of the small De Broglie wavelength of the ions (the probe size is typically $\sim 0.5\ nm$[192]). However, this imaging technique is also destructive since the target atoms are also sputtered by the ions[193]. For lithography purposes, the use of helium ions is not appropriate because of surface blistering[194]. It is possible to switch to neon ions in the Orion setup, for which there is no noticeable blistering effect. The Ne^+ beam was used all throughout this work for the fabrication of nanostructures, while the He^+ beam is used for convenient in-situ imaging. The Ne^+ beam was regulated at an energy of $30\ keV$ for producing an isolated pillar. To increase the control on the single pillar diameter, the nanofabrication process was divided in three steps: (i) milling of a $2x2\ \mu m^2$ square with a central pillar of $\sim 500\ nm$ diameter, (ii) rough polishing of the central pillar, reduced to a diameter of $\sim 150\ nm$, (iii) fine polishing of the central pillar to obtain the sharpest and finest pillar possible. This process results in spatially separated individual pillars with a height of $\sim 400\ nm$ and a diameter of $70\ nm$ (Figure (3.1c)). Some squares were intentionally etched without the central pillar.

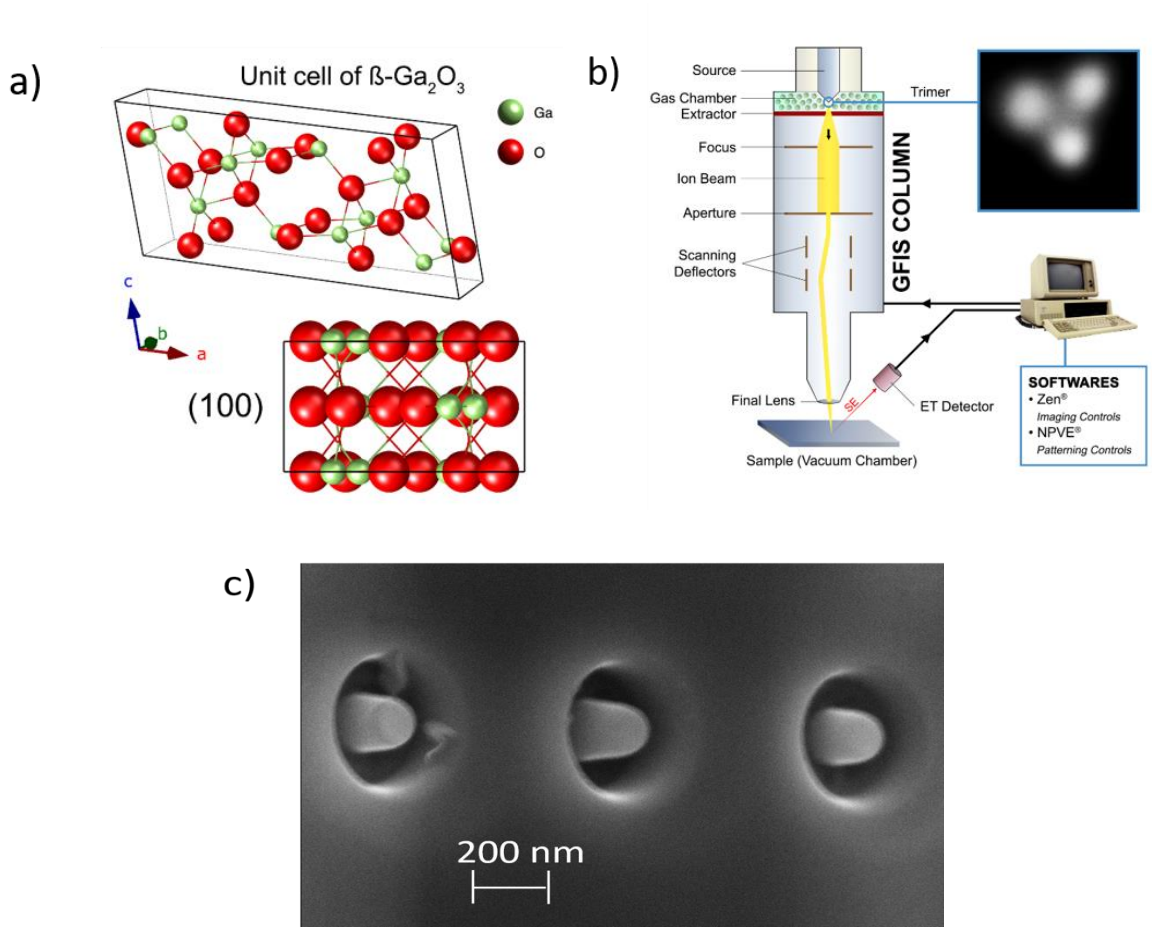


Figure 3.1 – a) Monoclinic unit cell of ß-Ga_2O_3 with the lattice parameters[7] a = 12.214 Å, b = 3.0371 Å, c = 5.7981 Å and ß = 103.8°[7]. A projection of the cell in the (100) plane is shown below the unit cell. b) Experimental setup of the Carl Zeiss Orion NanoFab helium ion microscope. The inset shows an in-situ *image of the trimer. c) SEM image of three nanopillars with ~400 nm height and ~70 nm diameter.*

3.1.2 Field emission measurements experimental setup

The electrical characterization of this devices was carried out in collaboration with the University of L'Aquila, where the field emission properties were investigated during a series of scientific missions of the candidate. All electrical measurements were performed with the sample kept inside a Zeiss LEO 1530 SEM chamber in high vacuum (pressure < 10^{-6} mbar) and at room temperature. A W-tip, mounted on a piezoelectric-driven arm, installed inside the SEM chamber, and the SEM sample holder were electrically connected to a semiconductor parameter analyser (Keithley 4200-SCS) and

used as the anode and the cathode for the two-terminal device characterization. The W-tip positioning was controlled with a resolution better than $5\ nm$ in all directions. Figure (3.2 a) shows a diagram of the measurement setup. The W-tip (anode), guided by the SEM arm, is gently approached to the surface of the sample until it establishes an intimate electrical contact with it (Figure (3.2 b)). An ohmic contact (cathode) on the backside of the sample is created with silver paste covering a large scratched area of the $\beta - Ga_2O_3$ sample.

3.1.3 I-V characteristic

As usual, the first approach was to perform a standard electrical characterization. The I-V characteristic between top and bottom contacts is shown in Figure (3.2 c). The curve exhibits a pronounced rectifying behavior with a rectification ratio, defined as the current ratio at $\pm 5V$, greater than 10^6, pointing to the formation of Schottky barriers, as explained in Chapter 2.[134]

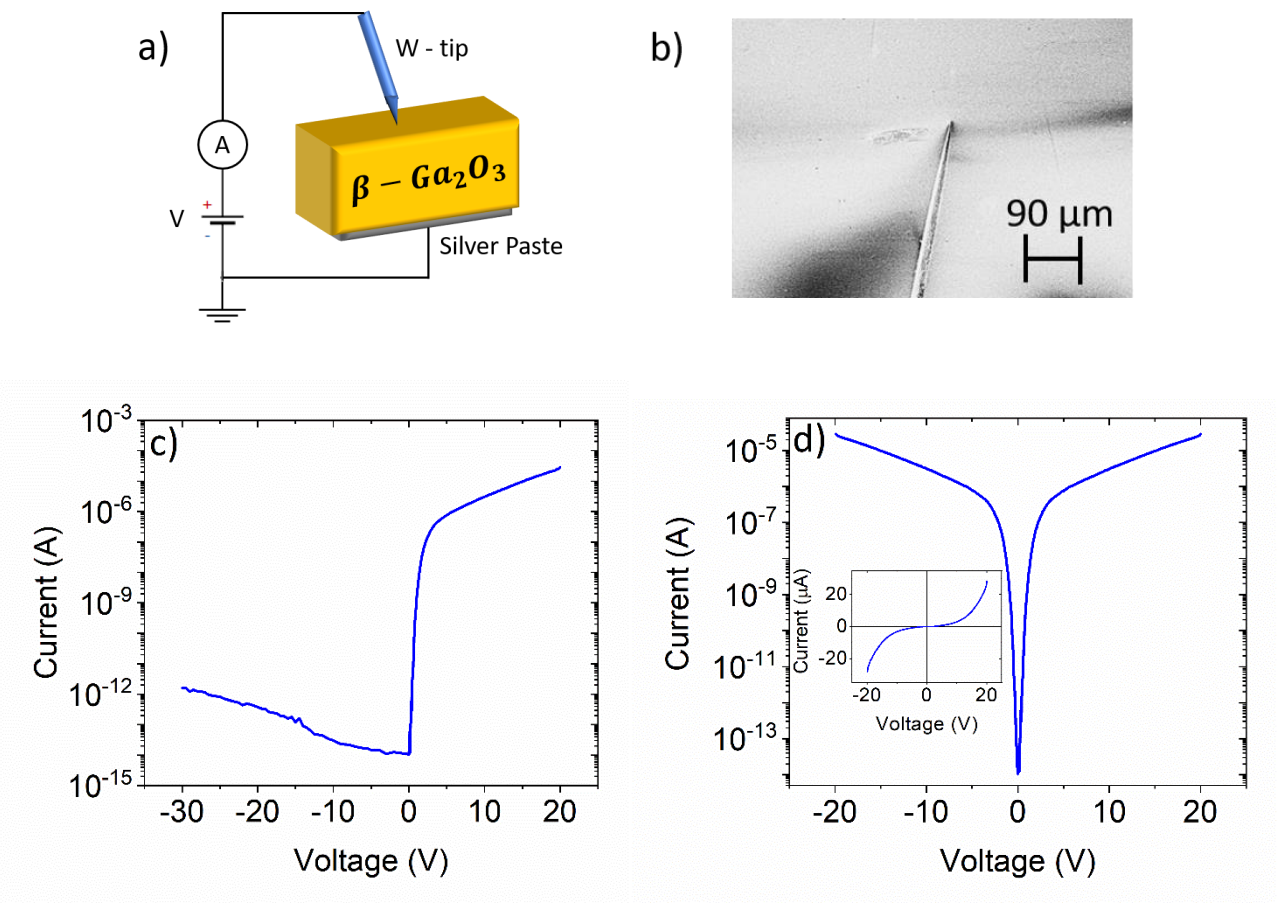


Figure 3.2 – a) Diagram of the measurement setup: a tungsten tip, placed on the top surface of the sample and a large silver paste bottom contact are electrically connected to a source measurement unit (SMU Keithley 4200 SCS). b) SEM image of the tungsten tip used as contact for the electrical measurements. c) Two-probe I-V characteristic between the W-tip and the back Ag-paste contact used as the anode and the cathode of a two-terminal device. d) I-V characteristic between two silver-paste contacts placed on the top and on the bottom of the device, respectively (the inset shows the current on linear scale).

The forward current at positive bias confirms the n-type behavior of the $\beta - Ga_2O_3$ sample, which can facilitate the extraction of a field emission current. To check that the Ag-contact on the bottom of the device iwas non-rectifying, a similar contact of silver paste was realized on the top of the sample and I-V measurements were performed between these two contacts. The result is shown in

Figure (3.2 d), from which a symmetrical although non-linear characteristic is noted as a confirmation of the non-rectifying nature of the Ag-paste contacts.

3.1.4 Field emission measurements

To perform field emission measurements, the W-tip was moved away from the sample surface at given distances. The field-emission current was first measured from the edge of a box that does not contain the pillar, at two selected tip-edge distances d' $\sim 200\ nm$ and d' $\sim 350\ nm$ (Figure (3.3 a)). The current was monitored while the voltage was ramped up to 60 V (a constraint imposed to avoid damage of the device and of the measurement setup).

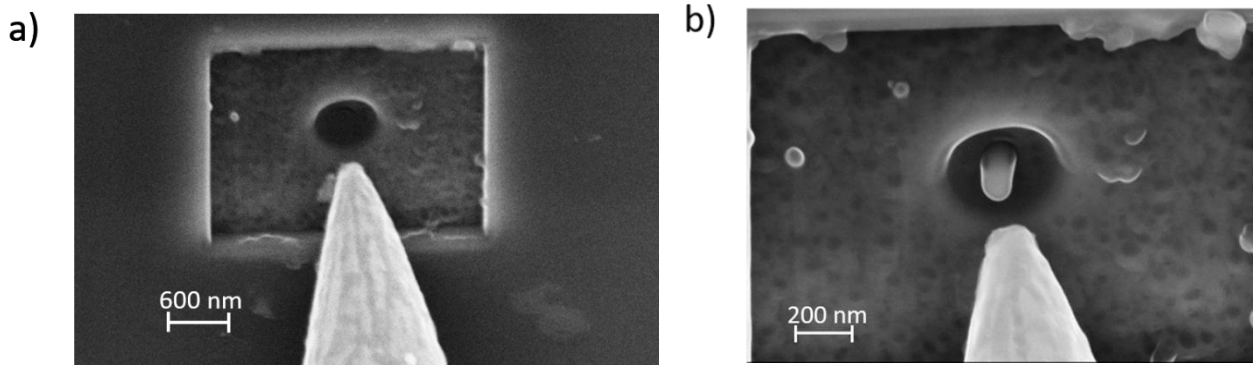


Figure 3.3 – SEM images showing the W-tip positioning for field emission measurements. The W-Tip is close to (a) the step edge of the box or to (b) the apex of the nanopillar, which is the emitter site.

Figure (3.4 a) shows that for a voltage up to $\sim 40\ V$ the current fluctuates around the noise floor $\sim 10^{-13} A$, and no clear charge flow is detected. For $V > 40\ V$ an exponential increase of the current is observed. Measurements at a distance $d' < 200\ nm$ easily result in uncontrolled tip-edge contacting caused by the attractive electrostatic-force, while for $d' > 350\ nm$ a field emission current is hardily extracted given the limitation imposed to the maximum applied voltage.

Next, the W-tip was moved above the top of one of the nanopillars as shown in Figure (3.3 b), and the current was measured with the same parameters reported above, at three different distances. This time, a field emission current was measured, over the same voltage range, even at $d = 1\ \mu m$ distance, clearly indicating the better field emission performance of the nanotip-shaped $\beta - Ga_2O_3$. The extraction of the current from the nanopillar occurs at a much lower voltage and achieves higher current value under the same applied electric field if compared with the similar measurements from the step edge (Figure (3.4 b)). The smoother increase of the field emission current at higher voltages, as noticed from Figure (3.4 b) compared to Figure (3.4 a), is due to the series resistance of the nanopillar. At $d = 400\ nm$ and $45\ V$ bias a remarkable density current higher than $100\ A/cm^2$ is obtained. This current density, although affected by an incertitude around 10%, is particularly relevant when compared to the one obtained from several other materials under similar experimental conditions. For instance, at comparable high electric fields, Gallium Nitride[195–197], Zinc Oxide[198] or Molybdenum Oxide[199] emit a current with a density that is few orders of magnitude lower. The achieved current density is also higher than the one of $\sim 10\ A/cm^2$ reported for carbon nanotubes [200–202]. We note that the $\beta - Ga_2O_3$ nanopillar also competes with individual carbon nanotubes, measured in similar conditions, for the turn-on field[203,204] and the stability[204,205].

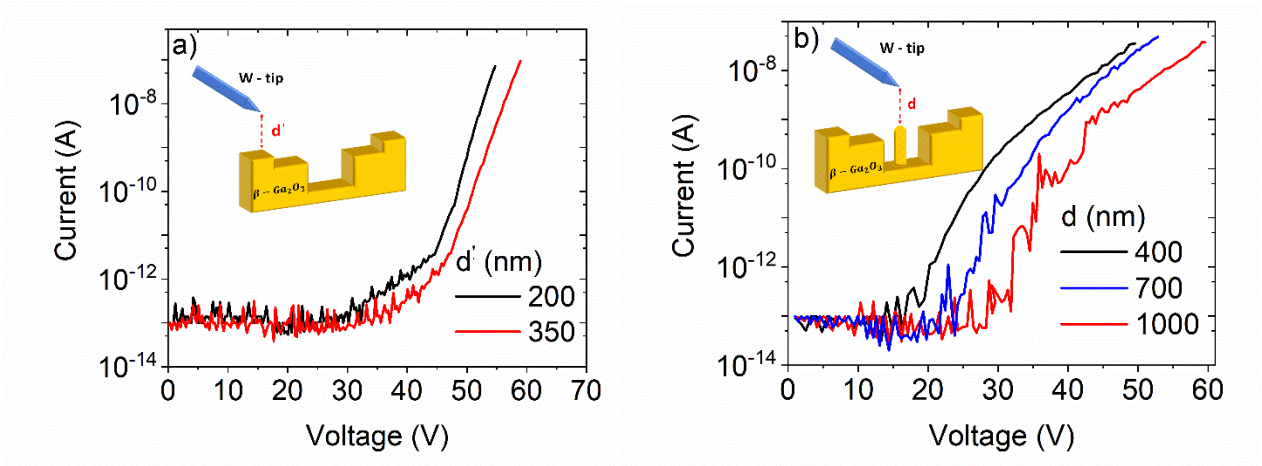


Figure 3.4 – a) Field emission current as a function of the applied voltage measured at a tip-box edge distance d' of $200\ nm$ *(black line) and* $350\ nm$ *(red line); the inset shows the measurement setup. b) Field emission current as a function of the applied voltage measured at a tip-top nanopillar distance* d *of* $400, 700$ *and* $1000\ nm$*; the inset shows the measurement setup.*

3.1.5 Fowler-Nordheim analysis

To confirm the field-emission nature of the measured current, the I-V curves are analyzed in the framework of the classical Fowler-Nordheim (FN) theory[204,206]. Equation (3.1) is used, imposing $\varphi = 4.8\ eV$ for the Ga_2O_3 work function.[207] In a parallel plate configuration, the electric field is simply V/d. As said in the introduction a slight deviation from the ideal FN equation is needed to consider the 1D nature of the emitter. In particular, to account for the spherical termination of the W-tip in our setup, an anode-correction factor $k \approx 1.5$ must be introduced[208] and the applied electric field is expressed as $\frac{V}{kd}$. Figure (3.4 b) shows a field emission current starting at $20\ V$ for $d = 400\ nm$, which corresponds to the low applied turn-on field $E_{on} \approx 30\ V/\mu m$. The pointed cathode enables a local amplification of the applied field, owing to the accumulation of the field lines at the apex of the emitting site. Introducing a β factor to account for such amplification, the local field E_s is finally expressed as: $E_s = \beta \frac{V}{d \cdot k}$. The so-called field enhancement factor β constitutes an important figure-of-merit in field emission studies, being strictly dependent on the shape of the emitter. The higher is β, the more performant is the field emitter.

The FN behavior of the measured emission current is confirmed by the linearity of $ln(I/V^2)\ vs\ 1/V$ curves (FN plot), shown in figures (3.5 a) and (3.5 b). The slope of the fitting straight lines ($m = (b\varphi^{\frac{3}{2}}\ dk)/\beta$) are used to estimate the field enhancement factor[209], which is displayed in Figure

(3.6 a) for different cathode-anode distances. The nanopillar has a β about ten times larger than that of the box edge because of its shaper form and higher aspect ratio that greatly enhance the local electric field. Also, β increases with the cathode-anode distance, consistently with what has been reported for field emission from carbon nanotubes[204,208] or nanowires[209]. The field enhancement factor is often used as the parameter to benchmark a field emitter, despite it can strongly depend on the measurement setup. A significant comparison is therefore possible only when the measurements are performed under the same experimental conditions. That said, for a rough assessment of the single Ga_2O_3 nanopillar field emission performance against other cold cathodes, the linear β-distance behavior of Figure (3.5 a) to distances comparable with the ones of $100 - 400\ \mu m$[186–188] reported in previous works that have used differently-shaped Ga_2O_3 has been extrapolated. This is a reasonable assumption, based on the experimental observation that the field enhancement factor increases with the distance[31,32,210]. The resulting $\beta > 4000$ at a distance of $100\ \mu m$ suggests that the nanopillars here presented are not only better than other, differently-shaped, Ga_2O_3 field emitters[186–188], but are also competitive with emitters known for their high field enhancement factor and low turn on field like carbon nanotubes[211,212].

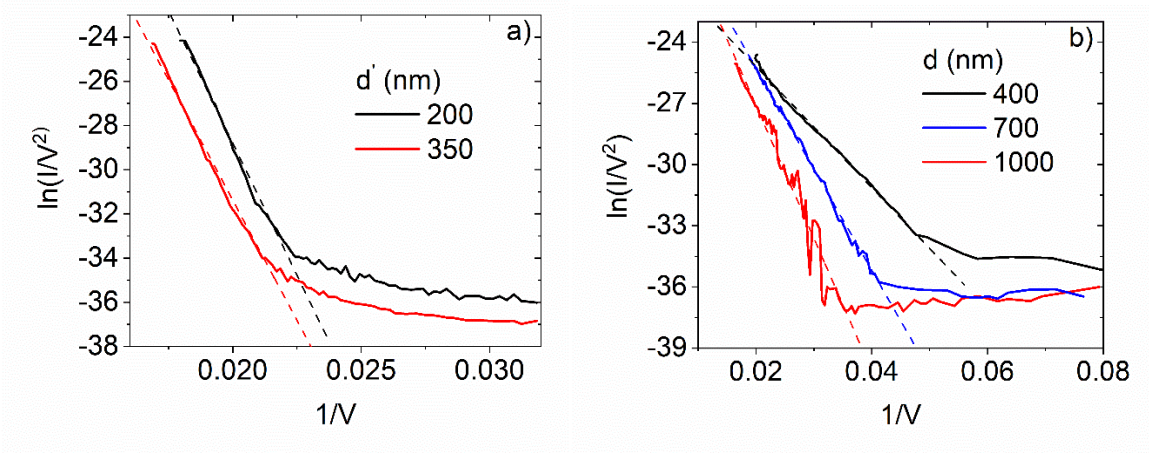


Figure 3.5 - (a) and (b) Fowler- Nordheim plots corresponding to the currents of Figures (3.5 a) and (3.5 b), respectively.

The current stability is another important parameter that a good field emitter must possess. The field emission stability of the $\beta - Ga_2O_3$ nanopillar was checked under the applied bias of $40\ V$ with the W-tip at $400\ nm$. Figure (3.6 b) plots the current for a time of 25 minutes and shows fluctuations within 10% of the average value, which is a satisfactory result, especially taking into account the difficulty to control the W-tip/nanopillar distance over time. As well known, the emission current instability is mainly caused by the local heating effect in metal oxide semiconductor emitters[213]. Then the observed good stability indicates an efficient heat dissipation of the fabricated nanopillar, despite the low thermal conductivity of $\beta - Ga_2O_3$ ($\sim 21\ Wm^{-1}K^{-1}$).[214]

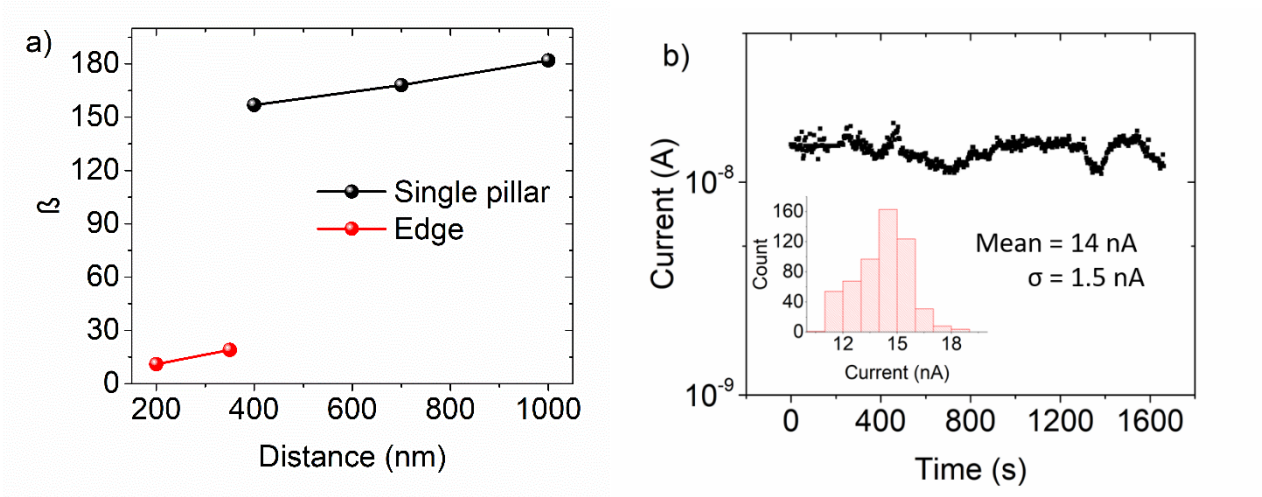


Figure 3.6 – a) Field enhancement factor β vs cathode-anode distance for the single nanopillar and for the box edge emitter. b) Field emission current versus time. The inset shows the histogram of the current with mean and standard deviation.

3.2 Tungsten Disulphide (WS_2)

The last material whose electrical properties investigation is reported in this thesis is tungsten disulphide (WS_2), another member of the TMDs family, shaped in the form of a nanotube. As described in Chapter 1, also WS_2 presents a layered structure where monolayers, constituted by a plane of W atoms sandwiched between two planes of S atoms, are piled on top of each other and bonded by weak van der Waals forces. WS_2 presents a highly anisotropic nature which is reflected in its mechanical,[215] optoelectronic and electrical properties,[216] and has been proposed for several applications, such as solar cells[217] and catalysis,[218,219] or used as a solid lubricant.[220] Since the electronic properties of INTs mostly derive from the bulk material counterpart, multi-walled WS_2 NTs are exclusively semiconductors, with a well-defined band gap ranging from $0.1\ eV$ to $1.9\ eV$, depending on their diameter.[221,222] Theoretical calculations done for single layered nanotubes showed that, depending on their chirality, WS_2 NTs band gap can be both direct (for zigzag) and indirect (for armchair), with values varying with diameter as well.[223] WS_2 nanotubes were isolated for the first time in 1992[224] and ever since several synthesis methods have been explored.[225–228]Their scalable production was reported in 2009[229] and further revised recently, extending the acquired experience to the synthesis of MoS_2 INTs in pure phase and significant amounts.[230] The availability of these nanotubes has raised a great interest in the scientific community and has enabled the wide investigation of their properties. The layered structure of WS_2 INTs supports inert van der Waals surface combined with excellent optoelectrical properties[231–235] making WS_2 NTs suitable candidates for the next generation of electronic and optoelectronic applications. Moreover, the defect-free structural morphology of WS_2 NTs result in excellent mechanical properties,[236–240] making them resistant to large tensile and compressive forces and pressure shockwaves.[241] It has been also demonstrated that WS_2 NTs are nontoxic and biologically benign.[242] Although there are

many studies on the structural and mechanical properties of WS_2 nanotubes, still few researches have been dealing with their electronic[243–245] and, particularly, with electro-mechanical[246] properties. For instance, a study of the resonant torsional behaviour has shown that WS_2 NTs have higher quality factor (Q) and torsional resonance frequency than boron nitride or carbon nanotubes, which makes them promising building blocks for high-Q nanoelectromechanical systems.[247] Moreover, using density-functional theory, it has been predicted that substantial tensile strain can reduce the bandgap, or even induce a semiconductor-to-metal transition, and dramatically affect the quantum conductance in large diameter single- and multi-walled WS_2 NTs,[246] but no experimental evidence has been provided yet.

The paragraphs below report the fabrication and an experimental electrical and electro-mechanical characterization of individual multi-walled WS_2 nanotubes. The electrical conduction of WS_2 NTs is measured in a standard two-contact configuration, under electron beam (e-beam) irradiation and axial strain. Carbonaceous deposits induced by electron irradiation of the nanotube-metal electrode area are used to improve the electrical quality and the mechanical stability of the contacts. Indeed, electron beam exposure of both contacts yields more than two orders of magnitude increase of the NT current. The high aspect ratio of WS_2 NTs suggests their use for field emission applications. In this study, a field emission current density up to $600\,\frac{kA}{cm^2}$, with turn-on field of $\sim 100\,\frac{V}{\mu m}$ and field enhancement factor $\beta \sim 50$, is obtained from a single WS_2 NT. Despite the theoretically predicted reduction of the bandgap[246], it is found that the resistivity of a multi-walled WS_2 NT increases exponentially with the applied axial tensile stress. Changes in resistivity have been recorded for strain increasing up to 12%, evidencing the suitability of individual multi-walled WS_2 NTs as piezoresistive strain sensors.

3.2.1 Solid-gas synthetic approach fabrication method

Multi-walled WS_2 NTs were synthesized through the high temperature solid-gas synthetic approach using tungsten oxide nanoparticles as precursor and H_2S and H_2 as reactive gases.[248] As the first step, tungsten oxide nanowhiskers with length $\leq 20\ \mu m$ are obtained from loosely agglomerated oxide nanospheres of $\sim 80\ nm$ diameter. The mild reduction of the precursor oxide into the intermediate volatile tungsten suboxide phase served as a building material for the suboxide nanowhiskers growth. Subsequently, the suboxide nanowhiskers are converted into hollow multi-walled tungsten disulphide NTs by an outside inwards oxygen/sulphur exchange reaction**.** Figure (3.7) shows transmission electron microscope (TEM) and scanning electron microscope (SEM) images of the final product. The multi-walled WS_2 NTs have length in the range 2–20 μm and diameter between WS_2 and $120\ nm$. The radial direction, perpendicular to the layers and nanotube axis, is the c-axis (002), while the interlayer distance is $0.63\ nm$.

3.2.2 Sample preparation and field emission setup

For the electrical characterization, the as prepared NTs were dispersed into acetone and solution-casted on a flat $SiO_2/p-Si$ substrate. The SEM image of Figure (3.7 d) shows that the WS_2 NTs deposited on the substrate form a random mesh of bundles, from which individual NTs can be picked up by a piezo-driven nanotips, as we will see next. The setup for the electrical measurements is the same used for the characterization of the Ga_2O_3 nanopillar.

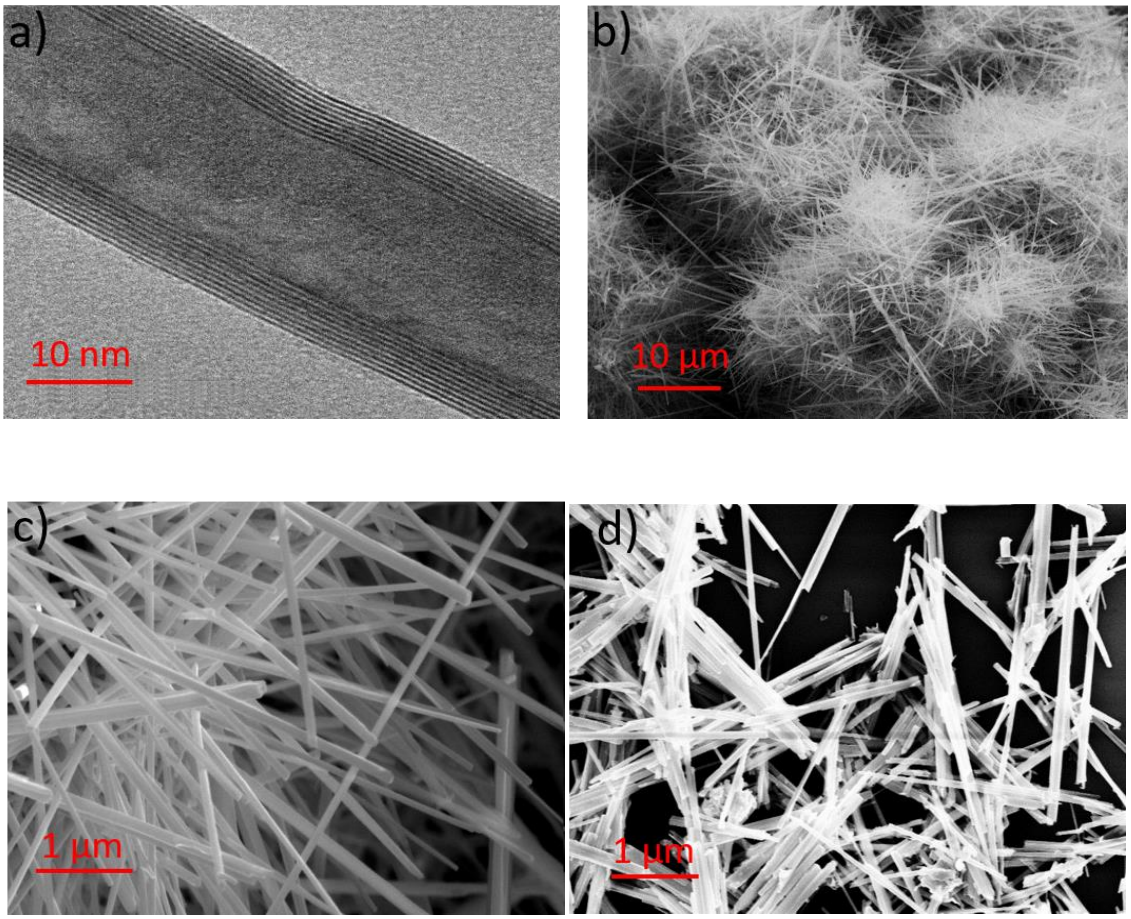


Figure 3.7 - a) TEM image of a single multi-walled WS2 NT. b) SEM image of the WS_2 NTs as obtained from the production process. c) Higher magnification SEM image of as-produced WS_2 NTs. d) SEM image of mesh of WS_2 NT bundles deposited after dispersion on a $SiO_2/p-Si$ substrate.

3.2.3 X-ray photoelectron spectroscopy

The morphology and the compositional-electronic properties of the WS_2 NTs were obtained by SEM and X-ray photoelectron spectroscopy (XPS), respectively. The SEM images were taken through the same microscope used for the electrical characterization, equipped with two piezoelectric-driven tungsten nanoprobes (referred as W-tips), that were used to manipulate and contact the WS_2 NTs for the electrical transport measurements. XPS measurements were performed in a PHI ESCA ultra-

high vacuum chamber ($P \approx 10^{-10}\ Torr$) endowed with a Mg X-ray source ($h\nu = 1253.6\ eV$) and a hemispherical analyser. To get the relative concentration and chemical states of the elements in the WS_2 NTs, XPS analysis was surveyed in the binding energy (BE) $0 - 1000\ eV$ range, over $0.8 \times 2.0\ mm^2$ area, as shown in Figure (3.8 a). The survey scan shows the presence of O, C, S, and W. In particular, $C\ 1s$ and $O\ 1s$ peaks are attributed to surface adventitious atmospheric carbon and adsorbed surface water molecules, respectively. No contamination species were observed within the sensitivity of the instrument. High-resolution spectrum of all the core level spectra were acquired with a pass energy of $11.85\ eV$, corresponding to an overall experimental resolution of $0.75\ eV$, and the BE calibration of the spectra was referred to $C\ 1s$ peak located at $BE = 284.8\ eV$.[249]

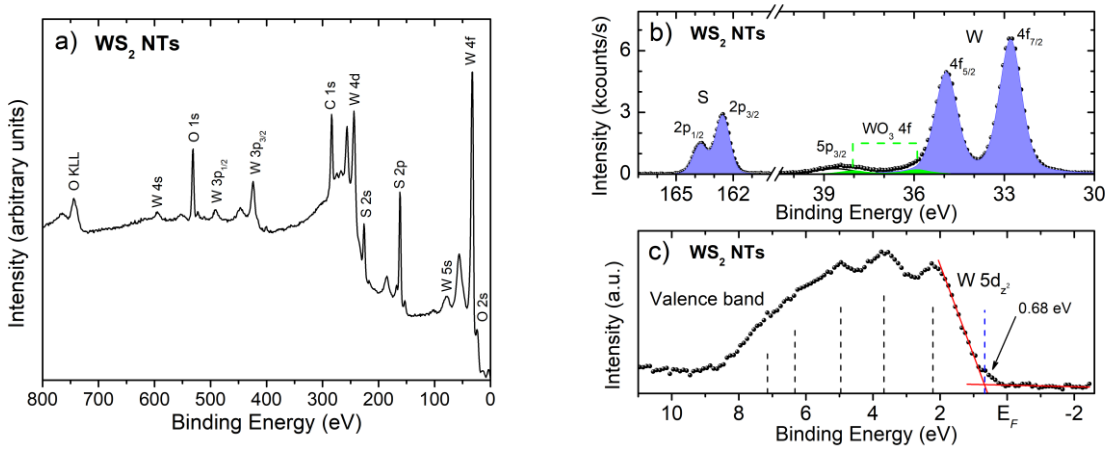


Figure 3.8 - a) Survey spectrum of the as-prepared multi-walled WS_2 NTs. High-resolution XPS spectra; b) S 2p and W 4f core level peaks; c) Valence band of WS_2 NTs.

Figure (3.8 b) illustrates the deconvoluted $S\ 2p$ and $W\ 4f$ electron core-level XPS spectra from the WS_2 NTs. The $S\ 2p$ and $W\ 4f$ levels are each formed by the convolution of two peaks due to the spin-orbit splitting (s.o.s.) that produce the $2p_{\frac{3}{2}}$ and $2p_{\frac{1}{2}}$ and $4f_{\frac{7}{2}}$ and $4f_{\frac{5}{2}}$ core level peaks for S and

W, respectively. The XPS data analysis of the S, W, O and C (that are not shown here) was performed with the XPSPeak4.1 program, and a Shirley function was used to subtract the background. The BE core level peak positions, the s.o.s. and the calculated atomic concentration, of the elements, are listed in Table (3.1). In the last column, the functional groups of the $C\ 1s$ are reported.

Table (3.1). Core level peaks position BE, s.o.s. and atomic concentration (%) of different elements; BE of the functional groups $C\ 1s$ and the relative $O\ 1s$.

Elements	WS_2 Core level peak BE(s.o.s.) (eV)			WO_3 Core level peak BE(s.o.s.) (eV)			Functional groups of C 1s (eV)			
	$2p_{3/2}$	$4f_{7/2}$	At. Co. (%)	$4f_{7/2}$	1s	At. Co. (%)	C-C	C-OH	C-O-C	C=O
S	162.6(1.2)	-	66	-	-	-	-	-	-	-
W	-	32.8(2.1)	34	35.8(2.1)	-	30	-	-	-	-
O	-	-	-	-	530.6	70	-	533.8	532.3	-
C	-	-	-	-	-	-	284.8	285.9	286.9	288.2

From the BE of the deconvoluted peaks (Table (3.1)), $W\ 4f$ level has two core peaks at a BE of 32.8 and $34.9\ eV$ that can be ascribed to the $W^{4+}\ 4f_{\frac{7}{2}}$ and $W^{4+}\ 4f_{\frac{5}{2}}$ in WS_2 NTs. In addition, the W spectrum (Figure (3.7 b)) presents a double peak, at BE of 35.8 and $37.9\ eV$, due to $W^{6+}\ 4f$, which

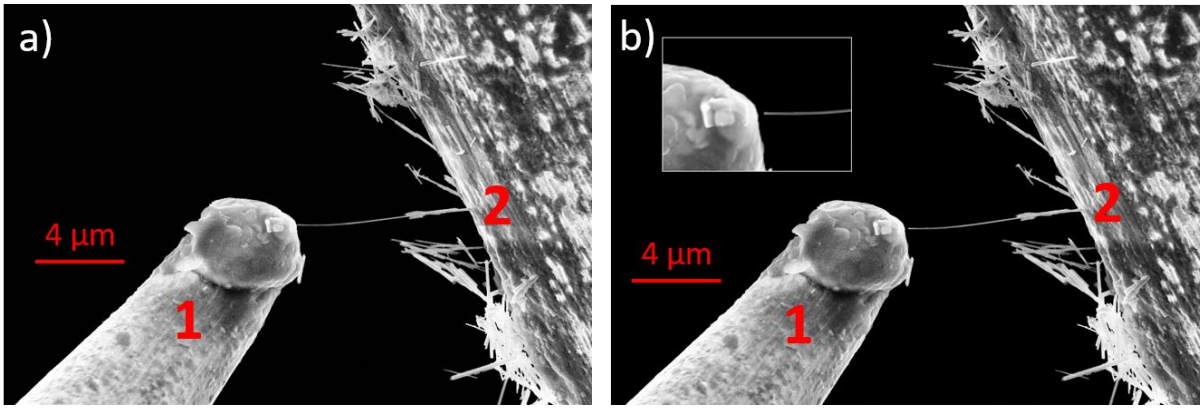
indicates a slight amount of WO_x in the WS_2 NTs. The s.o.s. for $S\ 2p$ produces two well defined peaks at 162.6 and $163.8\ eV$, respectively due to $2p_{\frac{3}{2}}$ and $2p_{\frac{1}{2}}$ core levels, which correspond to the S^{2-} orbitals. A quantitative analysis of the integrated peak area gives the atomic concentration of various constituents, by using the Physical-Electronic peak area sensitivity factors: 0.717 for S, 3.863 for W and 0.733 for O. The results reported in Table (3.1) indicate a $W{:}S$ atomic ratio of $1.0{:}\,1.9$ indicating a very close stoichiometric composition of the grown WS_2 NTs. Furthermore, $W{:}O$ atomic ratio of about $1.0{:}\,2.5$, very closed to $WO_{2.72}$, that can be ascribed to suboxide residuals (intermediate precursor) rest in the core of anomaly wide nanotubes (slow diffusion reaction of gases into wide tubes may not complete oxygen-to-sulphur conversion), which is in compliance with the INTs' growth mechanism.[230,248] The $S\ 2p$ well-resolved peaks, the W^{4+} and S^{2-} species character, in agreement with the elemental composition data, suggest a good quality WS_2 NTs.

Figure (3.8 c) shows the valence band of the WS_2 NTs in which, between $WS_2$and Fermi level (E_F), five peaks (black dashed line), mainly due to the strong hybridization of $W\ 5d$ and $S\ 3p$ states, are well resolved. At $\sim 2.2\ eV$ electronic states from $W\ 5d_z$ orbital are generated with a valence band edge located at $0.68\ eV$ below E_F, that gives to the WS_2 NTs a behavior alike the WS_2 bulk.[250] Moreover, considering a bandgap of $1.57\ eV$ for the bulk[251] this material can be considered a p-type semiconductor, with a little amount of states near the Fermi level due to WO_x. We note that WO_x residuals, being highly conducting, can be beneficial for NT contacting and field emission applications.

Finally, for the electrical measurements the same setup described for the charcaterization of $\beta - Ga_2O_3$ nanopillar was used.

3.2.4 I-V and field emission characterizations

As usual. The first approach was to perform a standard I-V characteristic. The W-tip labelled 2 was slowly moved through the WS_2 NT mesh on the $SiO_2/p-Si$ substrate to allow NT bundles to attach to it by van der Waals forces. A bundle oriented perpendicularly to the W-tip and with a protruding single WS_2 nanotube was selected and approached by the other W-tip (labelled 1) until the nanotube got stuck to it (Figure (3.9 a)). The black curve in Figure (3.9 c) shows the I-V current-voltage characteristic recorded in this configuration, highlighting a non-linear symmetric behaviour typical of high resistance electrical contacts with tunnelling barriers.[134,252,253] To improve the electrical contact between the WS_2 NT and the W-tips, the nanotube-tip 2 contact region was irradiated for increasing time intervals, using the electron beam of the SEM ($10\ keV$, $10\ pA$). The I-V characteristics changed as shown by the coloured curves of Figure (3.9 c). Although the qualitative behaviour of the device remained the same, a clear enhancement of the current was detected with the increasing irradiation time up to 20 min. After 30-minute total irradiation, we observed only a negligible increase of the current.



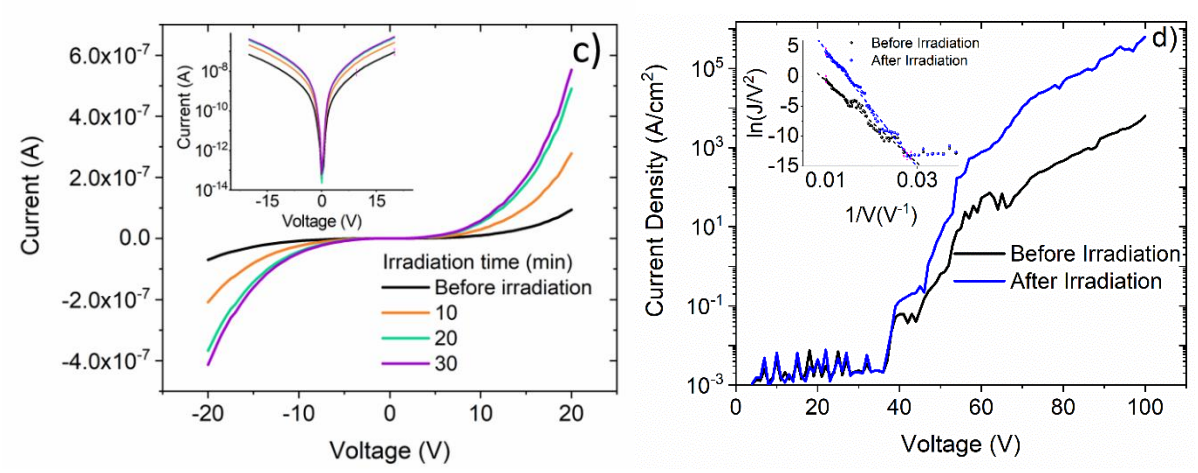


Figure 3.9 - a) SEM image showing bundles and individual NTs attached to W-tip 2. A single, long NT, held between tips 1 and 2 by van der Waals forces, is used for electrical measurements. b) SEM image of the configuration adopted for field-emission characterization with the single NT detached from tip 1, which is used as the anode. The inset shows a magnification of the tip 1 and the nanotube-tip region. c) I-V characteristic recorded for different irradiation times. The inset shows the experimental data on logarithmic scale. d) Field emission current density as a function of the applied voltage recorded before and after 30 minutes irradiation. The inset shows the linear fit of the FN plot used to estimate the field enhancement factors.

At this point, field emission characterization, one of the main purposes of this experiment, was carried out. To do that, tip 1 was detached and moved away from the WS_2 NT edge, at a distance $d \sim 400\ nm$. The measurements were repeated both before and after the e-beam conditioning of the WS_2 NT-tip 2 contact (Figure (3.9 b)). The applied voltage was ramped from 0 to 100 V (a constraint imposed to avoid damage of the device and the measurement setup) while monitoring the current. The black curve of Figure (3.9 d) shows that, before irradiation, the current density J, obtained as the ratio between the measured current and the nanotube section area, is below the $\sim 10^{-2}\ \frac{A}{cm^2}$ noise floor for $V \leq 38\ V$, while for higher voltage an exponential increase of the current

density is observed, up to a maximum value of $\sim 6\frac{kA}{cm^2}$. After 30 minutes total irradiation time of the WS_2 NT-tip 2 contact, the field emission current density increases reaching a maximum value of $\sim 600\frac{kA}{cm^2}$, as shown by the red curve in the same figure.

3.2.5 Fowler-Nordheim analysis

To confirm the field-emission nature of the measured currents, the $J-V$ curves are analysed in the framework of the classical Fowler-Nordheim (FN) theory.[206] Equation (3.1) was used to describe the current behaviour and the same slight deviation from the classical model made in the case of the Ga_2O_3 nanopillar, i.e. considering that the applied electric field as $\frac{V}{kd}$, where $k \approx 1.5$ is a corrective factor, has been taken into account to consider the spherical termination of the W-tip.[254] Moreover, also in this case the sharp shape of the nanotube causes the accumulation of the field lines at its end, resulting in an amplification of the local field, so also the field enhancement factor β needs to be considered. The typical field emission figures of merit were obtained following the procedures described in the previous paragraph. Before irradiation, it was obtained $\beta \sim 65$, turn-on field $E_{on} \sim 100\ V/\mu m$ and $J_{MAX} = 6\frac{kA}{cm^2}$ while after 30 min irradiation on tip 2 contact $\beta \sim 50$, $E_{on} \sim 100\ V/\mu m$ and $J_{MAX} = 600\frac{kA}{cm^2}$. The slight reduction of the field enhancement factor is likely due to the removal of surface adsorbates from the nanotube tip by Joule heating during the first sweep. Generally, these adsorbates act as accumulation points for the electrical fields lines further increasing the local electric field. The study on the field emission properties of WS_2 NTs follows a pioneering study[245] which showed that WS_2 NTs can be a potential candidate for vacuum nanoelectronics and flat panel display applications. In that work the authors demonstrated that free-standing WS_2 NTs protruding on top of silicon microstructures are efficient cold emitters. Here it has been demonstrated that the electron beam irradiation of the contact area can highly increase

the maximum current density. Indeed, J_{MAX} is increased by a factor 100 after irradiation and is higher or comparable to the maximum current density of others well-established field emitters, such as Mo tips,[255] bare and metal coated Si tips,[256] carbon nanotubes,[201,257] MoS_2 nanoflowers,[258] graphene or graphene-like nanosheets.[259–261]

3.2.6 The effects of electron irradiation

In the previous section the effects of electron irradiation on the transport properties have been reported. In this section such effects are depth and their causes are investigated. To understand the effects of the e-beam irradiation, the device can be divided into three resistive elements, as shown in Figure (3.10 a). R_{C1} and R_{C2} indicate the contact resistance of the NT with tip 1 and tip 2, respectively, while R_3 is the intrinsic resistance of the WS_2 NT. The total resistance, referred to as R_{tot}, is given by the sum of the three components:

$$R_{tot} = R_{C1} + R_{C2} + R_3 \qquad (3.2)$$

Since up to this phase of the experiment the NT contact with tip 2 was the only one irradiated, R_{C2} is the unique resistance improved by e-beam. However, as can be seen from Equation (3.2), a reduction of one of the three resistances affects the total resistance leading to the experimentally observed increase of the device current. R_{tot}, estimated from low bias part ($|V| < 5\ V$) of the I-V curves of Figure (3.9 c), exhibits an exponential decrease with increasing electron fluence (Figure (3.10 b)).

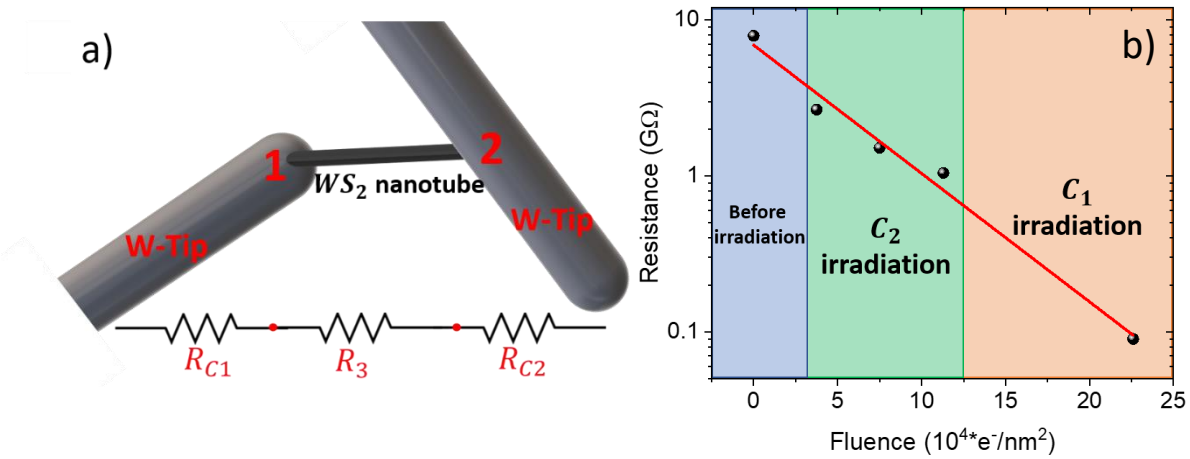


Figure 3.10 - a) Modelling of the tip 1-WS_2 NT-tip 2 device. R_{C1} and R_{C2} indicate the two resistances at the interface between the nanotube and the W-tips, while R_3 is the nanotube intrinsic resistance. b) Measured total resistance as function of the electron fluence on the two exposed area. The red line represents the exponential fit.

The main effect of electron irradiation is a physical modification of the WS_2 NT-tip 2 contact. Indeed, since the pressure inside the SEM chamber is about $10^{-6}\,Torr$ some residual hydrocarbon molecules are present inside it. Such molecules are decomposed under the electron beam irradiation resulting in carbonaceous material across the exposed area.[236,262–264] This carbonaceous material acts as a glue which strengthen the contact between the nanotube and the tip and reduces the contact resistance. Before the electron beam exposure, contact is only due to van der Waals forces with a mean bonding distance of several angstroms.[265] This contact is unstable, and vibrations of the measuring apparatus can cause a further increase of NT-tip distance. The carbonaceous deposit at the junction introduces an additional mechanical stability, which allows a more effective interaction between the NT and the tip, resulting in the reduction of R_{tot}. Moreover, the electron irradiation facilitates, via local annealing, the removal of unavoidable residual surface

adsorbates, such as water, nitrogen, and oxygen, that can contribute to the global resistance of the device. The experimentally observed negligible increase of the current after 30 minutes irradiation is due to the saturation of both the described mechanisms. Indeed, after a certain time, the beam-induced deposit is not expected to further contribute to the mechanical stability of the NT/tip junction, leading only to a progressive growth of the carbonaceous deposit. The e-beam effect on R_{tot} is corroborated by the field-emission measurements. Indeed, while the turn on field and the field enhancement factor, which are mainly related to the intrinsic WS_2 properties, are the same before and after electron beam irradiation, the maximum current density increases by two orders of magnitude after electron beam exposure, highlighting the effect of the reduction of R_{tot}.

To further decrease R_{tot}, we irradiated the WS_2 NT-tip 1 contact for 30 minutes obtaining another order of magnitude lowering, as shown in Figure (3.10 b). The presence of carbonaceous material at the contact region is evident in the SEM images shown as inset in Figure (3.11 a).

3.2.7 Electrical response to mechanical stress

Once the effects of irradiation are understood, the research has focused on another important property of NTs, their electrical response when subjected to mechanical stress. The measurements were carried out taking advantage from the stronger WS_2 NT-tip adhesion. Tip 1 was moved stepwise, using the piezo-driven controller of the tip. The evolution of the stretching process is shown in Figures (3.11 a-f). Starting from an initial length of $9.200\ \mu m$, the WS_2 NT was stretched until breaking after 20% elongation of its initial value, corresponding to a length of $10.995\ \mu m$ as shown in Figures (3.11 a-f), highlighting a high axial strength. From Figure (3.11 f), it is clear that the sum of the lengths of the two nanotube fragments obtained after breaking is greater than the initial length of the nanotube. This indicates that the breaking occurs well beyond the elastic limit, after a phase of plastic deformation of the nanotube in which sliding of walls with respect to each other

could occur. For this reason, in the study of the piezoresistive response reported below, the trend was limited to 12% elongation, i.e. to the elastic regime for WS_2 nanotubes, consistently with previous experimental results and theoretical calculations.[236]

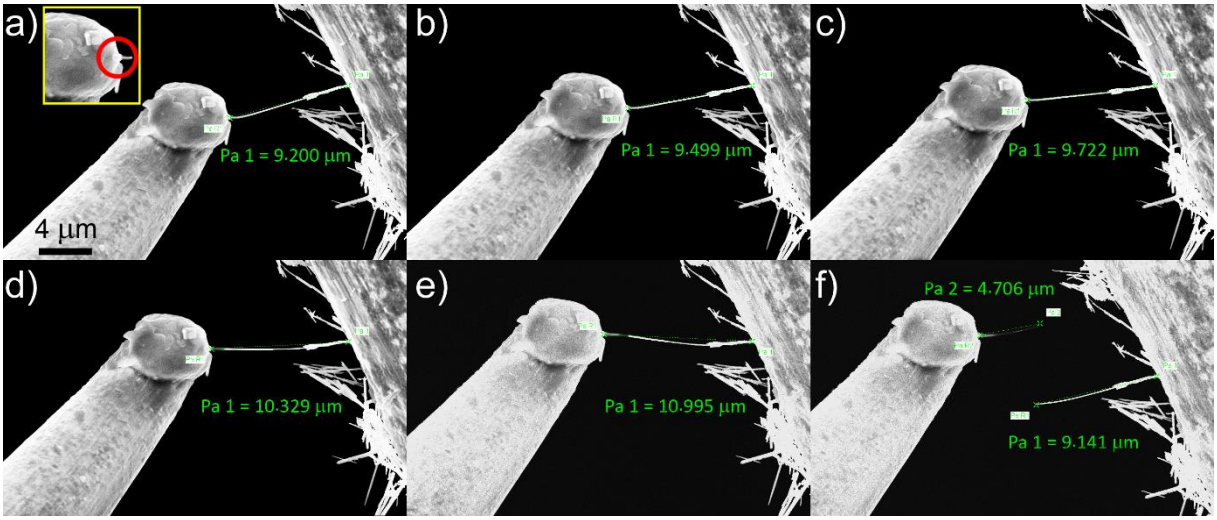


Figure 3.11 - a-f) SEM images of the elongation process of the WS2 NT. The strain is obtained moving tip 1 to the left of the image. The initial NT length (figure a) is $9.200\ \mu m$ *while the final length before NT rupture (figure e) is* $10.995\ \mu m$*. The inset in figure 5a shows a magnification of the NT-tip 1 area in which the presence of the carbonaceous deposit, circled in red, is clearly visible.*

Figure (3.12 a) shows the I-V characteristics of the WS_2 NT recorded for every stretching step. The device current decreases when the strain increases. The last detectable signal is recorded at 12% elongation, while the current falls below the noise floor level when the nanotube is extended by 20% of its initial length. It has been reported in literature that the stress–strain plot of an individual WS_2 NT has a linear trend until the nanotube rupture at 14% elongation.[236] This feature indicates that WS_2 nanotubes deform elastically making it possible to know the applied stress, σ, from the

measurement of the nanotube deformation, $\varepsilon = \frac{L_f - L_i}{L_i}$, through the equation $\sigma = E\varepsilon$, where L_f and L_i are the final and the initial lengths of the nanotube and $E = 171\ GPa$ is the Young's modulus.[266]

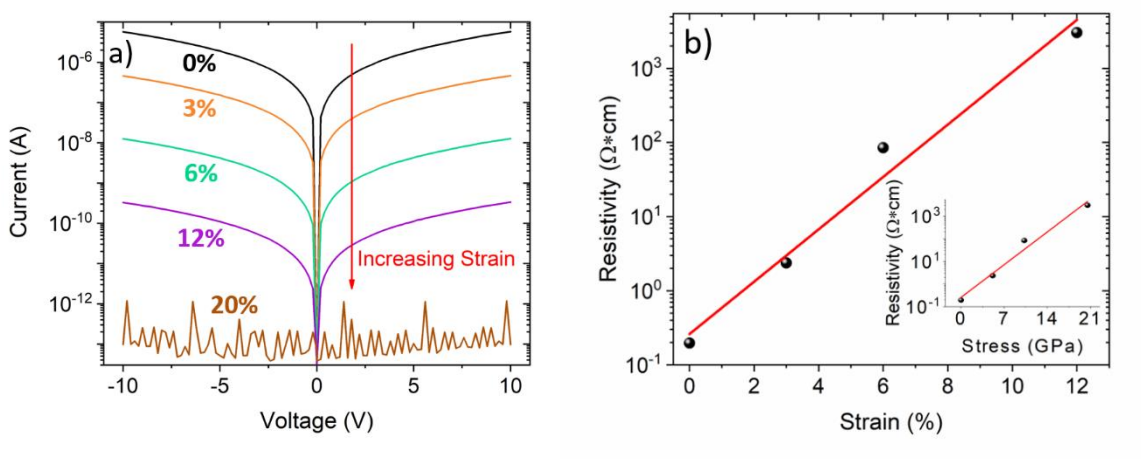


Figure 3.12 - a) I-V characteristics of the individual WS_2 NT for each elongation step. The black curve represents the I-V for the unstrained NT, while the brown line is the noise floor. b) Resistivity as function of the strain with exponential fit (red line). The inset shows the measured resistivity as function of the applied stress with the exponential fit.

Figure (3.12 b) shows the WS_2 NT resistivity (ρ) versus strain. The resistivity is obtained as $\rho = R_T \frac{A}{L}$, where R_T is the resistance measured from the low-bias I-V curves, A is the nanotube section area and L is its length. The plot shows an exponential growth of the resistivity as function of the strain. The large variation of resistance with stress enables the use of WS_2 NTs as piezoresistive sensors. Although the contribution of the contact resistances is included, this strong dependence is likely dominated by the WS_2 nanotube, indicating an increasing NT resistivity with growing tensile strain. Indeed, as shown in Figure (3.11), no apparent change is observed at the NT-tip contacts, owing to the e-beam strengthening effect, while the NT is stretched. Moreover, a similar behaviour has been already reported for carbon nanotubes.[267,268] According to a recent theoretical study,[246] the

bandgap of WS_2 NTs decreases with the tensile strain, which could induce a reduction of the resistivity. However, the study refers to an ideal single wall NT with well-defined chirality and does not consider inter-layer interaction of layers with different chirality and diameter in real multi-walled NTs. Indeed, it was shown that the chirality, diameter and number of layers strongly influence the electronic structure of bent layered nanostructures.[221,223,246]

Additionally, the incommensurate stacking of WS_2 layers stimulates the ''locking'' between the layers and therefore facilitates the elongation of the nanotube as a whole.[239] This results in collective influence of all layers on the band gap and resistivity.

In another study, it was shown that under specific conditions the outer walls could slide over the inner ones,[237] and this option also should be taken into account. Moreover, structural imperfections in the real nanotubes could induce further defects upon the application of a tensile stress.

Although the physical mechanisms that cause the observed increase of resistivity are not clear yet, the strong dependence of the resistivity on the tensile strain, up to 12%, is a unique feature of WS_2 nanotubes. For comparison, CNTs are only studied in $0-1\%$ strain range.[269,270] The observed electrical response over a wide range of strain makes WS_2 nanotubes suitable as piezoresistive strain sensors.

3.3 Summary

In summary, in this chapter two studies have been reported concerning the electrical properties of two 1D materials, such as Ga_2O_3 nanopillars and WS_2 nanotubes. The obtained results showed that both materials are excellent candidates for the realization of practical field emitting devices thanks to their remarkable figures of merit.

Specifically, in the first paragraph the fabrication of nanopillars with $400\,nm$ height and $70\,nm$

diameter from $\beta - Ga_2O_3$ single crystals using Ne^+ ion milling is reported. The field emission properties of such nanopillars were experimentally investigated using a tip-shaped anode with fine movement control. The main result of this research was the achieving of a stable field emission current, with a high current density over $100\ A/cm^2$, well described by the standard Fowler-Nordheim theory, with a turn on field of $30\ V/\mu m$. The field enhancement factor was found to be a linear function of the distance and achieves the remarkable value of about 200 at $1\ \mu m$ distance. The turn-on field and the β factor could be further improved by sharpening the nanopillar tip. This study shows that $\beta - Ga_2O_3$ nanopillars are suitable candidates for field emission applications and, if appropriately patterned, can compete with well-established emitters such as carbon nanotubes.

Then, in the second paragraph, the fabrication of multi-walled WS_2 NTs and their electrical characterization under electron beam irradiation and axial tensile strain is reported. This study demonstrated that electron beam exposure can be used to improve the quality of the nanotube-electrode contacts, leading to a reduction of the contact resistance through mechanical stabilization. A field emission current, achieving the high current density of $600\frac{kA}{cm^2}$, with turn on field $\sim 100\frac{V}{\mu m}$ and field enhancement factor ~ 50, has been reported. Finally, it was demonstrated that individual WS_2 nanotubes can be suitable for piezoresistive strain sensors as they can withstand over 12% strain without rupture and their resistivity exponentially increases with strain, similarly to what has been observed for carbon nanotubes.

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