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Exploring 2D van der Waals heterostructures for advanced electronic and optoelectronic applications

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ABSTRACT

As silicon-based semiconductor technology approaches its fundamental scaling limits, the exploration of low-dimensional materials has become imperative for the next generation of electronic and optoelectronic systems. This thesis investigates the fabrication, electrical, and optoelectronic properties of two-dimensional (2D) van der Waals (vdW) heterostructures and one-dimensional (1D) nanostructures, demonstrating their potential to overcome the constraints of traditional Moore and More Moore paradigms. The research first addresses the challenges of material stability and contacts resistance in black phosphorus (bP). By implementing optimized capping strategies and contact engineering, bP-based devices were fabricated, exhibiting high carrier mobility (on the order of 10^2 cm^2 V^{-1} s^{-1}). When combined with MoS_2 in a staggered type-II heterojunction, the system enables self-powered photovoltaic operation, with an open-circuit voltage of 75 mV and short-circuit current of 0.12 nA, and significantly accelerated charge carrier extraction, reducing relaxation time constants compared to isolated MoS_2 layers. To ensure environmental robustness, the study explores WS_2 and $PdSe_2$ devices and their combination. WS_2/$PdSe_2$ heterostructures demonstrate a remarkable multifunctionality, serving as air-stable visible-light photodetectors and optoelectronic pressure sensors. The WS_2/$PdSe_2$ heterostructures achieve response times an order of magnitude faster than individual WS_2 devices because of the high mobility of $PdSe_2$. Furthermore, the exploitation of persistent photoconductivity (PPC) allowed for the emulation of biological synaptic plasticity, with paired-pulse facilitation (PPF) and post-tetanic potentiation (PTP) indexes reaching 140% and 300%, respectively. Addressing the critical scarcity of stable p-type 2D materials, this work investigates an innovative p-doping strategy for $MoSe_2$ via interfacial coupling with the antiferromagnetic insulator CrOCl. This approach enables the realization of high-performance complementary field-effect transistor architectures and lateral homojunctions exhibiting anti-ambipolar transport. These homojunctions were successfully implemented into resistive-load and CMOS inverters (gain ≈ 1.2, total noise margins ≈ 70%), alongside with floating-gate non-volatile multilevel memories capable of mimicking biological action potentials. Additionally, optoelectronic characterization across the pristine and p-doped $MoSe_2$, as well as the $MoSe_2$ homojunction, revealed a stable, linear photoresponse and a distinct photovoltaic effect within the $MoSe_2$ homojunction, enabling autonomous, self-powered photodetection. Finally, the transition to 1D nanostructures highlights the role of dimensionality. WS_2 nanotubes were found to exhibit intrinsic ambipolarity and enhanced self-powered photodetection due to curvature-induced strain, while InAs nanowire inverters served as a high-mobility platform for 1D logic circuits. Thus, this thesis demonstrates that vdW engineering and dimensionality control provide a versatile framework for integrating logic, memory, and neuromorphic computing into simplified, high-performance, and multi-modal electronic platforms.

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INTRODUCTION

Silicon has been the cornerstone of semiconductor technology for decades, enabling continuous progress in device performance through the progressive miniaturization of field-effect transistors (FETs). In the so-called post-Moore's law era, as silicon approaches the physical and practical limits of scaling, the exploration of alternative materials and innovative strategies has become essential.[1–3] Two-dimensional (2D) materials, with their angstrom-scale thickness, dangling-bond-free surfaces, high charge carrier mobility, and favourable thermal properties at sub-nanometre scale, are promising candidates for next-generation electronic devices. Despite the intensive efforts dedicated to the implementation of 2D materials in electronics, the transition from silicon to 2D-based technology still faces significant challenges. In particular, their integration with existing silicon platforms remains one of the main goals of industrial research in this field.[4–6] The realization of high-speed and high-performance electronic devices relies on several factors, including the optimization of device architecture, minimization of contact resistance, fabrication of defect-free, high-quality flakes, and the identification of appropriate gate oxide materials.

In the last decades, the combination of 2D materials to form van der Waals (vdW) heterostructures has attracted increasing attention. The absence of dangling bonds on 2D material surfaces and the weak vdW interactions between adjacent layers enable the fabrication of advanced functional devices without the constraints of lattice matching. Such 2D heterostructures broaden the range of accessible bandgaps and offer new strategies for the realization of novel devices. They can be integrated into electronic, optoelectronic, photovoltaic, and valleytronic systems, enabling efficient architectures for data storage, communication technologies, and power electronics. Moreover, the unique interfacial properties of 2D heterostructures enhance their potential for achieving universal electrical contacts that can mitigate the electrical mismatch between different phases and dimensionalities of matter, for instance at organic-inorganic interfaces, bio-inspired or artificial synaptic contacts, and 1D/2D/3D heterointerfaces.[7]

This thesis explores the fabrication, electrical and optoelectronic characterization of 2D vdW heterostructures, highlighting their transformative potential in electronics, photovoltaics, sensing, and neuromorphic computing. The first chapter establishes the theoretical foundation for this work by introducing the broad family of 2D materials and their unique role in post-Moore's law era. After discussing the fundamental properties of specific crystals, ranging from group-VA elements like black phosphorus (bP) to various transition metal dichalcogenides (TMDs), the chapter provides a state-of-the-art overview of 2D materials-based FETs. A dedicated section also addresses the formation of heterojunctions and homojunctions. By analysing various device architectures and band-alignment models, this section provides the necessary framework to understand how these interfaces are implemented in the advanced practical applications discussed throughout this research. The second chapter establishes the experimental framework of this work, detailing the material synthesis and fabrication procedures utilized for realizing the devices analysed in this thesis. Much of the device processing and nanofabrication was carried out during dedicated research stays at international facilities, allowing for the implementation of advanced fabrication techniques. This chapter also provides a comprehensive description of the characterization techniques and specialized measurement setups employed for the electrical and optoelectronic investigations discussed in the subsequent chapters, the results of which have been published in peer-reviewed journals and

presented at international conferences, as detailed in the last Section *Publications* and *International conferences*.

In the third chapter, the results on bP-based FETs are reported, focusing on the optimization of contact resistance and the development of a capping strategy to prevent material oxidation.[8,9] The electrical and optoelectronic characterization of the devices is carried out under different conditions, and potential applications such as non-volatile memory devices and photodetectors are discussed.[10–12] Following the investigation of bP properties, it is combined with molybdenum disulphide (MoS_2), which is one of the most widely studied materials among TMDs, to form staggered bP/MoS_2 heterojunctions. These heterostructures are electrically characterized under varying illumination conditions, and their potential for photovoltaic applications is also explored.[13–16]

Building upon the investigation of bP/MoS_2 heterostructures presented in the previous chapter, the fourth chapter seeks to address one of the primary challenges in 2D electronics: achieving high-performance optoelectronic functionality without compromising environmental stability. While bP exhibits high charge carrier mobility and tunable bandgap, its rapid degradation under ambient conditions necessitates complex encapsulation techniques. The fourth chapter transitions to a more chemically robust material platform by exploring tungsten disulphide (WS_2) and palladium diselenide ($PdSe_2$) FETs, as well as vdW WS_2/$PdSe_2$ heterostructures. The electrical characterization of individual WS_2 and $PdSe_2$ devices is first discussed, together with their photoresponse under different ambient conditions. Subsequently, the vdW WS_2/$PdSe_2$ heterostructures are electrically characterized under varying pressure, both in the dark and under illumination, and the results are compared with those obtained from the single-flakes devices. Finally, the WS_2/$PdSe_2$ heterostructures are evaluated as optoelectronic pressure sensors, visible-light photodetectors, and optoelectronic synaptic devices.[17,18]

In the fifth chapter, a floating-gate complementary FET based on molybdenum diselenide ($MoSe_2$) is investigated. The electrical and optoelectronic responses of a pristine $MoSe_2$ FET, exhibiting n-type conduction, and a p-doped $MoSe_2$/CrOCl FET are analysed. The behaviour of the homojunction formed between the pristine and p-doped $MoSe_2$ is also examined. This device architecture enables the implementation of logic gates, such as a resistive-load inverter and a CMOS inverter, by combining n-type and p-type transistors. Additionally, the optoelectronic properties of the individual pristine and p-doped $MoSe_2$ devices, as well as of their combination, were thoroughly explored, showing a linear photoresponse as a function of incident optical power and a peak responsivity at 780 nm, consistent with the excitonic transitions of $MoSe_2$. Notably, the strong built-in potential at the p-n interface enabled self-powered photovoltaic operation, allowing for efficient photodetection without external bias, with I_{sc} that reach up to 1 nA. Furthermore, the integration of a floating gate enables non-volatile memory functionality by exploiting controlled charge trapping and storage. Additionally, the application of consecutive short voltage pulses, mimicking action potentials, allows for the incremental tuning of the channel conductance, thereby emulating synaptic plasticity in biological synapse.

Finally, the sixth chapter explores the transition from 2D layers to one-dimensional (1D) nanostructures, investigating how the reduction in dimensionality affects electronic transport and device functionality. This chapter focuses on two distinct 1D systems: WS_2 nanotubes (NTs) and

Indium Arsenide (InAs) nanowires (NWs). The first section analyses WS_2 NTs, providing a direct comparison to the planar WS_2 sheets discussed in Chapter 4; here, the cylindrical geometry and curvature-induced strain lead to unique electronic properties, including intrinsic ambipolar conduction and potential for self-powered photodetection.[19] The second section investigates InAs NWs as a high-mobility fundamental blocking for 1D electronics. After exploring their thermal stability and electrical performance across a wide temperature range, InAs NWs are implemented into resistive-load inverters.[20,21] This allows for a critical performance evaluation of 1D logic circuits in comparison to the 2D $MoSe_2$-based inverters developed in Chapter 5, highlighting the performance of 1D architectures for post-Moore's law digital technology.

1. TWO-DIMENSIONAL MATERIALS AND DEVICES

Nanomaterials represent a transformative frontier in condensed matter physics and electronic engineering, providing a paradigm-shifting pathway to transcend the fundamental scaling and performance limits of conventional bulk semiconductor systems. As material dimensions are reduced to the nanoscale, the emergence of quantum confinement effects and the increasing dominance of surface-mediated phenomena lead to fundamental variations in the electrical, chemical, and optical profiles observed in 3D crystals.

This chapter establishes the theoretical and material-science foundation required to understand the devices fabricated and characterized in this thesis. It begins with the fundamental properties of individual 2D materials, moves through the physics of FETs, and concludes with an exploration of the emerging applications that exploit these low-dimensional systems for logic gates, memory, and sensing.

1.1 Fundamental properties of 2D materials

Since the isolation of graphene in 2004, 2D materials have emerged as a unique class of crystals characterized by exceptional light-matter interactions, a high surface-to-volume ratio, and an inherently dangling-bond-free surface. While graphene serves as a prototypical 2D system, its lack of a primary bandgap has necessitated the exploration of alternative layered materials. This has led to the intensive study of bP, with its high carrier mobility and anisotropic transport, and the vast family of TMDs, which provide a wide range of tunable bandgaps suitable for next-generation electronic and optoelectronic devices.[22]

The defining characteristic of these materials lies in their structural anisotropy, where atoms within a single layer are connected by strong covalent bonds, while the individual layers are held together by weak vdW forces. Unlike traditional 3D semiconductors, where broken covalent bonds at the surface result in dangling bonds that act as charge traps, the surfaces of 2D flakes are inherently passivated and chemically inert. This unique bonding nature allows for the mechanical isolation of single atomic layers through different exfoliation strategies. More importantly, it enables the artificial assembly of disparate 2D crystals into vdW heterostructures. Considering that these layers are not constrained by the rigid requirements of lattice matching, 2D materials with different lattice constants and symmetries can be vertically stacked, creating designed materials with tailored band alignments and synergistic properties that do not exist in nature.

1.1.1 Graphene

Graphene was first isolated in 2004 by Andre Geim and Konstantin Novoselov, a discovery for which they were awarded the Nobel Prize in Physics in 2010.[23,24] Obtained through the mechanical exfoliation of bulk graphite, a single sheet of graphene consists of carbon atoms arranged in a 2D hexagonal honeycomb lattice. Within this plane, each atom is covalently bonded to three neighbours with a C-C bond length of 0.142 nm. The strength of these sp^2-hybridized covalent bonds, known as σ-bonds, endows graphene with exceptional mechanical robustness and thermal conductivity.[25] The remaining fourth valence electron occupies a p_z orbital oriented perpendicular to the plane. These orbitals hybridize to form delocalized π and π^* bands that extend across the entire lattice, governing the material's electronic properties and providing a pathway for highly mobile charge carriers.[26,27]

The graphene lattice comprises two interpenetrating triangular sublattices shifted with respect to each other, defining its honeycomb geometry (see Figure 1.1a). This unique symmetry dictates its electronic band structure, first modelled in 1947 using the tight-binding approximation.[28] As illustrated in Figure 1.1b, the energy dispersion relation of graphene is characterized by the meeting of the conduction and valence bands at six corners of the first Brillouin zone. Near these Dirac points (K and K'), the dispersion relation is linear rather than parabolic, meaning the carriers behave as massless Dirac fermions. In its pristine, undoped state, the Fermi level (E_F) lies precisely at the Dirac point (Figure 1.1c), resulting in a zero-gap semimetal behaviour. While this gapless nature enables ambipolar transport and easy tuning of carrier density via electrostatic gating, it presents a significant challenge for digital logic. The lack of an energy bandgap prevents the device from reaching a true off state, leading to low on/off current ratios that hinder graphene's direct application in conventional complementary-metal-oxide-semiconductor (CMOS) logic gates.

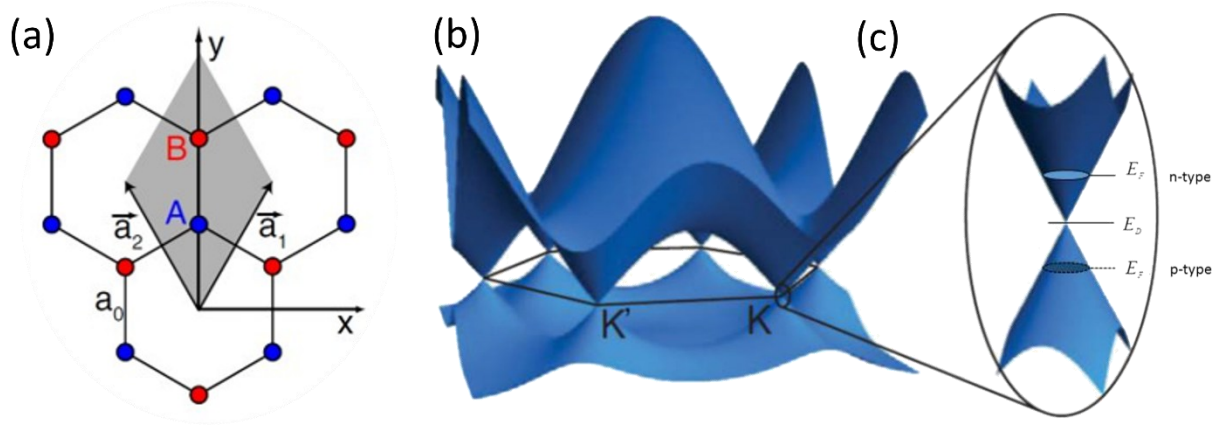


Figure 1.1: (a) Hexagonal lattice structure of graphene. The blue and red circles indicate the atoms belonging to the two sublattices, labelled as A and B. (b) Three-dimensional band structure of graphene. (c) Zoom of a Dirac cone near the K Dirac point. E_D indicates the intrinsic Fermi level; its shift for the n-type or p-type conduction is displayed. Reproduced with permission from Elsevier.[27]

1.1.2 Black phosphorus

The absence of an electronic bandgap in graphene has stimulated the search for 2D materials with semiconducting properties. Among these, bP also exhibits a layered structure and has attracted considerable attention as a promising candidate for electronic and optoelectronic applications. BP was first synthesized by Percy Williams Bridgman in 1914 through the conversion of white phosphorus under a pressure of 1.2 GPa and at a temperature of 200 °C. Following the discovery of graphene, bP was rediscovered in 2014 as a layered material that can be exfoliated down to a single atomic layer.[29] Each layer of this material is composed of phosphorus atoms that are strongly bonded in plane forming layers that are stacked together by vdW interactions, with an interlayer spacing of 0.53 nm. The lattice constants along the main three directions are a = 4.47 Å (armchair), b = 3.34 Å (zigzag), and c = 10.71 Å (interlayer). Phosphorus atoms have five valence electrons with a valence shell configuration $3s^2 3p^3$. Among these five electrons, three of them are involved in bond with other atoms, while the remaining two electrons form a lone pair. The three bonds are not in the same plane because of their repulsion by the lone pair on each atom. Such atomic structure resembles the one of graphite with the difference that the atomic rings in bP layers exhibit a puckered structure, yielding strongly anisotropic in-plane properties. Figure 1.2a shows the orthorhombic crystal structure of bP, highlighting the localization of atoms on two different planes. Figure 1.2b-c show the

band structure of bulk and monolayer bP, respectively.[30,31] This material exhibits a direct bandgap that ranges from 0.3 to 2 eV. The nonzero and tunable bandgap of bP enables its use in FETs and optoelectronic applications. However, similar to the bandgap, the electrical properties of bP strongly depend on its thickness. The puckered honeycomb lattice of bP results in a significant breaking of in-plane symmetry, distinguishing it from the isotropic hexagonal lattice of graphene or other 2D materials. Along the armchair direction, the atoms follow a corrugated path, whereas along the zigzag direction, the atoms are arranged in a more rigid, linear way. This structural asymmetry leads to a strong in-plane anisotropy in the effective masses of charge carriers, which in turn manifests as direction-dependent carrier mobility and thermal conductivity.[32] Furthermore, bP exhibits a highly anisotropic optical response due to its linear dichroism. The absorption of light is strongly dependent on the orientation of the incident electric field relative to the crystal axes. Specifically, the optical transmissions are allowed when the light is polarized along the armchair direction and forbidden, or significantly suppressed, along the zigzag direction. This property allows for the fabrication of polarization-sensitive photodetectors and optical modulators without the need of external polarizing filters, making bP a unique platform for integrated optoelectronic systems that require orientation-selective sensing.

The practical use of bP is hindered by its instability under ambient conditions. In the presence of oxygen and water, bP gradually oxidizes, leading to structural degradation and a significant reduction in its electrical and optical performance. To gain insight into the degradation process mechanism, Wang et al.[33] studied the interaction of O_2 and H_2O with phosphorene by means of density functional theory calculations combined with first-principles molecular dynamics simulations. They reported that the pristine bP surface is hydrophobic, a property that was later confirmed experimentally by Huang et al.[34] The formation of phosphorus-oxygen bond is favoured by the lone electron pairs on each phosphorus atom, arising from its sp^3 hybridization. Upon oxidation, the bP surface becomes more hydrophilic, enhancing its interaction with H_2O molecules and accelerating the degradation process, which eventually leads to the decomposition of the material. Given the strong tendency of bp to degrade under ambient conditions, the development of effective protection strategies has become crucial to preserve its intrinsic properties and ensure its suitability for electronic applications.

To enable the use of bP in electronic devices, it is essential to protect the material from oxidation by isolating it from air and moisture. Various strategies have been developed to improve its stability, including encapsulation, chemical functionalization, solvent-based passivation, and polymer incorporation. Encapsulation with dielectric materials such as SiO_2 and Al_2O_3 effectively delays degradation, although the protection efficiency depends on the thickness and quality of the deposited layers.[35–37] Two-dimensional materials like hexagonal boron-nitride (hBN), graphene, and MoS_2 have also been employed as capping layers, providing chemical inertness and impermeability to oxygen, but their manual transfer processes limit large-scale applicability. Chemical functionalization offers another route to passivate bP surfaces: covalent functionalization provides robust protection but can alter the material's intrinsic properties, whereas noncovalent functionalization preserves them through vdW interactions. Solvent-based methods, particularly those using ionic liquids, improve the lifetime of liquid-exfoliated flakes by preventing oxidation during processing.[38] Among the proposed approaches, polymer-based protection has shown significant promise for laboratory-scale research and device prototyping. Encapsulating bP with

polymers such as poly(methyl methacrylate) (PMMA) immediately after exfoliation provides a physical barrier that effectively inhibits the diffusion of oxygen and water molecules to the bP surface. This strategy not only enhances environmental stability but also maintains the transparency required for optical characterization and remains compatible with standard lithographic processes. Furthermore, PMMA coatings can be selectively removed or patterned, offering a versatile platform for investigating bP's intrinsic properties across various device architectures.[39,40] Consequently, polymer-based encapsulation represents a key strategy for the realization of stable, high-performance bP FETs, as explored in the experimental sections of this work.

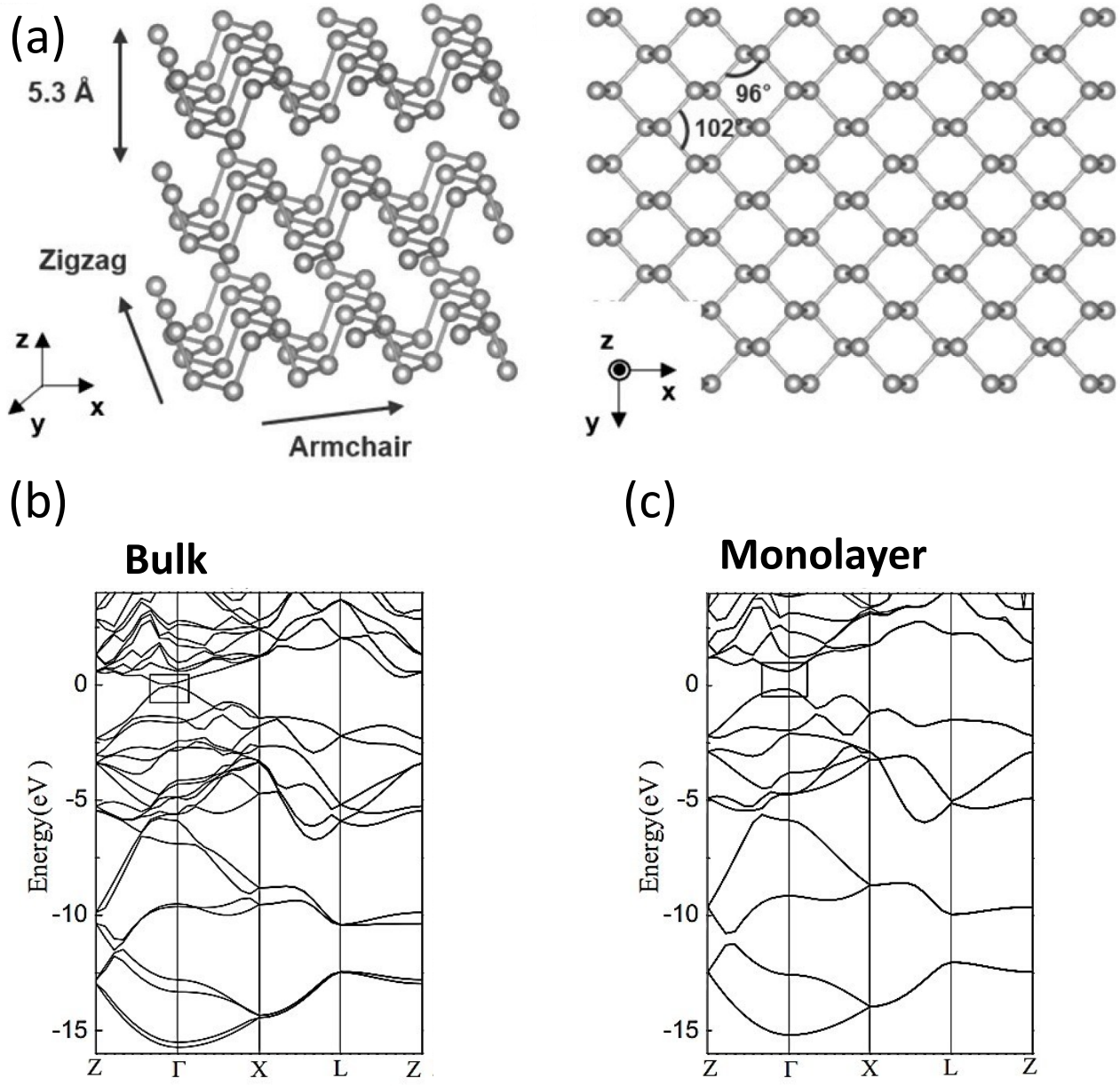


Figure 1.2: (a) Atomic structure of phosphorene. Band structure of (b) bulk and (c) monolayer bP. Reproduced with permission from AIP Publishing.[41]

1.1.3 Transition metal dichalcogenides

Two-dimensional TMDs represent a versatile class of materials with the general formula MX_2, where M is a transition metal atom (e.g. Mo, W, Pd) and X is a chalcogen atom (S, Se, Te). Structurally, each

monolayer consists of a plane of metal atoms covalently sandwiched between two planes of chalcogen atoms. The structure is characterized by strong intralayer covalent bonds and weak interlayer vdW interactions. This structural arrangement results in a unique combination of atomic-scale thickness, high surface-to-volume ratio, and remarkable mechanical and electronic properties, making TMDs ideal candidates for next-generation nanoelectronics, nanophotonics, sensing, medicine, and neuromorphic computing.[42]

The electronic behaviour of TMDs is intrinsically linked to their structural polymorphs, which depend on the coordination environment of the transition metal atoms. Bulk TMDs can exist in various polymorphs, such as hexagonal (2H), trigonal (1T), and rhombohedral (3R) forms. The two most prominent phases in monolayer TMDs are the trigonal prismatic (2H) and the octahedral (1T) coordination. Depending on the particular combination of transition metal and chalcogen elements, the thermodynamically stable phase can be either the 2H or the 1T phase, and the other can generally be obtained as a metastable phase. For the most well-known TMDs (MoS_2, WS_2), the 2H phase is thermodynamically stable, while the 1T phase is metastable. These polymorphs can be understood as different stacking arrangements of the three atomic planes (chalcogen – metal – chalcogen) that constitute each individual layer. In the 2H phase (ABA stacking), chalcogen atoms in different atomic planes occupy equivalent positions and are aligned on top of each other along the direction perpendicular to the layer. In contrast, the 1T phase exhibits an ABC stacking order, where atoms occupy different positions in successive planes (see Figure 1.3). In multilayer or bulk TMDs, the overall structure is determined by the stacking arrangement of the individual layers and may exhibits distortions that reduce the lattice periodicity. These distortions can lead to the formation of metal-metal bonds which originated from the dimerization of the 1T phase in group VI TMDs.

The chemical composition and structural phase of TMDs give rise to a wide variety of electronic behaviours, ranging from metallic to semiconducting and even correlated or topological phases. The 2H phase generally exhibits semiconducting properties with thickness-dependent bandgaps, from 1 to 3 eV, whereas the 1T phase is metallic and strongly hydrophilic. As the layer number decreases, bulk TMDs with an indirect bandgap transform into direct bandgap semiconductors, enabling efficient light emission and optoelectronic applications. Owing to their tunable electronic properties, TMDs are promising materials for transistors, sensors, and energy-related devices such as electrocatalysts, supercapacitors, and batteries. Similar to graphene, the valence band maximum and conduction band minimum of TMDs are located at the corners of the hexagonal Brillouin zone, giving rise to valley-dependent phenomena relevant for valleytronics. Furthermore, the lack of inversion symmetry in 2H-TMDs, combined with strong spin-orbit coupling, induces spin splitting of the electronic bands, opening new perspectives for spintronic device design without the use of magnetic materials. While the Mo- and W-based TMDs are the most widely explored, the family also includes more complex systems like $PdSe_2$, which exhibits a pentagonal structure and high air-stability, further expanding the accessible range of electronic properties investigated in this work.

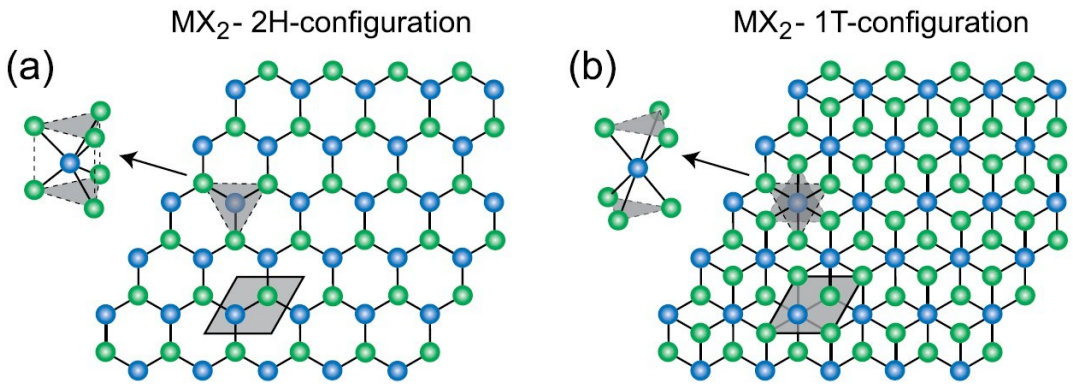


Figure 1.3: Atomic structure of single layers of TMDs in their (a) 2H and (b) 1T configurations. Reproduced with permission from De Gruyter.[43]

1.1.3.1 Molybdenum disulphide

Molybdenum disulphide (MoS_2) is the most extensively studied member of the TMD family, serving as a prototypical system for 2D semiconductor physics. In its bulk form, MoS_2 consists of vertically stacked layers held by weak vdW forces, with each monolayer comprising a plane of Mo atoms covalently coordinated in a trigonal prismatic geometry by two planes of S atoms. While MoS_2 can exist in metallic (1T) or rhombohedral (3R) phases, the 2H phase is the thermodynamically stable semiconducting configuration (Figure 1.4a). This hexagonal lattice is defined by in-plane lattice constants a = b = 3.15 Å and an interlayer spacing of c = 12.30 Å.

The electronic structure of MoS_2 is highly sensitive to quantum confinement. As the material is thinned from bulk to a monolayer, the indirect bandgap of approximately 1.2 eV (located between the Γ and K points) transitions into a direct bandgap of about 1.8 eV at the K-point of the Brillouin zone (Figure 1.4b-c).[44,45] This transition significantly enhances the photoluminescence quantum yield, making monolayer MoS_2 a key material for optoelectronic devices.

In typical field-effect transistor configurations, MoS_2 naturally exhibits n-type conduction, often attributed to sulphur vacancies or unintentional impurities that act as donors. Furthermore, unlike bP, MoS_2 possesses high environmental stability and a relatively inert surface, making it an excellent candidate for forming stable vdW heterostructures. When combined with p-type materials like bP, MoS_2 facilitates the formation of staggered (type-II) band alignments, which are essential for the photovoltaic explored in Chapter 3.

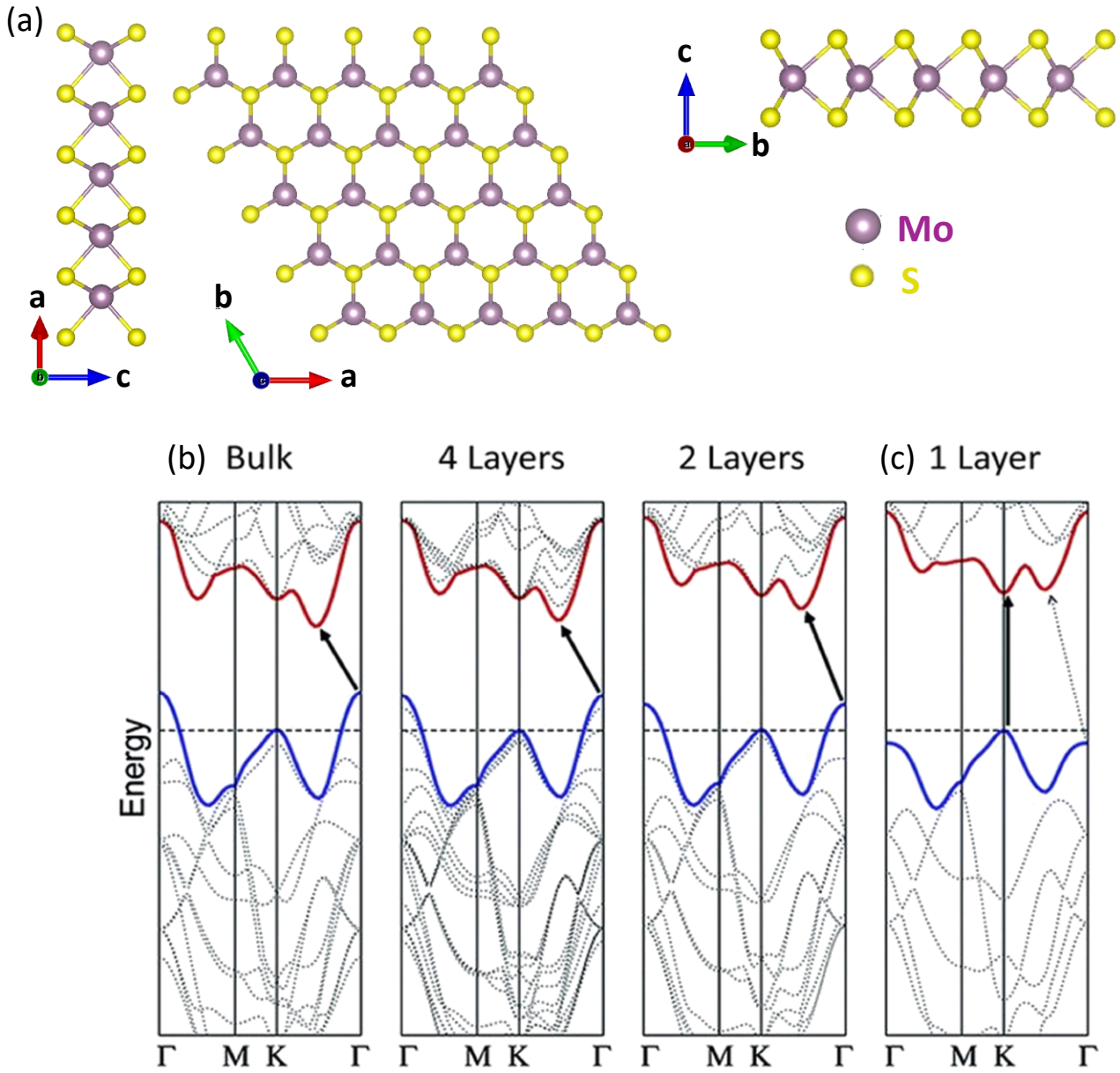


Figure 1.4: (a) Atomic structure of MoS_2. Band structure of MoS_2 from (b) bulk *to* (c) monolayer. Reproduced with permission from American Chemical Society.[46]

1.1.3.2 Tungsten disulphide

Tungsten disulphide (WS_2) is another prominent member of the group-VI TMD family, sharing structural similarities with MoS_2. It consists of S – W – S monolayers stacked via vdW interactions, with the 2H phase being the thermodynamically stable semiconducting configuration (Figure 1.5a). The hexagonal lattice is characterized by an in-plane lattice constant of a = b = 3.15 Å and an interlayer constant of c = 12.30 Å. It is characterized by a layer thickness of approximately 0.7 nm.

WS_2 is particularly noted for its exceptional optical properties. Like its molybdenum-based counterpart, WS_2 undergoes an indirect to direct bandgap transition when reduced to a monolayer. While bulk WS_2 has an indirect bandgap of around 1.3 eV, the monolayer exhibits a direct bandgap of approximately 2.1 eV at the K-point (Figure 1.5b-c).[47] Due to the higher atomic mass of tungsten compared to molybdenum, WS_2 exhibits a significantly stronger spin-orbit coupling, leading to a

large valence band splitting (up to 400 meV). This makes it an ideal platform for exploring valleytronic and spintronic phenomena.

In the context of this thesis, WS_2 is a key component in heterostructure-based sensors and artificial synapses (Chapter 4). Its high photo-responsivity and the presence of charge-trapping states at the interface, especially when combined with other TMDs like $PdSe_2$, enable the emulation of biological synaptic functions by exploiting the persistent photoconductivity. This property, characterized by a slow relaxation of the photocurrent after the light source is removed, allows the device to retain information, mimicking the synaptic weight modulation found in biological neural networks.

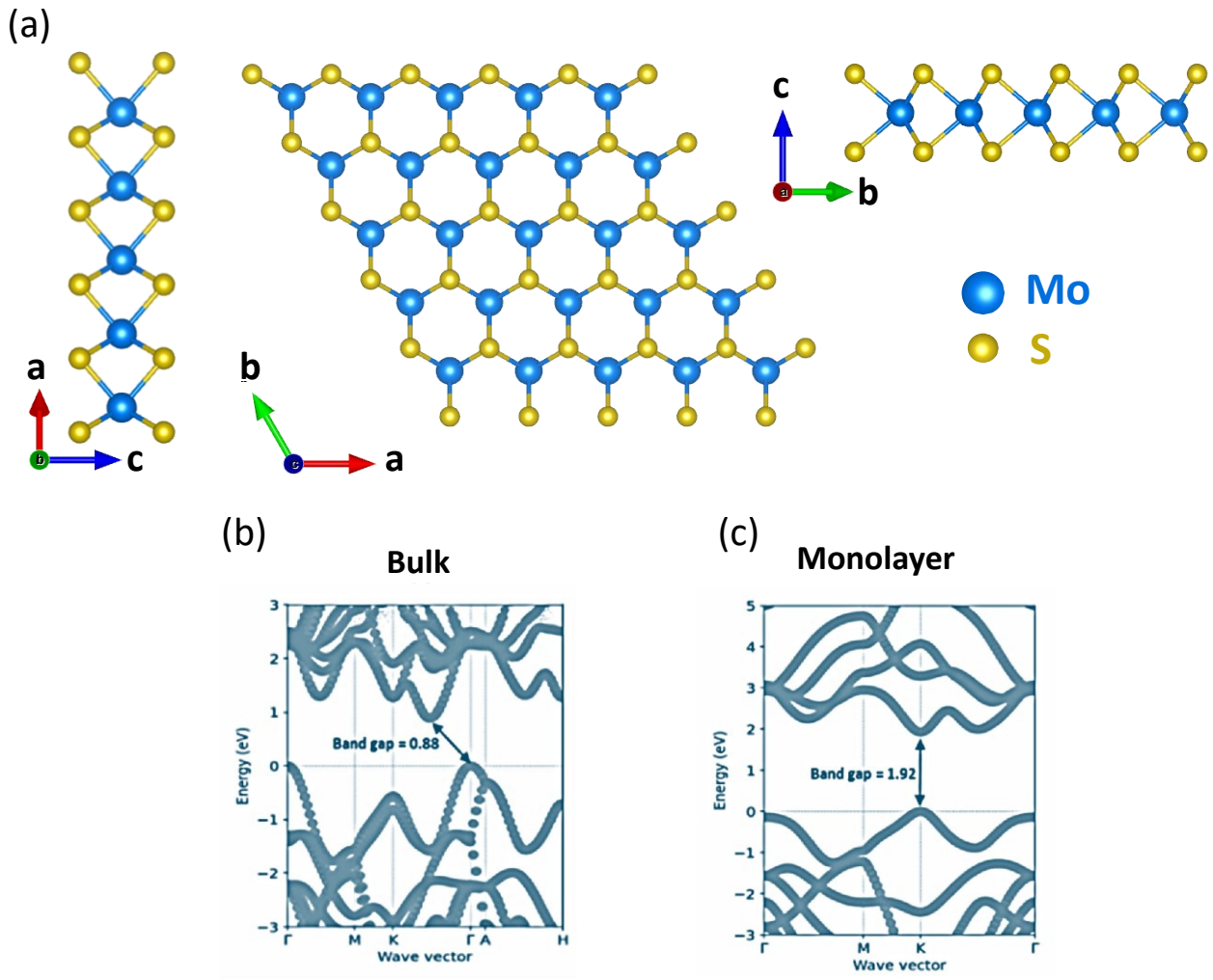


Figure 1.5: (a) Atomic structure of WS_2. Band structure of (b) bulk and (c) monolayer WS_2. Adapted from [48].

1.1.3.3 Palladium diselenide

Palladium diselenide ($PdSe_2$) belongs to the group-X noble transition metal dichalcogenides and is the first of its class discovered to exhibit a unique 2D pentagonal structure. Unlike the hexagonal coordination of MoS_2, each Pd atom in $PdSe_2$ is coordinated with four Se atoms in a planar tetra-coordination, while adjacent Se atoms form covalent Se-Se bonds. This arrangement results in a lattice of slightly distorted, asymmetric pentagonal rings (Figure 1.6a). The orthorhombic unit cell is defined by lattice parameters a = 5.75 Å, b = 5.87 Å, and an interlayer spacing of c = 7.69 Å.

A distinctive structural feature of $PdSe_2$ is its vertical puckering height of approximately 1.6 Å, which gives the layers a corrugated profile similar to that of bP. This puckered geometry is central to the material's high sensitivity to environmental stimuli, such as ambient pressure and strain. External pressure can easily modulate the interlayer coupling and the internal bond angles, leading to significant changes in the electronic transport properties, a phenomenon that underpins the pressure-sensing applications discussed in Chapter 4.

Electrically, $PdSe_2$ exhibits a thickness-dependent indirect bandgap that is highly tunable. It transitions from a nearly metallic (semimetallic) state in the bulk to a wide-bandgap semiconductor in the monolayer ($E_g \approx 1.3$ eV), as shown in Figure 1.6b-c.[49,50] Furthermore, $PdSe_2$ is characterized by high carrier mobility and remarkable ambient stability, which, combined with its unique symmetry, makes it an ideal candidate for high-performance, multi-functional vdW heterostructures.

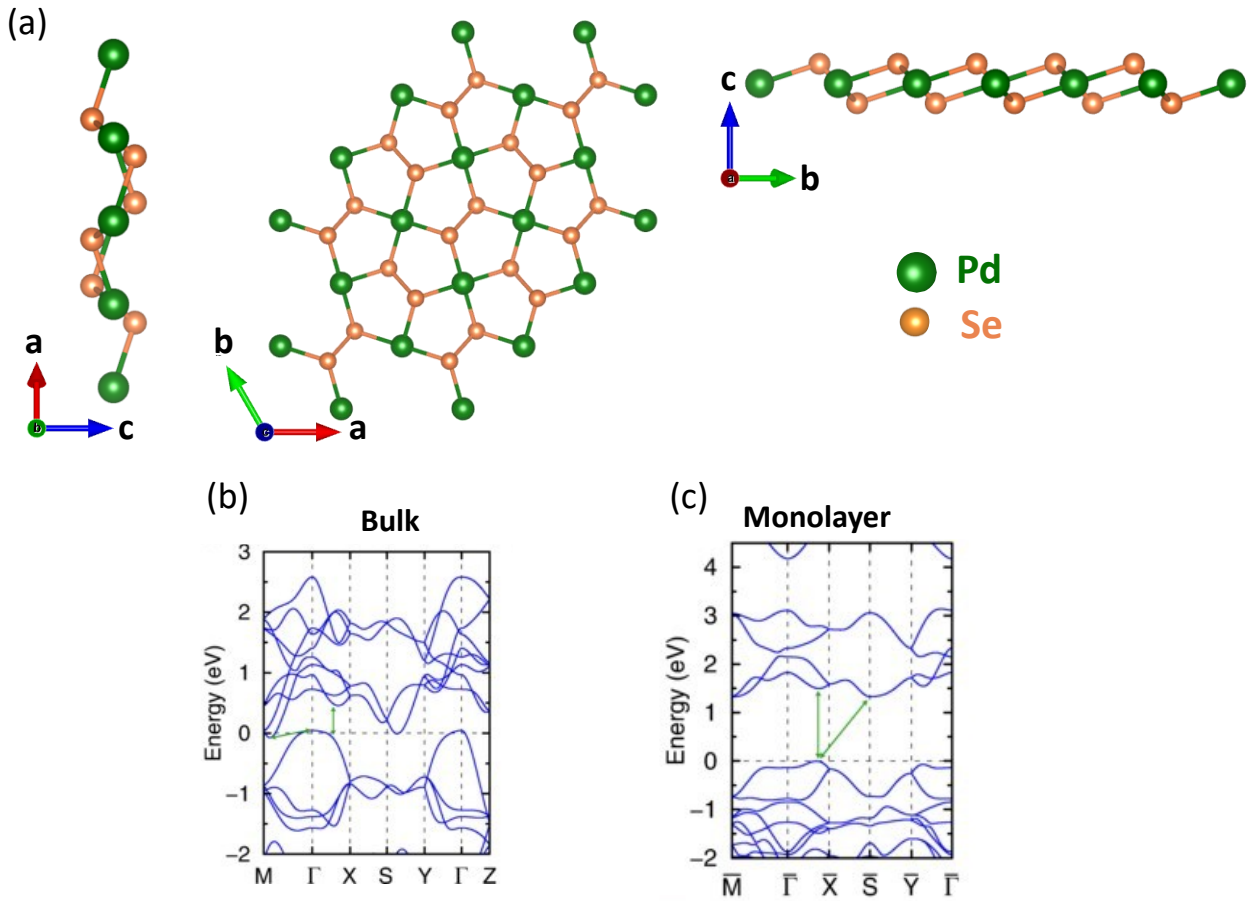


Figure 1.6: (a) Atomic structure of $PdSe_2$. Band structure of (b) bulk and (c) monolayer $PdSe_2$. Adapted from [51]

1.1.3.4 Molybdenum diselenide

Molybdenum diselenide ($MoSe_2$) is another representative member of the group VI-TMD that shares the hexagonal crystal symmetry of MoS_2 and WS_2. It consists of a plane of Mo atoms coordinated in trigonal prismatic geometry between two layers of Se atoms, with individual monolayers vertically stacked via weak vdW interactions (Figure 1.7a). The electronic band structure of $MoSe_2$ is characterized by an indirect to direct bandgap transition as the material thickness is reduced to a monolayer. While bulk $MoSe_2$ exhibits an indirect bandgap of approximately 1.1 eV, the monolayer

form presents a direct bandgap of 1.5 eV located at the K-point of the Brillouin zone (Figure 1.7b).[52] This slightly smaller bandgap compared to MoS_2 makes $MoSe_2$ particularly interesting for infrared-sensitive optoelectronics and logic applications. $MoSe_2$ is generally reported in the literature as an intrinsic n-type semiconductor, exhibiting transfer characteristics with on/off current ratios on the order of 10^6.[53–55] However, when contacted with Ti electrodes, $MoSe_2$ exhibits ambipolar behaviour, with the n-type branch strongly dominating over the p-type, and electron mobility exceeding hole mobility by about two orders of magnitude.[56,57]

In this thesis, $MoSe_2$ serves as the foundational material for Chapter 5, where its electronic landscape is precisely modulated through chemical p-type doping by using its interfacial coupling with CrOCl. This ability to switch the majority carrier type from electrons to holes allows for the fabrication of lateral p-n homojunctions, which are critical for developing 2D-based complementary logic circuits and CMOS-like inverters.

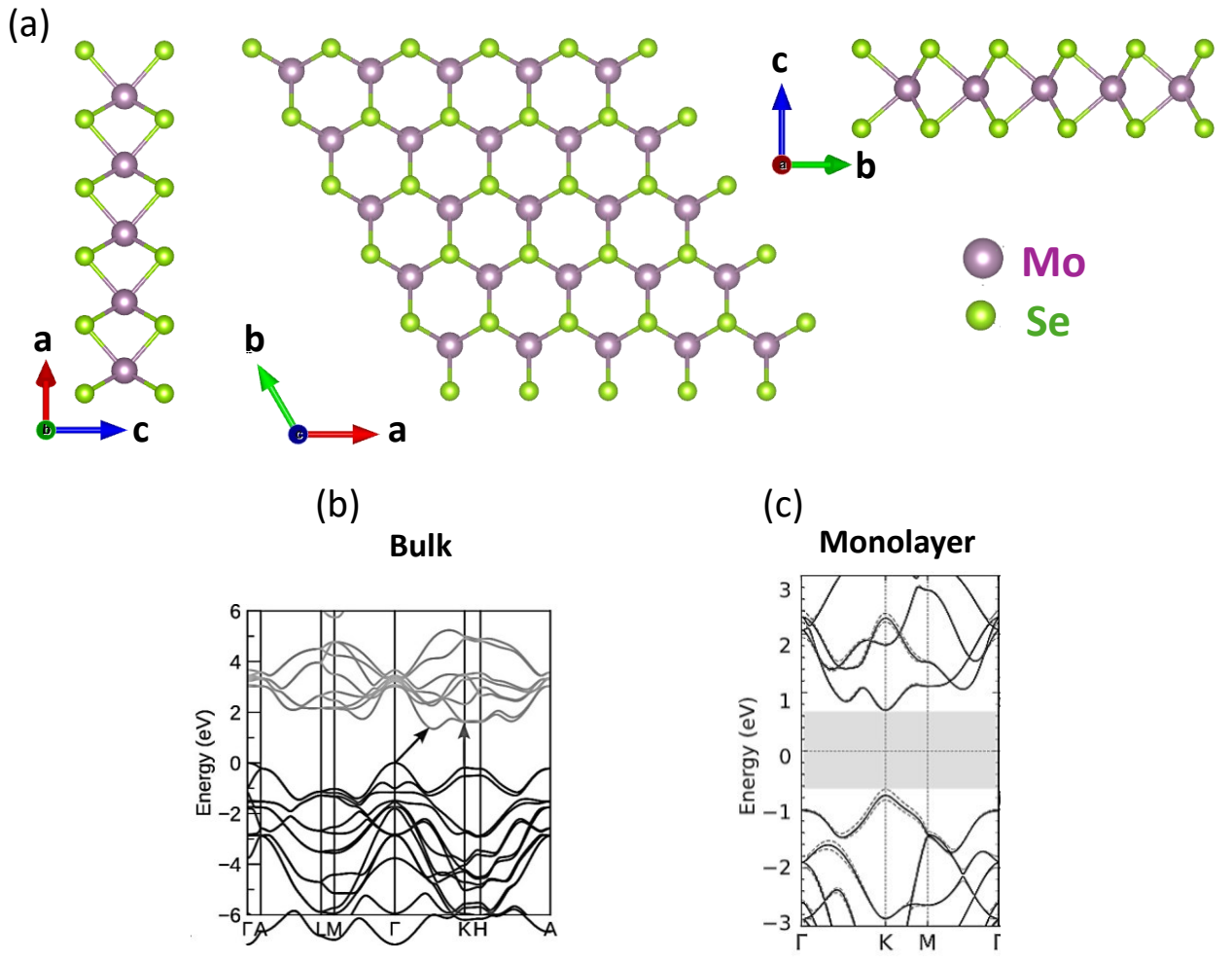


Figure 1.7: (a) Atomic structure of $MoSe_2$. Band structure of (b) bulk and (c) monolayer $MoSe_2$. Adapted from [58,59].

1.2 Field-effect transistors

The transistor is a semiconductive device that can be exploited to amplify, control, and generate electrical signals. First realized in 1925 and patented in 1934, FET is a three-terminal device that utilizes an electric field to modulate current flow within a semiconductor channel.[60] In the metal-

oxide-semiconductor (MOS) configuration, the 2D material acts as the conducting channel between two metallic electrodes: the source and the drain. The conductivity of this channel is modulated by a third electrode, the gate, which is separated from the channel by a thin insulating dielectric layer.

1.2.1 MOS electrostatics and channel formation

The fundamental principle of a FET is the modulation of the semiconductor's surface conductivity via an external electric field. This process is most clearly understood by examining the operation of a MOS capacitor, which serves as the core of the FET structure. Figure 1.8a shows a schematic of a conventional, planar, single-gate n-type MOSFET with the chosen coordinate system with the x-direction along the channel, the y-direction along the width and the z-direction oriented perpendicular into the substrate. Two highly n-doped source and drain regions are separated by a channel of length L within the p-doped silicon substrate. On top of the substrate, a gate electrode consisting of highly doped poly-silicon or a metal is placed and insulated from the substrate by a gate dielectric. The gate length and width W are considered to be equal to the channel length and width, respectively. Figure 1.8b-c show the band structure of a MOS structure at the thermal equilibrium, before (Figure 1.8b) and after (Figure 1.8c) the contact of the materials. By applying a gate voltage V_{gs}, the energy bands at the semiconductor-dielectric interface are bent, transitioning the device through different electrostatic regimes.

For a n-type MOSFET, the initial state depends on the relation between the gate voltage (V_{gs}) and the flat-band voltage (V_{fb}), which is the potential that takes account for the difference in the metal and semiconductor work functions, ϕ_m and ϕ_s, respectively. When $V_{gs} < V_{fb}$, there is the accumulation regime: majority carriers (holes) are attracted to the interface, increasing the local charge density but keeping the device in a non-conductive state for electrons (Figure 1.8d). As V_{gs} increases and exceeds V_{fb}, the positive gate potential repels holes from the interface. This creates a space charge region consisting of fixed, negatively charged ionized acceptors. This is the depletion regime, characterized by $V_{gs} > V_{fb}$ (Figure 1.8e). The thickness of this depletion layer grows with the gate voltage, but the channel remains non-conductive because there are no mobile electrons. When the surface potential (ψ_s) satisfies the condition $\psi_s = 2\phi_B$, where ϕ_B is the bulk potential, the MOSFET enters the inversion regime. The inversion point is defined as the moment when the concentration of minority carriers (electrons) at the semiconductor surface equals the concentration of majority carriers in the bulk. This condition marks the threshold voltage (V_{th}), which distinguishes the off-state of the transistor from its on-state. Beyond the inversion point, any further increase in gate voltage is primarily balanced by the increase in mobile electron density rather than an expansion of the depletion layer (Figure 1.8f). Specifically, the transition between the off-state and the on-state is related to the distinction between the weak and strong inversion. The weak inversion occurs when $\phi_B < \psi_s < 2\phi_B$. Although electrons are beginning to gather at the interface, their density is still relatively low. In this state, current transport is not dominated by drift but by diffusion over the potential barrier, leading to the exponential current-voltage characteristic of the subthreshold region, $I_d^{subth} \approx I_0 e^{\frac{q(V_{gs}-V_{th})}{\gamma K_B T}}$. Once $V_{gs} > V_{th}$, the MOSFET enters the strong inversion regime, which is characterized by $\psi_s > 2\phi_B$. Under this condition, at the semiconductor surface, the inversion charge dominates the space charge. The electron concentration at the interface becomes significantly higher than the bulk doping concentration. The drift of these mobile carriers becomes the dominant transport mechanism in this regime.

In the context of nanoelectronics and 2D materials, strong inversion results in an extreme vertical confinement of the carriers at the interface. The carriers are trapped in a triangular potential well formed between the gate insulator and the semiconductor substrate. As a result of this quantum confinement, the carriers occupy discrete 2D subbands. The 3D carrier density n(x,z) becomes a 2D sheet charge density $Q_{inv}(x)$, where motion is restricted to the x and y directions, i.e. along the channel and across the width, while being quantized in the z direction.

The fundamental operation of a FET relies on the electrostatic modulation of the charge carrier density within the semiconducting channel. The operation of a FET is generally categorized into three distinct regimes: cutoff (subthreshold), linear (ohmic), and saturation regimes. The physical modelling of these regimes depends on the dominant transport mechanism and the level of carrier inversion.

1.2.2 Gradual channel approximation: triode and saturation regimes

To describe the fundamental operation of a FET in the on-state analytically, the gradual channel approximation (GCA) serves as the standard physical framework. Considering the chosen coordinate system of Figure 1.8a, the GCA model is based on two main assumptions: uniformity across the channel width and field separation. The channel width is assumed to be sufficiently large such that the potential distribution is independent of the y-coordinate; the variation of the electric field along the channel (ε_x) is assumed to be much smaller than the variation of the field perpendicular to it (ε_z) induced by the gate.

Under this approximation, the drain current I_d at any x point along the channel can be calculated, as detailed in Appendix A. In the linear regime, i.e. in the limit of small drain bias, specifically when $V_{ds} << V_{gs} - V_{th}$, the transistor behaves as a voltage-controlled resistor, and the current-voltage characteristic simplifies to:

$$I_d = \mu \frac{W}{L} C_{ox}(V_{gs} - V_{th})V_{ds} \qquad (1.1)$$

As V_{ds} increases and reaches the gate overdrive, $V_{ds} \geq V_{gs} - V_{th}$, the carrier density at the drain end of the channel theoretically approaches zero, a condition known as pinch-off (Figure 1.9a). Beyond this point, the current remains constant (saturated) as the reduction in carrier density is compensated by an increase in carrier velocity. In the saturation regime, I_d depends quadratically on V_{gs}, equation 1.1 becomes:

$$I_d^{sat} = \frac{1}{2} \mu \frac{W}{L} C_{ox}(V_{gs} - V_{th})^2$$

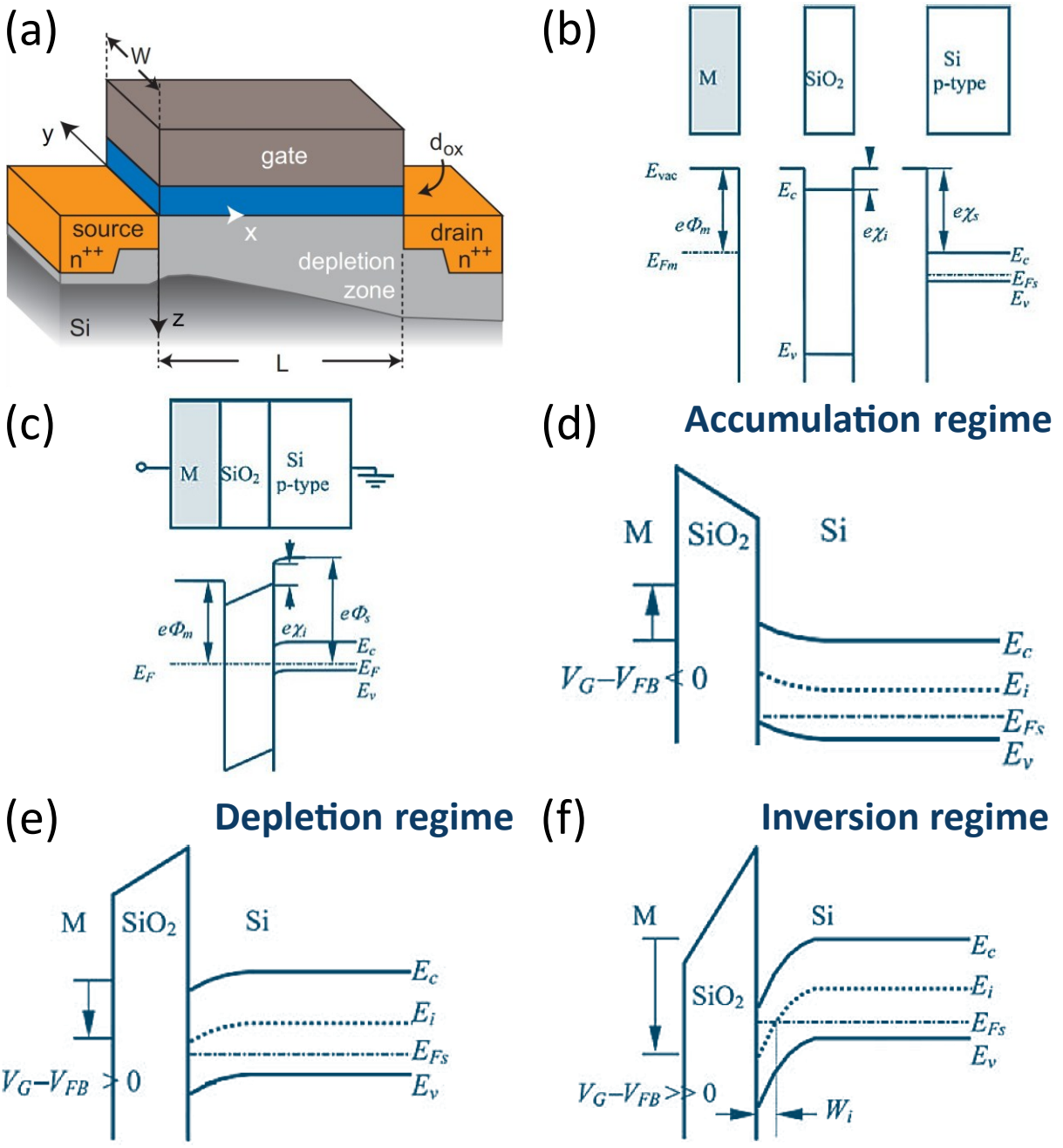


Figure 1.8: (a) Schematic of a conventional n-type, planar, single-gate MOSFET with channel length L and width W. The transistor channel is made of silicon, the oxide layer is depicted in blue, and the metallic gate is coloured of grey. Band diagram of a MOS structure (b) before and (c) after contacting the various materials. E_{vac} is the vacuum level, E_{Fm} and E_{Fs} are the Fermi energy of the metal and the semiconductor, respectively, ϕ_m is the metal work function, χ_i and χ_s are the insulator and semiconductor electron affinity, and E_c and E_v are the conduction band minimum and the valence band maximum energy MOS band diagrams in the (d) accumulation, (e) depletion and (f) inversion regimes. Adapted from [61].

While the GCA provides an accurate description of the strong inversion regimes (linear and saturation regimes), it inherently assumes that the inversion charge, and thus the current, vanishes once $V_{gs} \leq V_{th}$. However, in practical devices, the transition from the off-state to the on-state is not instantaneous. As illustrated in Figure 1.9b, the MOSFET operates across three primary regions:

cutoff (subthreshold), linear, and saturation regimes. When $V_{gs} > V_{th}$, the device is in its on-state, where the current is dominated by the drift of a high density of carriers, as modelled by the GCA. Conversely, when $V_{gs} < V_{th}$, the device enters the off-state or cutoff region. In this regime, the GCA's prediction of zero current fails, and a low-level subthreshold current persists between the source and drain.

The physics of the subthreshold regime is governed by the diffusion of carriers rather than drift. In this state, the gate voltage modulates the height of the energy barrier at the source end of the channel. As V_{gs} increases, this barrier is lowered, allowing a small number of carriers to be thermally injected from the source into the channel following a Boltzmann distribution. Consequently, the subthreshold current increases exponentially with the gate voltage according to the relation:

$$I_d = I_0 e^{\frac{q(V_{gs}-V_{th})}{\eta k_B T}} \qquad (1.2)$$

where I_0 is a technology constant, q is the elementary charge, k_B is the Boltzmann constant, and T is the absolute temperature. The parameter η is the ideality factor, which reflects the efficiency of the electrostatic coupling between the gate and the channel. This coefficient accounts for the capacitive voltage divider between the gate oxide and the depletion layer/interface traps, determining how effectively the gate can pull the surface potential and thus modulate the subthreshold current.

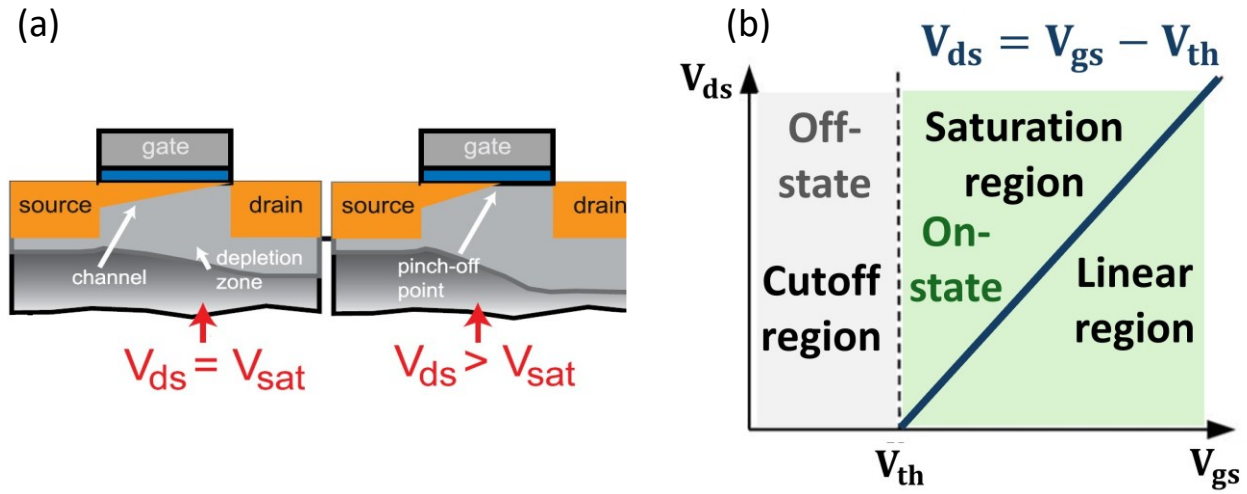


Figure 1.9: (a) Schematic of the MOSFET with the pinch-off condition. (b) Operating regions of a MOSFET.

1.2.3 Current-voltage characterization

The electrical performance and transport properties of 2D material-based FETs are typically quantified through two primary measurement configurations: output and transfer characteristics. These measurements allow for the extraction of fundamental parameters such as field-effect mobility, threshold voltage, and contact resistance, which are essential for determining material quality and device suitability for logic applications. The equation (1) is the fundamental equation for the electrical characterization of 2D materials in this thesis.

OUTPUT CHARACTERISTICS To measure the output characteristics (I-V characteristics) of a FET, I_d is measured as a function of V_{ds} at fixed V_{gs} (see Figure 1.10a). However, in the presence of contact resistance, only a portion of V_{ds} drops across the channel; thus, equation (1) must be further modified to address this issue, leading to

$$I_d = \frac{\mu_{eff} W}{L} C_{ox}\left[\left(V_{gs} - V_{th}\right)\left(V_d - I_d \cdot 2R_c\right)\right]$$

where $2R_c$ represents the total contact resistance at the source and drain junctions. It is important to note that when using a global back-gate, which will be detailed in section 1.2.5, the gate electric field simultaneously modulates the carrier density in both the channel and the contacts regions. Consequently, R_c becomes a function of V_{gs} and V_{ds}. The linearity of the output characteristics at low V_{ds} serves as a critical diagnostic tool to determine whether the device performance is limited by the intrinsic channel properties or by metal-semiconductor interfaces.

TRANSFER CHARACTERISTICS The transfer characteristics are obtained by measuring I_d as a function of V_{gs} while maintaining a constant V_{ds}. For n-type semiconductors, I_d increases as V_{gs} becomes more positive, whereas for p-type semiconductors, the current increase as V_{gs} becomes more negative (see Figure 1.10b). This measurement is fundamental for extracting the threshold voltage V_{th}, the on/off current ratio, the field-effect mobility (μ_{FE}) and the subthreshold swing (SS).

The threshold voltage is typically extracted by extrapolating the linear portion of the transfer curve to the x-axis (Figure 1.10c). This value separates the off-state from the on-state of the transistor. The ratio between the maximum current in the on-state and the minimum current in the off-state is a key metric for the switching efficiency of logic transistors. The on/off current ratio is generally indicated as a magnitude order, i.e. as a power of 10.

The transconductance, $g_m = \frac{\partial I_d}{\partial V_{gs}}$, quantifies the sensitivity of the drain current to gate voltage variations. According to equation 1.1, the field-effect mobility is derived from the transconductance of a MOSFET biased in the linear regime (Figure 1.10c), which is given by:

$$\mu_{FE} = \frac{g_m}{C_{ox} V_{ds}} \frac{L}{W} \tag{1.3}$$

The subthreshold swing, which is a key parameter indicating the sharpness of the switching behaviour of a 2D FET, is defined as the change in gate voltage required to change the drain current by one order of magnitude. It is calculated as the inverse of the slope of the transfer characteristic on a semi-logarithmic scale:

$$SS = \left(\frac{\partial \log_{10} I_d}{\partial V_{gs}}\right)^{-1} \tag{1.4}$$

Taking the logarithm of equation 1.2:

$$\log_{10} I_d = \log_{10} I_0 + \frac{q\left(V_{gs} - V_{th}\right)}{\eta k_B T \ln 10} \tag{1.5}$$

Differentiating equation 1.5 with respect to V_{gs} and taking the inverse yields:

$$SS = \frac{k_B T}{q} \eta \ln 10 \approx 60\eta \text{ mV/decade}$$

The ideality factor η accounts for the capacitive voltage divider between the gate and the channel, $\eta = 1 + \frac{C_{dm} + C_{it}}{C_{ox}}$, where C_{dm} is the depletion capacitance, and C_{it} represents the capacitance due to interface traps.

For an ideal 2D FET, the depletion capacitance C_{dm} is negligible due to the atomistic thickness of the channel ($C_{dm} << C_{ox}$). In the limit of a perfect dielectric interface ($C_{it} \approx 0$), η approaches unity. This results in the thermionic limit of $SS_{ideal} \approx 60$ mV/decade at room temperature (300 K). This value represents the physical lower bound for any classical FET at room temperature. Experimental values significantly higher than 60 mV/decade indicate a high density of interface traps (D_{it}) or poor electrostatic control. Since SS is directly proportional to temperature and $C_{it} = q^2 D_{it}$, it is possible to estimate the trap density D_{it} by performing a linear fit of the SS measured as a function of temperature: $SS = \frac{k_B T}{q}\left(1 + \frac{q^2 D_{it}}{C_{ox}}\right) \ln 10$.

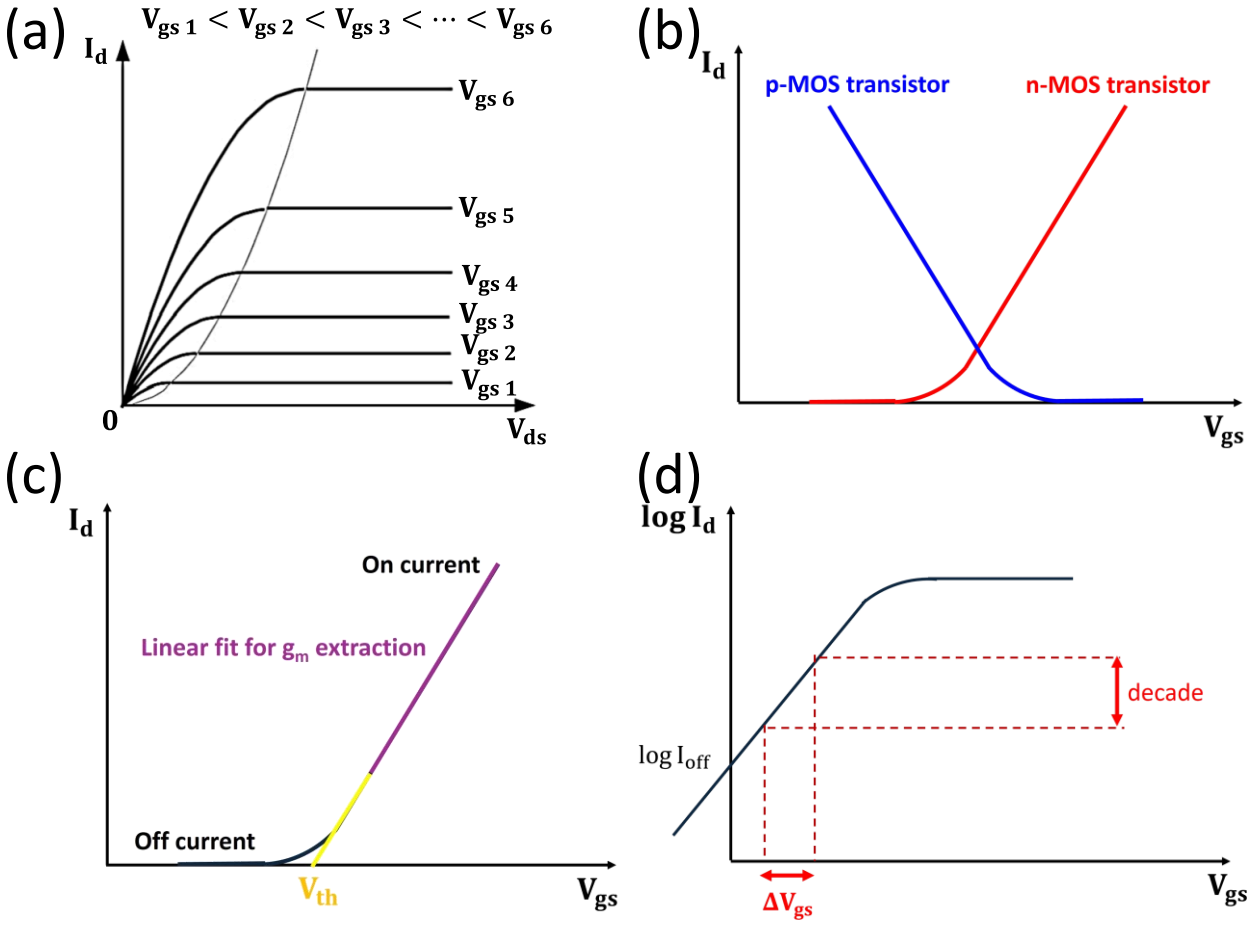


Figure 1.10: (a) Output characteristics of a MOSFET at different gate voltages. The grey line serves as the boundary between the linear region and the saturation region. (b) Transfer characteristic of a p-MOS (blue line) and a n-MOS (red line) transistor. (c) Transfer characteristic of a n-MOS transistor with the linear fit (purple line) for the extraction of the transconductance for the calculation of the charge carrier mobility and the estimation of the threshold voltage (yellow). The on and off current levels are indicated. (d) Log I_d vs V_{gs} for the extraction of the subthreshold swing.

1.2.4 Contact resistance

In the development of 2D materials-based FETs, contact resistance represents one of the most significant challenges for both device performance and accurate material characterization. Unlike traditional silicon technology, where heavy ion implantation ensures ohmic contacts, 2D materials lack a straightforward doping strategy. This often results in the formation of Schottky barriers at the

metal-semiconductor-interface due to Fermi level pinning or a large work-function mismatch. When R_c is high, i.e. on the order of 100 kΩ µm, it dominates the total device resistance, $R_{tot} = R_{ch} + 2R_c$, where R_{ch} is the channel resistance and R_c is the contact resistance, leading to a underestimation of the material's intrinsic mobility and a reduction in the on/off current ratio. Furthermore, in back-gated structures, R_c is not a constant because the gate field modulates the carrier density under the contacts, making the contact resistance a function of V_{gs}.

To isolate the intrinsic properties of the 2D channel, several experimental and analytical methods are employed, such as four-probe measurements, the transfer length method (TLM), and the Y-function method.

2PP AND 4PP MEASUREMENTS

In a standard two-probe (2PP) setup, the current and the voltage are assessed and applied by the same terminals; in this configuration, the measured resistance includes both the channel and the contacts. Assuming $R_{ch} > R_c$ along with the linear I_d vs V_{ds} characteristics, R_{ch}, R_{sh}, which is the sheet resistance, and σ, which is the electrical conductivity, can be determined by using the following relationship:

$$R_{ch} = R_{sh}\frac{L}{W} = \frac{1}{\sigma t_{ch}}\frac{L}{W}$$

where t_{ch} refers to the thickness of the 2D semiconducting channel. However, the contact resistance in back-gated 2D FETs is either comparable or higher than the channel resistance, resulting in significant errors in the R_{ch} value extracted using 2PP measurements. This issue can be resolved by using the four-probe (4PP) configuration, which can deconvolute the effect of R_c on the extracted R_{ch} and R_{sh} values.

In the Hall bar geometry, which is the configuration used in Chapter 3 (Section 3.2.4), the 2D material flake is patterned into a specific bridge-type structure where the source and drain electrodes are separated by a long channel with several arms serving as voltage probes. This configuration is specifically designed to facilitate accurate 4PP measurements by ensuring that the voltage probes are positioned away from the primary current path. A constant drain current is sourced through the two outer electrodes. Two intermediate voltage probes, V_1 and V_2, along the channel are used to sense the potential difference: $V_{12} = |V_2 - V_1|$. Because these inner probes are connected to high-impedance measurement terminals, they draw negligible current. Consequently, there is no voltage drop across the contact resistance of these sensing probes, allowing them to act as perfect voltmeters that measure the potential drop of the intrinsic channel only. The intrinsic R_{ch} is then extracted from the 4PP I-V characteristics using the following geometric relation:

$$R_{ch} = \frac{V_{12}}{I_d}\frac{L}{L_{12}}$$

Where L is the total channel length and L_{12} is the specific distance between the two inner voltage probes. This calculation effectively deconvolutes the effects of the source and drain contact resistance from the material's transport properties. Once R_{ch} is determined, the total contact resistance can be precisely isolated by subtracting this intrinsic value from the total resistance measured in a 2PP configuration, $2R_c = R_{tot} - R_{ch}$.[62]

TRANSFER LENGTH METHOD (TLM)

The transfer length method (TLM) is a widely utilized experimental technique for isolating the contact resistance from the intrinsic properties of a 2D semiconductor. This method requires the fabrication of a series of FETs on the same 2D flake with varying channel lengths while keeping the channel width constant. The fundamental principle of TLM is that the total measured resistance is a linear combination of the length-dependent channel resistance and the parasitic resistance from the two contacts:

$$R_{tot} = R_{ch}(L) + 2R_c = \left(\frac{R_{sh}}{W}\right)L + 2R_c$$

By plotting R_{tot} as a function of the channel length and applying a linear fit, several critical parameters can be extracted. The y-intercept of the linear fit at L = 0 corresponds to $2R_c$, the slope of the line multiplied by the channel width provides the R_{sh} of the 2D channel. The x-intercept where $R_{tot} = 0$ provides the value of $-2L_t$ with L_t the transfer length, which represents the effective distance over which the majority of the current is injected from the metal into the semiconductor. In back-gated 2D FETs, R_c and L_t are typically not constant but are functions of V_{gs}. This occurs because the gate electric field simultaneously modulates the carrier density in the channel and the region directly under the metal contacts, a phenomenon known as contact gating.

While TLM is material-agnostic and straightforward, it faces specific challenges in 2D research. Indeed, reliable extraction requires both R_c and R_{sh} remain consistent across all devices in the series. Irregular flake geometries or non-uniform polymer residues from lithography can lead to significant errors. To avoid Joule heating and impact ionization, TLM measurements should ideally be performed at low V_{ds}. If $R_c >> R_{ch}$, even minor inter-device variations can cause large errors in the linear fit.[62]

Y-FUNCTION METHOD

For the analysis of bP FETs, where flake sizes and device architectures limit the feasibility of TLM, the Y-function methos (or Ghibaudo method) serves as a powerful analytical alternative.[63] This method allows for the extraction of the low-field mobility (μ_0) and V_{th} while mathematically attenuating the effects of the contact resistance and mobility degradation. This analytical method also allows for the estimation of R_c from 2PP measurements. The Y-function is defined as:

$$Y = \frac{I_d}{\sqrt{g_m}} = \sqrt{\frac{W}{L}C_{ox}\mu_0 V_{ds}}\left(V_{gs} - V_{th}\right) \qquad (1.6)$$

In the strong inversion regime, a plot of Y vs V_{gs} yields a straight line. The slope of this line is directly proportional to the square root of the low-field mobility μ_0, and its intercept on the V_{gs} axis provides a highly accurate determination of V_{th}.

The primary advantage of this method is that the denominator $\sqrt{g_m}$ cancels out the first-order mobility degradation factor θ, which is heavily influenced by R_c in 2D FETs. Consequently, the Y-function provides a contact-independent view of the carrier transport, which is essential for evaluating the high-performance of 2D materials-based devices.

Since:

$$I_d = \frac{W}{L} C_{ox} \frac{\mu_0}{1 + \theta(V_{gs} - V_{th})} (V_{gs} - V_{th}) V_{ds}$$

And

$$g_m = \frac{W}{L} C_{ox} \frac{\mu_0}{\left[1 + \theta(V_{gs} - V_{th})\right]^2} V_{ds}$$

the mobility degradation factor is given by

$$\theta = \frac{\left(\frac{I_d}{g_m(V_{gs} - V_{th})} - 1\right)}{V_{gs} - V_{th}}$$

A plot of $1/\sqrt{g_m}$ versus V_{gs} yields a straight line whose slope is directly proportional to θ, because:

$$\frac{1}{\sqrt{g_m}} = \sqrt{\frac{1}{G_m V_{ds}}} \left[\theta(V_{gs} - V_{th}) + 1\right]$$

where $G_m = \frac{W}{L} C_{ox} \mu_0$. Once μ_0 and θ are known, R_c can be calculated considering that

$$\theta = \frac{W}{L} C_{ox} \mu_0 R_c$$

Once μ_0 and V_{th} are known, the gate dependent contact resistance can be also calculated using the relationship:

$$R_c(V_{gs}) = \frac{V_{ds}}{I_d} - \frac{L}{W C_{ox} \mu_0 (V_{gs} - V_{th})}$$

In practice, implementing the Y-function method requires a continuous transfer characteristic sweep at a fixed V_{ds} over different V_{gs} ranges. Alternatively, it can be performed using a series of I_d data points extracted from multiple output curves at varying V_{gs} for a constant V_{ds}. This high-density data set is necessary to accurately the transconductance across the entire gate voltage range.[64,65]

1.2.5 Back-gate and floating-gate device architectures

The device structure of 2D material-based FETs is not universal; rather, it is strategically chosen based on the intended application, whether it be fundamental material characterization, demonstration of specific functions or marketing applications. In the field of 2D electronics, the most common configurations are top-gate, back-gate, and floating-gate structures.

The implementation of a top-gate architecture is often viewed as the transition from experimental material study to circuit-level integration. In this configuration, a dielectric and a metal electrode are deposited on top of the 2D channel, allowing for the independent control of individual transistors, a fundamental prerequisite for logic gates and complex integrated systems. While top-gating provides superior electrostatic coupling and allows for the use of high-k dielectrics like HfO_2 to lower operating voltages, it presents significant fabrication challenges. Depositing conventional oxides directly onto the pristine, dangling-bond-free surface of 2D materials often results in interface traps or doping inhomogeneities. To mitigate this, high-performance top-gates frequently utilize hexagonal boron nitride (hBN) as a buffer layer or encapsulate the channel entirely to preserve its intrinsic mobility.

In this thesis, however, the primary focus is directed toward the back-gate (BG) and floating-gate (FG) architectures, as they provide the most robust platform for the characterization and functionalization of 2D flakes. The global back-gate configuration, utilizing a heavily doped silicon substrate separated by a thermal SiO_2 layer, serves as the fundamental characterization testbed. This structure is particularly advantageous for experimental flakes because it requires no precise alignment, allowing for the immediate evaluation of exfoliated samples. However, the BG structure introduces the phenomenon of contact gating, which is a central theme in the electrical analysis of this work. Because the gate electric field is applied globally, it does not only modulate the carrier density within the channel but also penetrates the region beneath the metal contacts. This causes the contact resistance to be highly dependent on the gate voltage, as the field thins the Schottky barrier at the source and drain interfaces. Consequently, the back-gate architecture necessitates the advanced extraction techniques discussed previously, such as the Y-function method, to deconvolute the gate-dependent contact effects from the intrinsic material properties of the 2D flake.

Moving beyond simple switching, the FG architecture is employed to transform the 2D FET into a data storage device. This structure builds upon the back-gate foundation by inserting an electrically isolated floating gate layer, typically graphene or a thin metal, between the channel and a control gate. The operation relies on the controlled injection of charge from the 2D channel into this floating gate through a thin tunnelling barrier often composed of a few layers of hBN. Once charge is trapped on the floating gate, it creates a persistent internal electric field that shifts V_{th} of the underlying FET. This shift allows the device to retain information even after the external power is removed. Furthermore, by modulating the amount of trapped charge in a quasi-non-volatile manner, these floating-gate devices can emulate synaptic plasticity, where the conductance of the channel represents a programmable weight in a neuromorphic computing circuit. This architectural choice thus bridges the gap between traditional semiconductor logic gates and the emerging field of brain-inspired hardware.[66]

1.3 Van der Waals heterostructures

Beyond the study of individual atomic layers, the ability to combine disparate 2D materials into complex vertical stacks has opened a new frontier in condensed matter physics and device engineering. These assemblies, known as vdW heterostructures, are formed by the precise stacking of different 2D crystals, effectively acting as artificial solids with tailored properties. As famously conceptualized by Geim and Grigoreiva[67], this process can be compared to building with Lego blocks, where individual 2D crystals serve as bricks that can be reassembled in any chosen sequence with one atomic plane precision (Figure 1.11).

The defining feature of these heterostructures lies in the nature of their interlayer bonding. Unlike traditional 3D semiconductors, 2D layers are held together by weak, out-of-plane vdW forces. This fundamental characteristic allows for the integration of materials with vastly different electronic, optical, and structural properties without the constraint of lattice matching. The absence of dangling bonds on the surfaces of these layers ensures atomically sharp and chemically pristine interfaces. The implementation of vdW heterostructures is central to the research presented in this thesis, as they offer the unique capability to engineer functional interfaces tailored for probing fundamental physical phenomena. Furthermore, these structures provide a versatile framework for developing

multifunctional platforms that seamlessly integrate disparate electronic applications into a single device architecture.

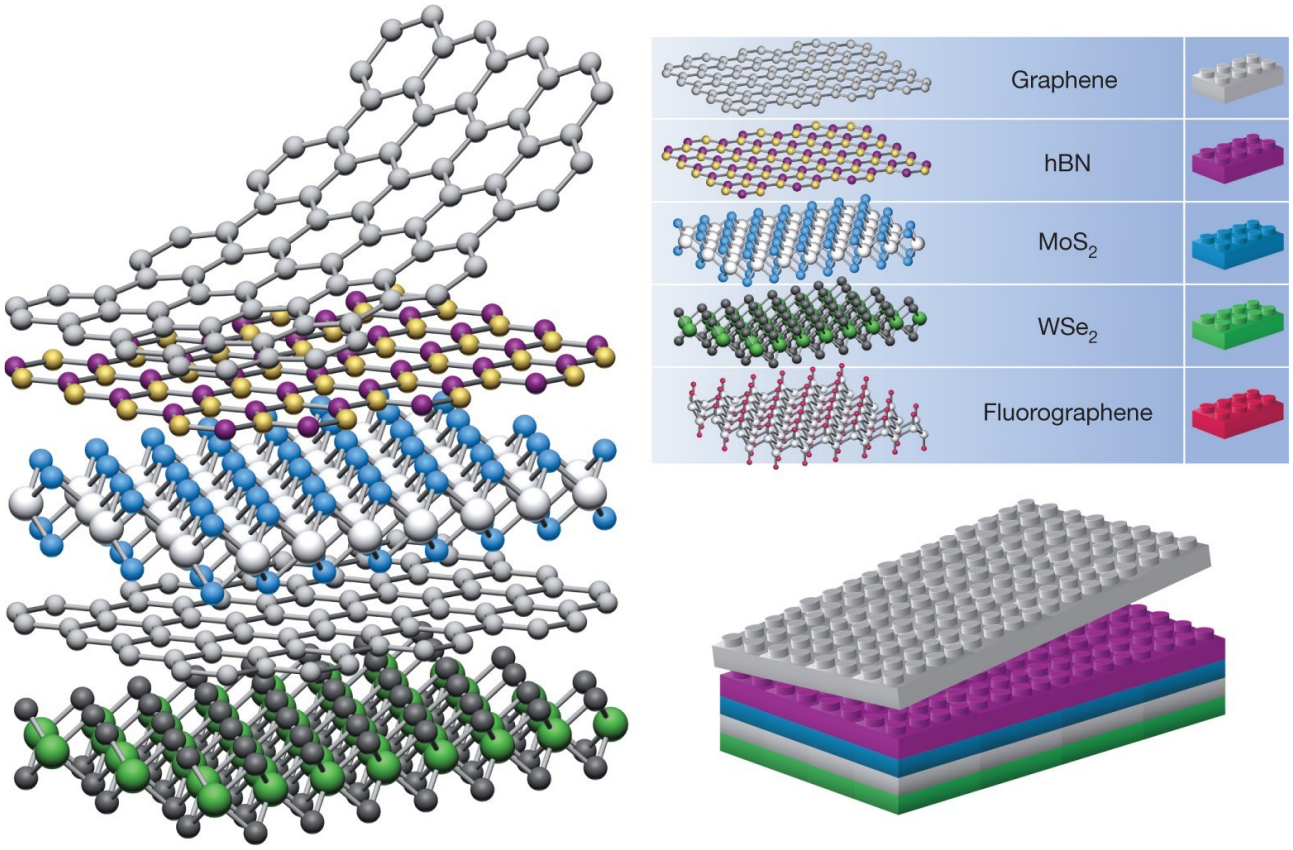


Figure 1.11: Building vdW heterostructures: 2D crystals serve as bricks to be reassembles in different ways. Reproduced with permission from Springer Nature.[67]

1.3.1 Band alignment theory: Anderson's rule

The electronic and optoelectronic functionality of a vdW heterostructure is fundamentally governed by the energy alignment of the band edges at the interface between the constituent layers. In the most basic model, this alignment is predicted using the Anderson's rule, also known as the electron affinity rule, which posits that the vacuum levels of two isolated semiconductors will align when they are brought into contact. Under this framework, the conduction band offset (ΔE_c) and valence band offset (ΔE_v) are determined solely by the intrinsic properties of the individual materials, namely their electron affinities (χ) and bandgaps (E_g), relative to a common vacuum reference (Figure 1.12a). Anderson's rule states that ΔE_c is given by the difference between the electron affinity of the two materials. In the case of Figure 1.12a, the band offset is given as:

$$\Delta E_c = e(\chi_n - \chi_p)$$

Once the conduction band offset is given, the valence band offset can be easily determined, since the bandgaps off the two materials are fixed. The sum of the band offsets is the difference of the bandgap of the two materials, $\Delta E_c + \Delta E_v = E_{g,p} - E_{g,n} = \Delta E_g$.[61]

The clarity of Anderson's rule is particularly appealing for 2D materials because the weak out-of-plane vdW forces typically preserve the electronic integrity of the individual layers. As a result, the energy bands of each layer can often be treated as rigid blocks that simply translate in energy when stacked. Based on the relative positions of these bands, vdW heterojunctions are traditionally

classified into three distinct categories: type-I (straddling gap), type-II (staggered gap), and type-III (broken gap) heterojunctions. In type-I heterojunctions (Figure 1.12b), the conduction and valence band edges of one material reside entirely within the bandgap of the other material. This configuration facilitates the spatial confinement of both electrons and holes within a single layer, making it the ideal architecture for high-efficiency light-emitting diodes and lasers. In type-II heterojunctions (Figure 1.12c), the band edges are staggered such that the lowest energy state for electrons is in one layer, while the lowest energy state for holes is in the adjacent layer. This separation of charge carriers is crucial for photovoltaic applications and photodetectors, as it inhibits recombination and promotes the formation of spatially indirect interlayer excitons. In type-III heterojunctions (Figure 1.12d), the conduction band minimum of one semiconductor lies below the valence band minimum of the other one. This extreme alignment allows for broken-gap tunnelling, serving as a platform for the development of tunnel FETs and Esaki diodes. The equilibration of the Fermi levels across a heterojunction results in band bending, as shown in Figure 1.12e.

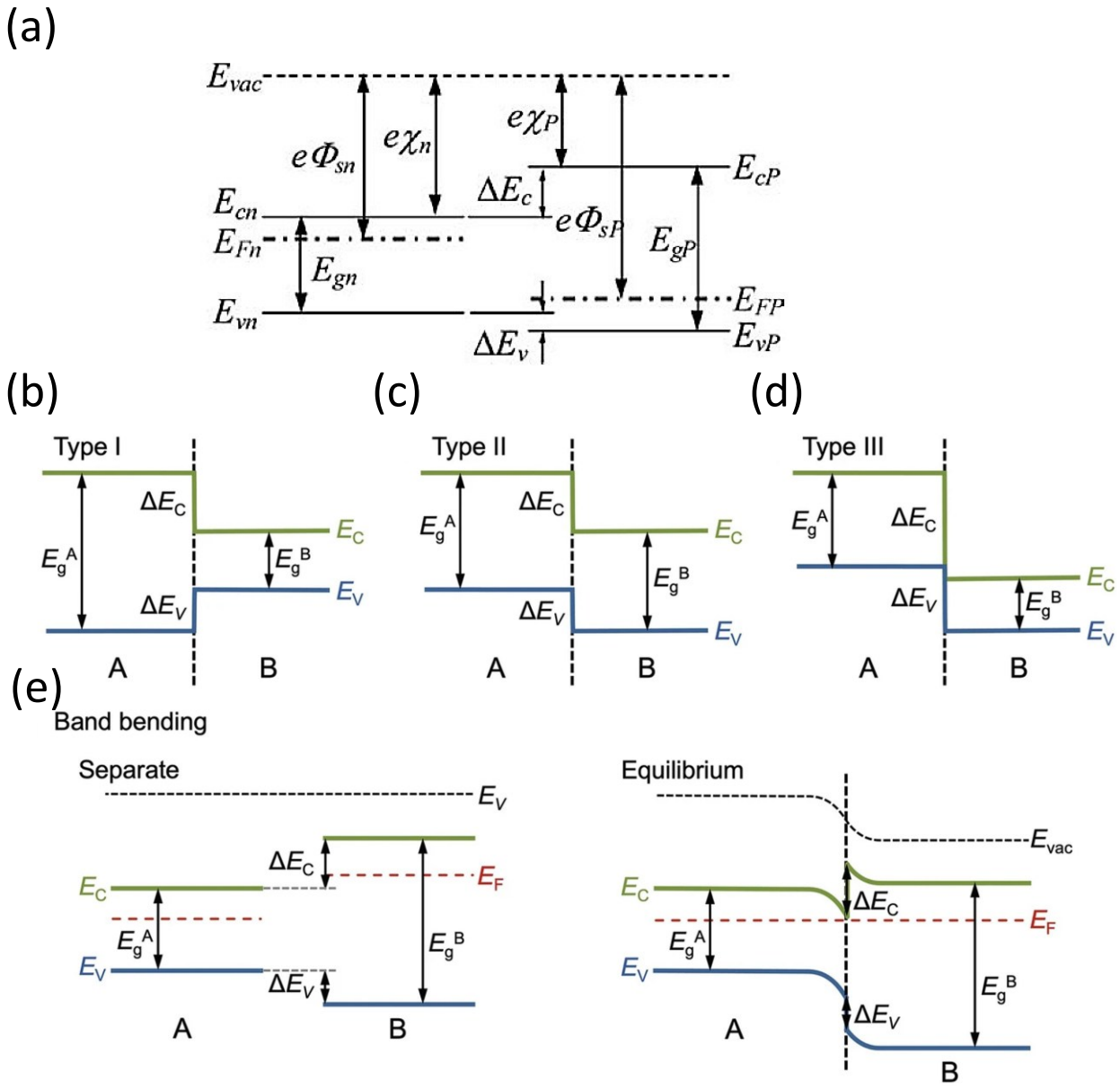


Figure 1.12: (a) Band alignment in a heterojunction system before the contact of materials. Conduction and valence bands of two semiconductors (A and B) and their band alignments for (b) type-I, (c) type-II, and (d) type-III heterojunctions. (e) Band bending as a result of the equilibration of the Fermi levels across a heterojunction. Adapted from [68].

1.3.2 p-n and n-n heterojunctions

Beyond the general classification of band offsets, the electronic behaviour of a heterostructure is fundamentally defined by the doping polarity of its constituent layers, leading to the distinction between anisotype (p-n) and isotype (n-n or p-p) junctions. The p-n heterojunction represents the most traditional configuration for electronic applications, where the integration of two semiconductors with opposite doping types creates a junction characterized by both a built-in potential and discrete band discontinuities. Unlike a standard homojunction, where the bandgap is continuous across the interface, the p-n heterojunction utilizes conduction and valence band offsets to provide an additional layer of control over carrier transport. This is notably exploited in the wide-gap emitter effect, where a large band offset on one side of the junction can be engineered to favor

the injection of one carrier type, such as electrons in the p-region, while simultaneously suppressing the back-injection of holes. This asymmetric injection is a cornerstone of high-performance heterojunction bipolar transistors and allows for significantly higher injection efficiencies than those achievable in silicon-based homojunctions.

In contrast, isotype heterojunctions, specifically the n-n configuration, involve materials of the same doping type but with different bandgaps and electron affinities. The physics of these junctions is governed by the redistribution of charge required to align the Fermi levels at equilibrium. Typically, electrons will migrate from the material with the higher Fermi level to the one with the lower level, resulting in the formation of an accumulation layer on one side of the interface and a depletion region on the other side.

While Figure 1.12a shows the band alignment of a n-p heterojunction system before the contact of materials, Figure 1.13a-b shows the band diagram of n-p and n-n heterojunctions after the contact is made. Due to the charge transfer and formation of depletion, or accumulation, regions, the bands start to bend, while maintaining the band offset at the interface. The charge transfer will stop when an equilibrium is reached. The built-in potential is the same as the difference in the Fermi levels of isolated materials.

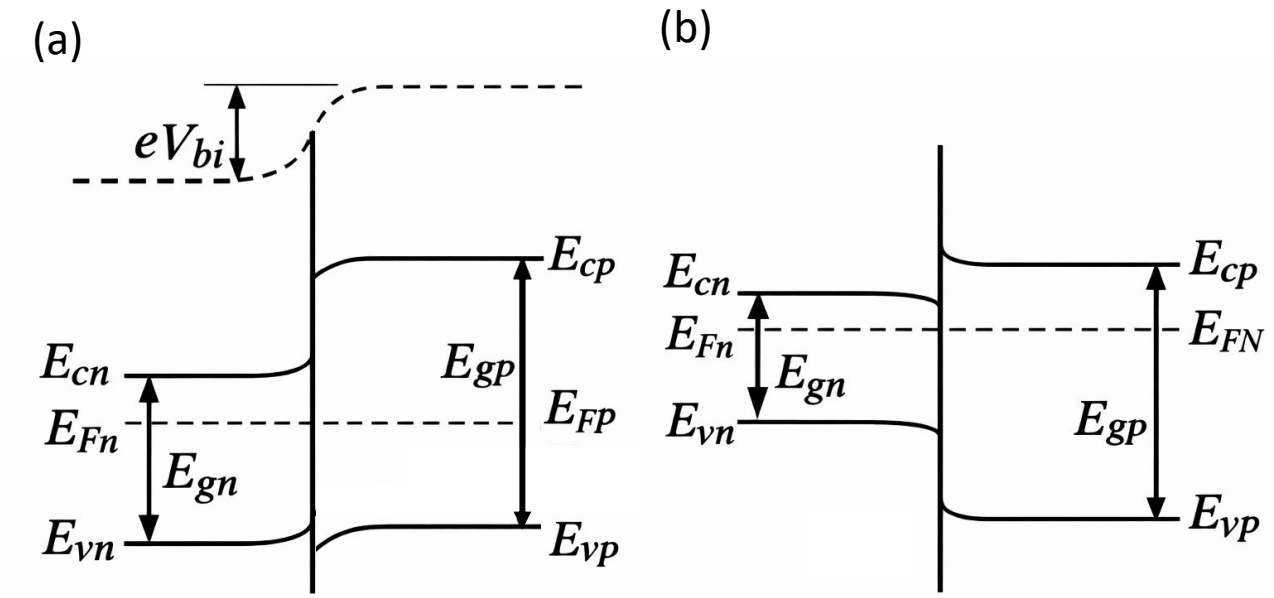


Figure 1.13: Band diagram of heterojunction systems after the contact of materials: (a) n-p heterojunction and (b) n-n heterojunction.

1.4 Emerging applications in 2D electronics

The exceptional electronic and optoelectronic properties of 2D materials, particularly when integrated into vdW heterostructures, have paved the way for a new generation of nanoelectronic devices that transcend the scaling limits of traditional silicon technology. The combination of atomic thickness, high carrier mobility, and a tunable bandgap allows these materials to be engineered for specific functionalities that are often difficult to achieve in 3D systems. This section explores the emerging applications of 2D materials-based devices, focusing on the architectures and performance metrics that characterize memory, logic, sensing, and neuromorphic platforms.

1.4.1 Non-volatile memory

The digital revolution has transformed data into the most valuable resource of the 21st century, observing an unprecedented global demand for high-capacity and energy-efficient storage solutions. From the massive data centres powering cloud computing to the billions of interconnected sensors in the Internet of Things (IoT) and the real-time processing requirements of artificial intelligence, the ability to store and retrieve information reliably is a fundamental pillar of modern technology.[69] At the heart of this data-driven era lies the non-volatile memory (NVM), which is a class of storage that retains its state even after the external power supply is removed. This thesis explores the potential of 2D semiconductors, with their exceptional electrostatic control and atomically thin profiles, as the foundation for next-generation storage. Specifically, I have demonstrated the implementation of 2D-based non-volatile memory functionality through two distinct architectural approaches: the BG and FG FETs.

Before exploring more complex structures, it is essential to understand that NVM functionality can be achieved by exploiting the intrinsic properties of the 2D material/dielectric interface. As demonstrated in Chapter 3, BG FETs can function as NVM by utilizing the trapping and detrapping of charges at the interface between the 2D channel and the SiO_2 gate oxide, as well as within intrinsic defects in the material itself.

In this architecture, the memory state is not stored in a separate layer but is instead a result of the trapped charges at the 2D material/dielectric interface. The memory states are programmed and erased through the application of gate voltage pulses. A set operation is performed by applying a gate pulse of a specific polarity, which shifts the current to a higher (or lower) value, while a reset operation utilizes a pulse of the opposite polarity to change the current to its alternative logical state. The readout is typically performed at zero gate bias (V_{gs} = 0 V). The reliability of the memory is largely determined by the memory window that is the magnitude of the separation between the current levels corresponding to the 0 and 1 logical states. Beyond the window size, the performance is characterized by the retention time, which is the duration the programmed state remains stable after the pulse is removed, and the endurance, which quantifies the number of write/erase cycles the device can withstand. By eliminating the need for complex, multi-layered charge-trapping architectures, this approach significantly simplifies the fabrication process and reduces costs while still achieving the endurance and stability required for non-volatile storage applications.

To achieve higher precision and long-term stability beyond what interface traps can provide, the FG architecture can be used. This structure, which I also explore in this work (Chapter 5), adds an electrically isolated conductive layer, i.e. the floating gate, between the 2D channel and a control gate, separated by a thin tunnelling dielectric like hBN. Unlike the BG approach, which relies on unintentional traps, the FG architecture uses a tunnelling mechanism, such as Fowler-Nordheim or direct tunnelling, to inject charge into a dedicated storage layer. Once trapped, this charge is protected by the high-quality vdW interface of the hBN, leading to superior data retention.[70–72]Furthermore, the precise control of charge injection inherent in the FG architecture enables the definition of multiple discrete threshold voltage levels, facilitating the implementation of multilevel memory. By finely tuning the magnitude and duration of the programming pulses, the device can store more than one bit per cell, a capability that I demonstrate in the experimental results of this thesis (Chapter 5).[73] This development is crucial for significantly increasing information density and

provides a clear pathway toward the high-capacity, energy-efficient memory arrays required for modern data storage and neuromorphic applications.

1.4.2 Logic gates: inverter

Digital electronics represents the backbone of the modern information age, translating complex data into binary language of 0 and 1. This binary system is physically realized through the rapid switching of electrical signals between two discrete voltage levels, typically referred as the logic high and logic low states. At the hardware level, this logic is implemented using FETs that function as high-speed, voltage-controlled switches. By modulating the conductance of the semiconductor channel via a gate electrode, a transistor can either allow or block the flow of current, effectively mapping mathematical Boolean algebra onto physical circuitry. The primary objective in digital circuit design is to ensure that these logic states are clearly distinguishable and resistant to electrical noise, a requirement that demands transistors with high on/off current ratios and steep subthreshold swings. As traditional silicon-based logic reaches its physical scaling limits, the transition to 2D semiconductors offers a competitive alternative. Due to their atomic thickness and exceptional electrostatic control, 2D FETs can maintain high switching performance even at extremely short channel length. This makes them ideal candidates for the fundamental building blocks of digital logic.

The most essential of these building blocks is the logic inverter, or NOT gate. The inverter is the simplest circuit capable of performing a logic operation, taking a single input and producing its opposite as an output. The behaviour of more complicated gates, such as NAND, NOR or XOR, which are the building blocks for other modules like multipliers and processors, can be explained by extending the analysis of inverters. The inverter it typically achieved through two primary architectures: the resistor-load inverter and the (CMOS) inverter.

The resistor-load inverter is often the first step in evaluating 2D semiconductors, particularly when only one carrier type, either n-type or p-type, is readily available or dominant in the material. This configuration consists of a single drive transistor connected in series with a large passive load resistor (R_L). An inverter based on a resistor load and a n-type transistor operates by connecting the load resistor between the voltage supply, V_{dd}, and the output node, while the transistor is placed between the output and the ground, as schematized in Figure 1.14a.[21,74–76] The input voltage, V_{in}, corresponds to the voltage applied to the gate electrode, $V_{in} = V_{gs}$, and the output voltage, V_{out}, corresponds to the measured voltage between the source and drain electrodes of the transistor, $V_{out} = V_{ds}$. When the input at the gate is low, the transistor is turned off, no current flows to ground, and the output is pulled up to V_{dd} by the resistor, corresponding to a logic 1. Conversely, when the input is high, the transistor is switched on, providing a conduction path to the ground.[77–79] In this condition, the circuit can be viewed as a voltage divider between the load resistor (R_{HETO}) and the channel resistance (R_{FET}) of the transistor. If the transistor is strongly conducting, $R_{FET} << R_{HETO}$, the output is pulled close to the ground, corresponding to a logic 0.

As a complementary architecture of the traditional resistive load inverter circuit, it can also be realised by employing a p-type transistor as the pull-up device and a resistor connected to the ground as the load, as schematized in Figure 1.14b. In this configuration, when a low signal is applied to the gate electrode of the transistor, the p-FET is turned on and strongly conducts, pulling the output close to V_{dd}, corresponding to a logic 1. Conversely, when the input is high, the p-FET is turned off and the output is discharged through the load resistor to ground, resulting in a logic 0.

While simple to fabricate, this architecture suffers from high static power consumption, which is the power drawn by the inverter in steady state due to leakage currents, $P_{static} = V_{dd}I_d|_{fixed\ input}$, as current flows through the resistor whenever the transistor is in its on-state, and it often exhibits limited output voltage swing.

For high-performance digital logic, the CMOS inverter is the gold standard. It utilizes a complementary pair of transistors: a n-type FET (pull-down) and a p-type FET (pull-up). A schematic of such inverter circuit is reported in Figure 1.14c. In the context of this thesis, a CMOS inverter is realized by integrating pristine n-type $MoSe_2$ and p-doped $MoSe_2$/CrOCl FETs. The input voltage, V_{in}, corresponds to the voltage applied on the common gate electrode, and the output voltage, V_{out}, corresponds to the measured voltage at the connection node that is the source of the p-type transistor and the drain of the n-type transistor. When the input is low, the n-type transistor is off and the p-type transistor is on, forming a conduction path from V_{dd} to the output. As a result, the output is pulled up to V_{dd}, corresponding to a logic 1. Conversely, when the input is high, the n-type transistor is switched on while the p-type device is turned off, leading to a conduction path from the output to the ground. The output is then pulled down close to 0 V, corresponding to a logic 0. The primary advantage of the CMOS architecture is its negligible static power consumption; since one transistor is always in its off-state when the other is in its on-state, current only flows during the brief switching transition. This efficiency, combined with full rail-to-rail logic swings, makes CMOS the foundation of modern integrated circuits.

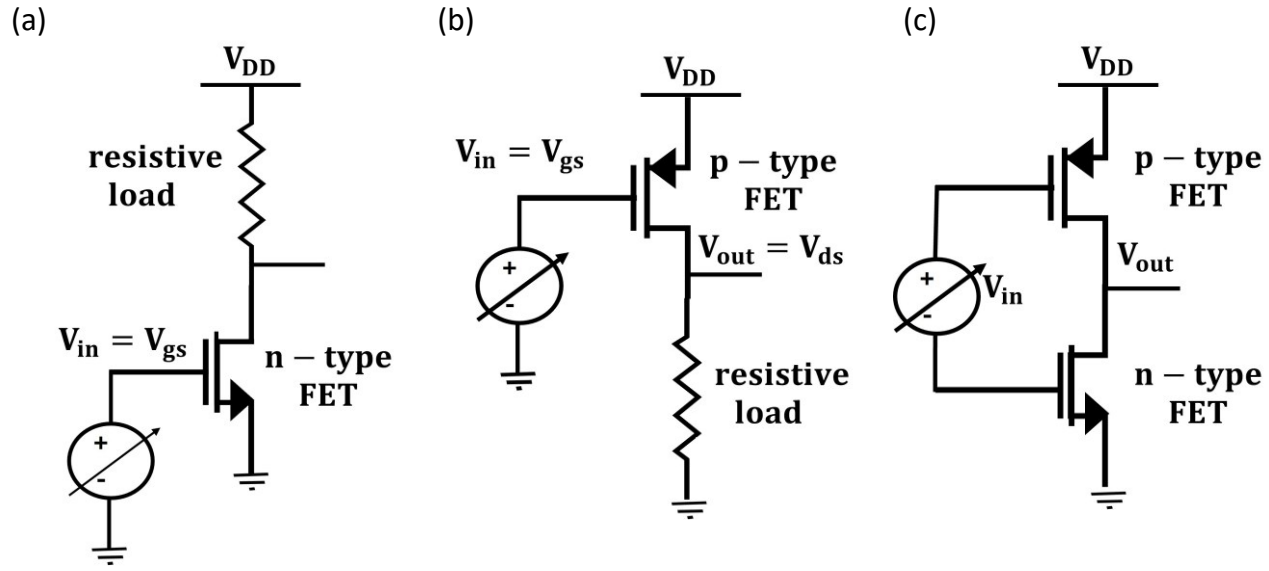


Figure 1.14: Schematic of a resistive-load inverter with a (a) n-type FET and (b) p-type FET. (c) Schematic of a CMOS inverter with a n-type and a p-type FET connected in series.

The performance of an inverter is characterized by its Voltage Transfer Characteristic (VTC), which plots the V_{out} as a function of V_{in}. From this curve, several critical figures of merit can be extracted. the threshold voltage, V_T, of the inverter indicates the point where the inverter changes its logic state. It is the input voltage at which $V_{in} = V_{out}$. In an ideal and symmetric inverter, this occurs at exactly $V_{in} = V_{out} = ½\ V_{DD}$, ensuring balanced switching speeds for both low-to-high and high-to-low transitions. [20,80] In the case of not equal V_{in} and V_{out} ranges, V_T is found as the intersection of the VTC and the line with equation $V_{out} = aV_{in}$, where a is the ratio between the output and input ranges.

The gain of an inverter is defined as the maximum slope of the VTC during the switching transition, $\text{gain} = \left|\frac{dV_{out}}{dV_{in}}\right|$. A gain greater than unity is a fundamental requirement for signal restoration and for cascading multiple gates without signal degradation. In the case of not equal V_{in} and V_{out} ranges, the gain must be greater than the ratio between the output and input ranges, gain >> a.[81,82]

The noise margins for the high and low levels, NM_H and NM_L, respectively, quantify the inverter's ability to tolerate electrical noise on the input without changing the logic state of the output. High noise margins ensure that the digital 0 and 1 remain stable in noisy environments. They are defined as $NM_H = V_{OH} - V_{IH}$ and $NM_L = V_{IL} - V_{OL}$, where V_{IL} and V_{IH} are defined as the maximum and minimum input voltage considerable as logical 0 and 1, respectively. The corresponding output voltages, V_{OH} and V_{OL}, are defined as the maximum and minimum output voltages considerable as logical 1 and 0, respectively. In the case of not equal V_{in} and V_{out} ranges, the input voltage values can be rescaled accordingly to the output voltage range, then having $NM_H = V_{OH} - V_{IH}^*$ and $NM_L = V_{IL}^* - V_{OL}$, indicating with the * symbol the modified values. To ensure optimized tolerance to electrical noise, the noise margins must be at least 10% of V_{DD}.[20,83] Figure 1.15 shows a VTC of an inverter with some characteristic points depicted.

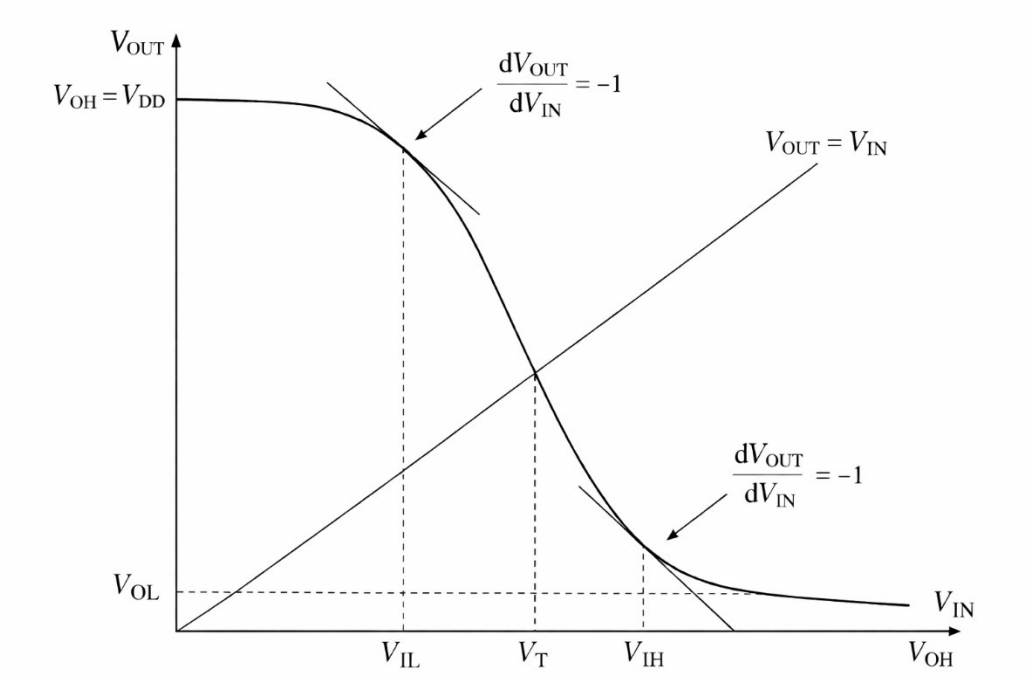


Figure 1.15: VTC of an inverter with some characteristic points depicted.

1.4.3 Pressure sensor: adsorption/desorption of air molecules on 2D materials' surface

In this section, the fundamental interactions between the environment and the surface of 2D semiconductors are discussed. This serves as the physical basis for the pressure-sensing applications explored in this thesis (Chapter 4).

Due to their atomic thickness, 2D materials exhibit an extremely high surface-to-mass ratio, ensuring that both the constituent atoms and intrinsic atomic defects are exposed to, and influenced by, the surrounding atmosphere. The interaction between air molecules and 2D materials can be broadly categorized into two regimes: physisorption and chemisorption. Most common atmospheric constituents, including nitrogen (N_2), carbon dioxide (CO_2), and water vapor (H_2O), interact with the

2D surface through weak vdW forces. These molecules are typically located at distances greater than 2 Å from the surface with adsorption energies typically less than 0.2 eV. This weak coupling makes physisorption highly reversible and sensitive to changes in ambient pressure and temperature: the molecules can easily desorb or diffuse away from the defect sites. In contrast, certain molecules like oxygen (O_2) can undergo chemisorption, particularly at defect sites such as chalcogen vacancies (V_x). This process is strongly exothermic, with energy reduction exceeding 1.5 eV that induces a permanent modification of the material's electronic structure (Figure 1.16a). Because the chemisorbed O_2 cannot be released under ambient conditions, this interaction effectively results in an irreversible transformation of the defect properties. This chemisorption process transforms V_x sites from detrimental carrier traps into electronically inactive configurations. This transition, rooted in the isoelectronic nature of the O_2-metal bond compared to the original chalcogen-metal bond, offers a facile strategy for defect passivation and enhancement of 2D device performance through controlled environmental exposure. The adsorption energy is defined as:

$$\mathrm{E_{ad}} = \mathrm{E(V_x + mol)} - \mathrm{E(V_x)} - \mathrm{E(mol)}$$

Where E(V_x + mol) is the energy of the system with a molecule adsorbed on the V_x site, and $\mathrm{E(V_x)}$ and E(mol) are the energies for isolated systems. According to the rate theory, the transition time from the physiosorbed state to chemisorbed state is:

$$\tau \approx \frac{1}{\mathrm{fe}^{-\frac{E_b}{k_B T}}}$$

where f is attempting frequency, $\mathrm{E_b}$ is the barrier, $\mathrm{k_B}$ is the Boltzmann constant, and T is the temperature. The f can be estimated by the flux of O_2 arriving at the V_x: $\mathrm{f \approx nvs_d}$, where n is O_2 density in air, v is the speed of O_2 molecule, and $\mathrm{s_d}$ is the cross section of V_x, which can be taken as the square of lattice parameter. At room temperature and one atmospheric pressure, f is about 10^8 molecules s^{-1}, which gives t ≈ 20 h for MoS_2.

The kinetic feasibility of O_2 chemisorption at V_x sites is closely related to the thermodynamic stability of the host semiconductor. It can be observed that the energy barriers for chemisorption decrease in correlation with the cohesive energy of the material (Figure 1.16b). Fundamentally, a lower cohesive energy represents a less stable lattice, which exhibits a stronger thermodynamic driving force to chemisorb O_2 at V_x sites. For a given cation, the activation barriers decrease as we move down the chalcogen group, from S to Se to Te; for a given anion, the barriers increase across the transition metals from Ga to Mo to W. As a result of these trends, WS_2 exhibits the highest calculated barrier (0.97 eV), rendering O_2 chemisorption kinetically forbidden at room temperature. In such cases, thermal activation or specialized treatments are required to overcome the barrier and initiate the passivation process.

While chemisorption at V_x sites is beneficial, O_2 molecules that are merely physiosorbed on the pristine basal plane can introduce non-uniform potential fluctuations and act as scattering centres for charge carriers. Therefore, to realize the full benefits of defect passivation, it is essential to remove these weakly bound physiosorbed molecules, e.g. through vacuum annealing or inert gas pumping, after the treatment process to prevent them from compensating for the improvements in defect properties.

Figure 1.16b shows the chemisorption barrier as a function of cohesive energy for different 2D semiconductors, calculated by using different methods. The barriers decrease as the cohesive energy of the semiconductor decreases.

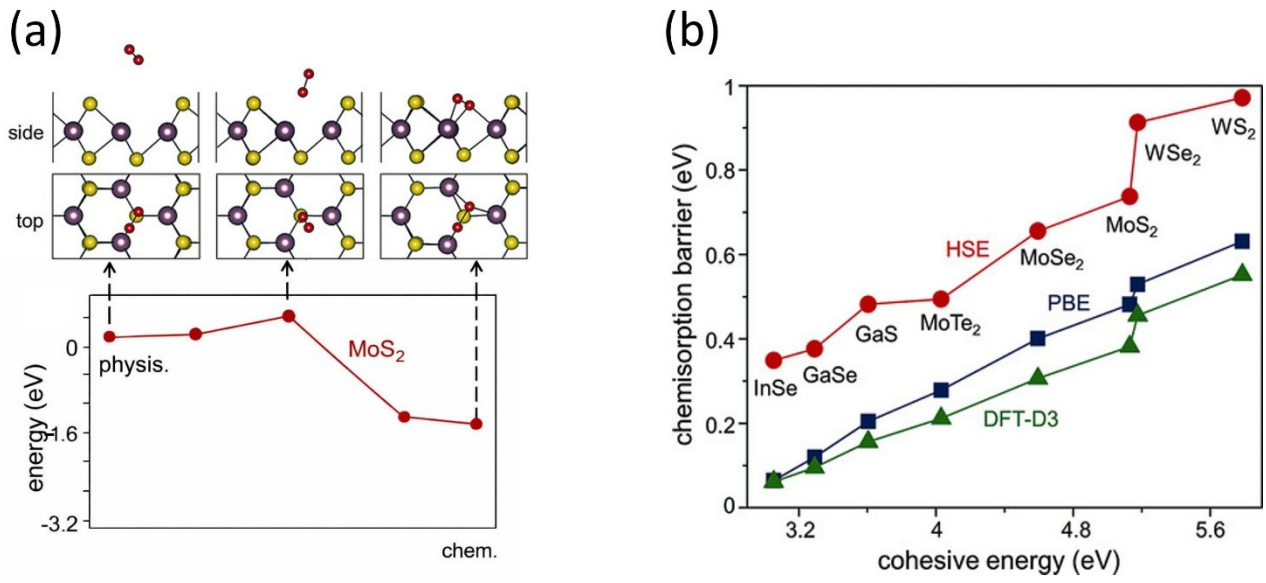


Figure 1.16: (a) Transition from physiosorbed to chemisorbed O_2 to V_x of MoS_2 with the energy evolution during the reaction, calculated by using the Perdew-Burke-Ernzerhof (PBE) exchange-correlation functional.[84] (b) O_2 chemisorption barriers at Vx for various 2D semiconductors, calculated by using PBE and other methods. Adapted from [85].

1.4.4 Photodetectors

2D vdW semiconductors have emerged as a disruptive platform for next-generation optoelectronics, offering a unique set of properties that address the fundamental limitations of traditional bulk materials like silicon. While bulk silicon photodetectors are limited by an indirect bandgap and require thick, opaque channels to achieve sufficient absorption, 2D materials provide a path toward transparent, flexible, and high-performance devices.[86] Key advantages of 2D materials for photodetection include strong light-matter interaction, bandgap tunability, and mechanical and structural flexibility. Indeed, despite their atomic thickness, 2D materials exhibit remarkably high absorption efficiencies, often enhanced by van Hove singularities in their density of states. In several 2D semiconductors, these singularities happen close to the conduction and valence band edges. Therefore, a photon with energy close to the bandgap has an increased probability to excite an electron-hole pair due to the large availability of empty states given by the diverging density of states at the singularity.[87] Additionally, the electronic properties of these materials are highly sensitive to the number of layers due to quantum confinement. For instance, most of TMDs transition from an indirect bandgap in bulk to a direct bandgap in the single layer, as described previously. The wide range of material properties, together with the possibilities for combining 2D materials with different layer numbers and compositions, allows for the realization of various nanophotonic devices and the exploration of fundamental optical sciences, covering a wide spectral range from the microwave to the ultraviolet (Figure 1.17). Finally, these materials can withstand large strains and lack surface dangling bonds, allowing them to be integrated into flexible architectures or stacked into complex vdW heterostructures without lattice mismatch constraint.

The conversion of light into electrical signals in 2D-based devices occurs through several distinct physical mechanisms, which can be broadly categorized as either driven by carrier separation of thermal processes. The mechanisms particularly relevant to (photo)FETs are the ones driven by electric field separation of electron-hole pairs generated by photon absorption. They include the photoconductive, photogating and photovoltaic effects.

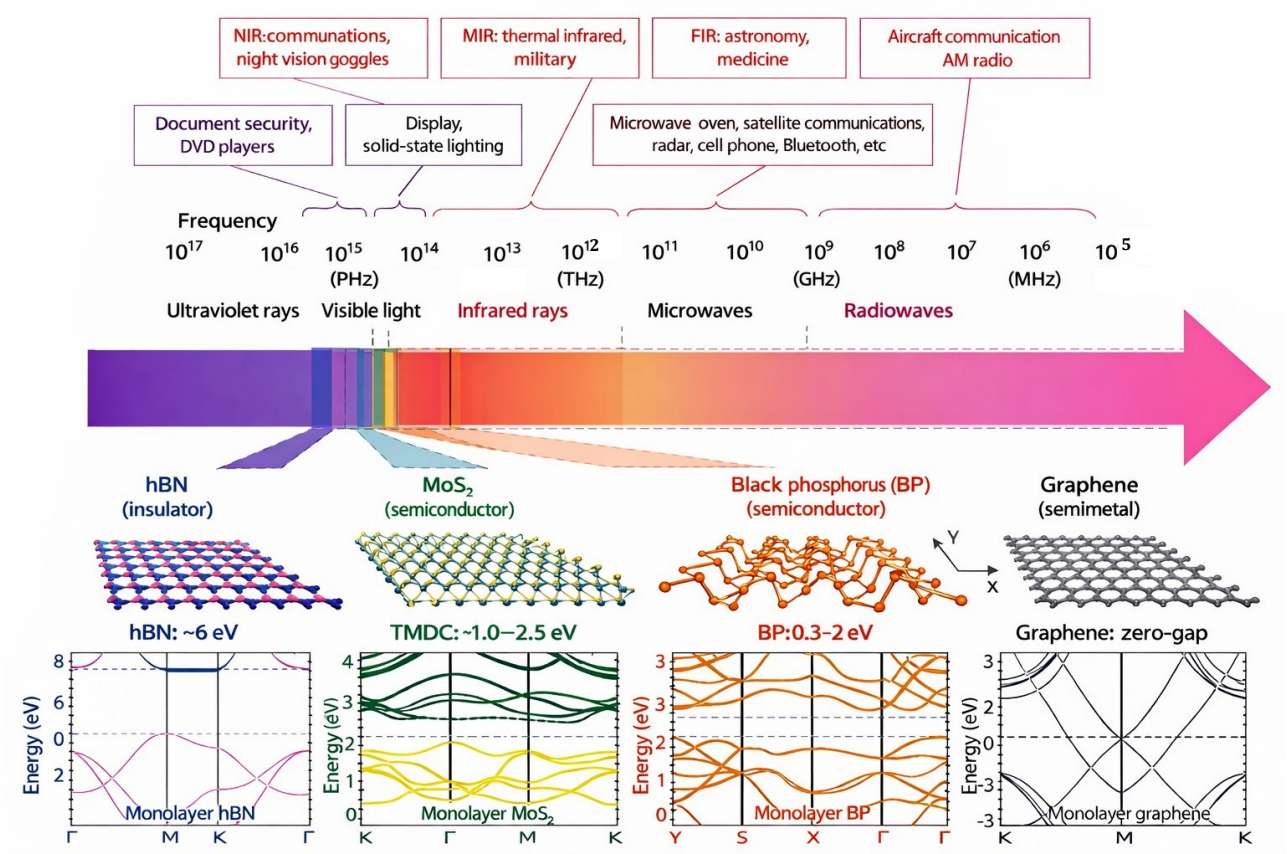


Figure 1.17: Spectral range of 2D materials. Applications that utilize the different spectral ranges are presented in the top portion of the panel. NIR, MIR and FIR indicate near-, mid- and far- infrared, respectively. The atomic structures oh hBN, MoS_2, bP and graphene are shown in the bottom of the panel, together with their electronic band structures (single layer). Adapted from [88].

1.4.4.1 Photoconductive effect

The photoconductive effect, which is the most common mechanism in 2D materials-based FETs, is characterized by the modulation of a semiconductive channel's electrical resistance through the generation of additional free charge carriers upon light absorption. In a standard FET configuration, a baseline current, I_{dark}, flows between the source and drain electrodes under a given bas in the absence of light (Figure 1.18a). When the device is illuminated with photons possessing energy greater than the material's bandgap, electron-hole pairs are generated within the channel. The external electric field provided by V_{ds} facilitates the separation of these pairs, driving the photogenerated electrons and holes in opposite directions. This movement results in a supplementary photocurrent, I_{ph}, that adds to the initial dark current (Figure 1.18b). Consequently, the total resistance of the device decreases under illumination, a transition that is typically visualized as a vertical shift of the transfer and output characteristics (Figure 1.18c-d).

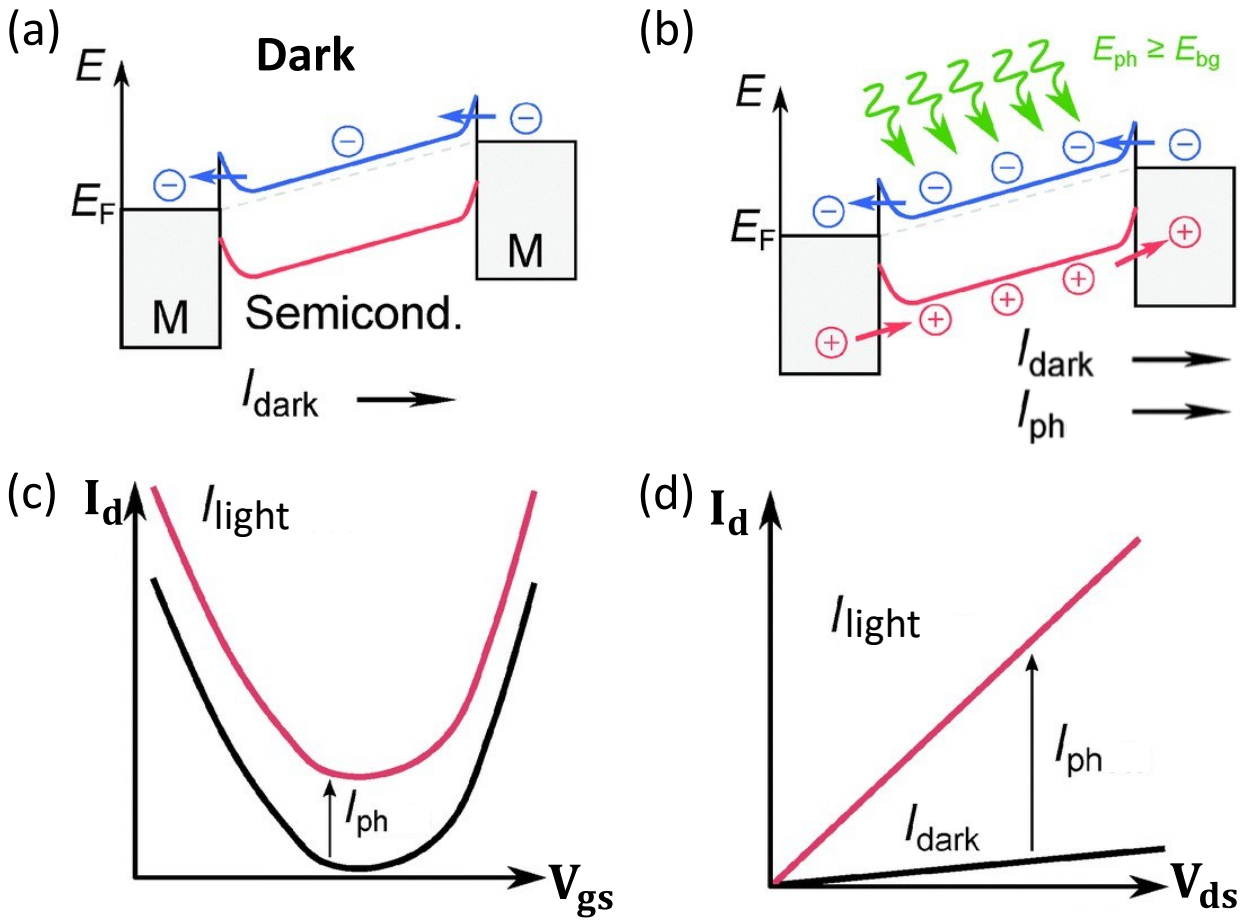


Figure 1.18: Schematic of the photoconductive effect. Band alignment for a semiconductor channel contacted with two metals under an external bias (a) without illumination and (b) under illumination. (c) Transfer characteristic in the dark (solid black line) and under illumination (solid pink line). (d) I-V characteristic in the dark (solid black line) and under illumination (solid pink line). Illumination results in an increase in the conductivity and a positive photocurrent. Partially reproduced with permission from Royal Society of Chemistry.[86]

1.4.4.2 Photogating effect

The photogating effect can be understood as a specialized manifestation of the photoconductive mechanism, where the modulation of a material's resistance is driven by the localized trapping of one carrier type. In 2D semiconductors, the high surface-to-volume ratio and reduced electrostatic screening make them particularly susceptible to this effect. When electron-hole pairs are generated by incident light, one type of carriers (e.g. holes) may become captured in localized trap states, which are typically associated with structural defects, surface adsorbates, or the semiconductor/dielectric interface (Figure 1.19a-b). These trapped charges act as a local gate, exerting an additional electric field that effectively shifts the Fermi level of the 2D channel. Physically, this is observed as a horizontal shift in the transistor's transfer characteristic under illumination. For example, the trapping of holes near the valence band edge creates a positive local potential that induces an increase in electron density in the channel, shifting the threshold voltage toward more negative values. This increase in carrier density leads to a significant rise in photocurrent (Figure 1.19c).

A defining characteristic of photogating effect is its impact on photoconductive gain (G), which is defined as the ratio of the photogenerated carrier lifetime ($\tau_{photocarriers}$) and the transit time ($\tau_{transit} = L^2/\mu V_{ds}$):

$$G = \frac{\tau_{photocarriers}}{\tau_{transit}} = \frac{\tau_{photocarriers}\mu V}{L^2}$$

It is evident that large $\tau_{photocarriers}$ and large mismatch in the electron/hole mobility yield large G. Since the lifetime of the photocarriers is determined by the long recombination times of the localized trap states rather than the fast transit time across the channel, the device can exhibit exceptionally high gain and responsivity. However, this often comes at the expense of bandwidth, as the slow release of carriers from these traps results in longer response times. Furthermore, the polarity of the trapped carrier dictates the direction of the horizontal shift; while positive charge trapping typically increases conductance in n-type devices, the trapping of the majority carrier can lead to a negative photocurrent, where the light-induced shift effectively depletes the channel and reduces the total current. (Figure 1.19d)

Both the photoconductive and photogating effects can take place in the same device. The difference in their time scales can be used to distinguish their signatures.[89]

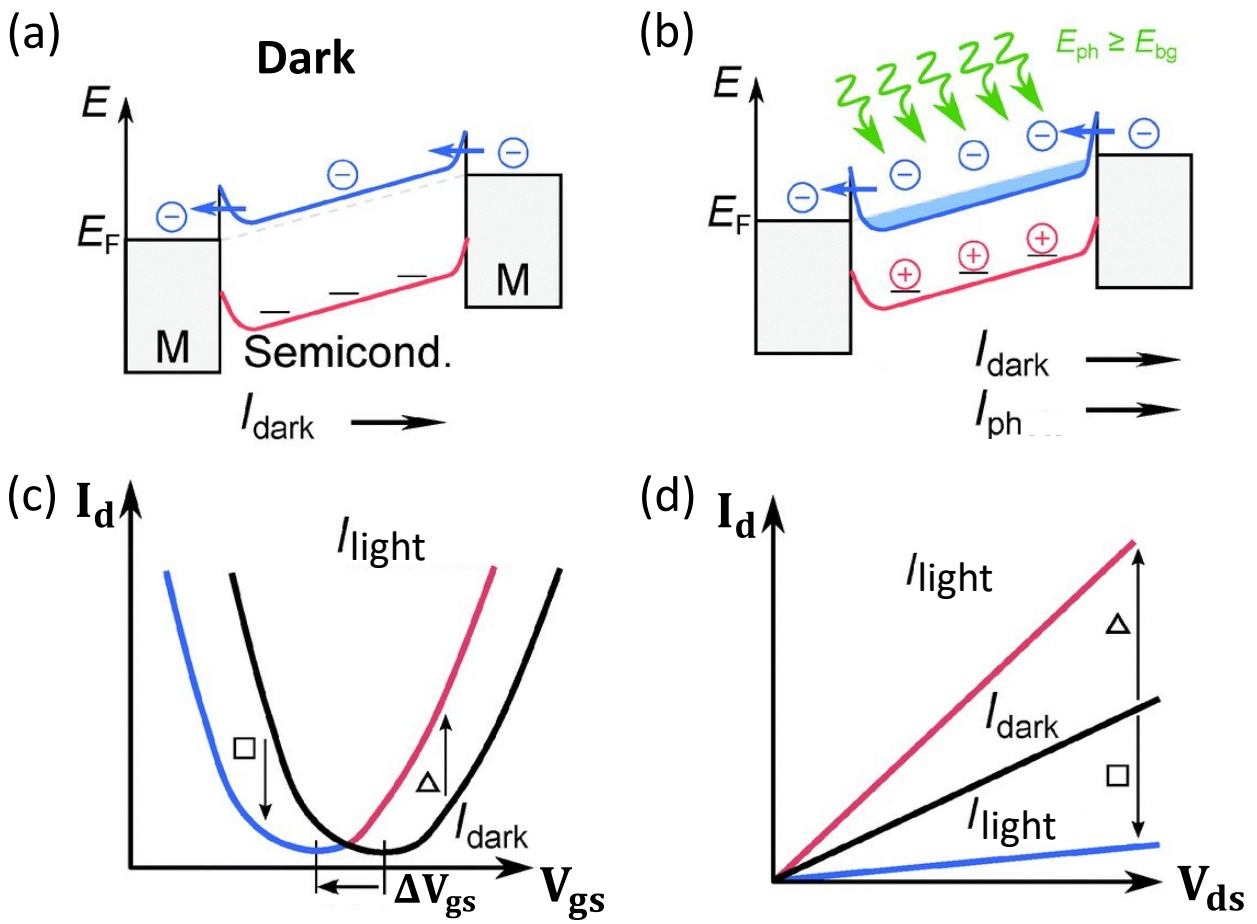


Figure 1.19: Schematic of the photogating effect. Band alignment for a semiconductor channel contacted with two metals under an external bias (a) without illumination and (b) under illumination. the solid horizontal segments represent trap states at the valence band edge. (c) Transfer characteristic in the dark (solid black

line) and under illumination (solid blue/pink line). (d) I-V characteristic in the dark (solid black line) and under illumination at the gate voltage marked by a triangle in panel (c) (solid pink line) and at gate voltage marked by a square in panel (c) (solid blue line). Illumination results in positive photocurrent for one gate voltage (triangle marker) and negative photocurrent for another gate voltage (square marker). Partially reproduced with permission from Royal Society of Chemistry.[86]

1.4.4.3 Photovoltaic effect

The photovoltaic effect is a fundamental photodetection mechanism in which photogenerated electron-hole pairs are separated by a built-in internal electric field rather than an external bias. In 2D-based devices, this internal field typically originates at the depletion region of a p-n junction or at the Schottky barrier formed at a metal-semiconductor interface (Figure 1.20a).

In the absence of light, these junctions exhibit non-linear, rectifying I-V characteristics. For a p-n junction, the dark current follows an exponential relationship under forward bias, while the reverse current remains negligible until the point of junction breakdown. Upon illumination, photons with energy exceeding the bandgap generate charge carriers that are immediately swept in opposite directions by the junction's internal electric field.

If the device is held at zero external bias, V_{ds} = 0 V, this carrier separation produces a measurable short-circuit current (I_{sc}). Conversely, if the circuit remains open, the accumulation of carriers of opposite polarities in distinct parts of the device generates a potential difference known as the open-circuit voltage (V_{oc}). Graphically, illumination causes the I-V curve to shift downward, moving a portion of the characteristic into the fourth quadrant (negative current, positive bias) (Figure 1.20b). This region critical as it represents the regime where the device can convert optical energy into electrical power, making the photovoltaic effect the operational basis for 2D-based solar cells.

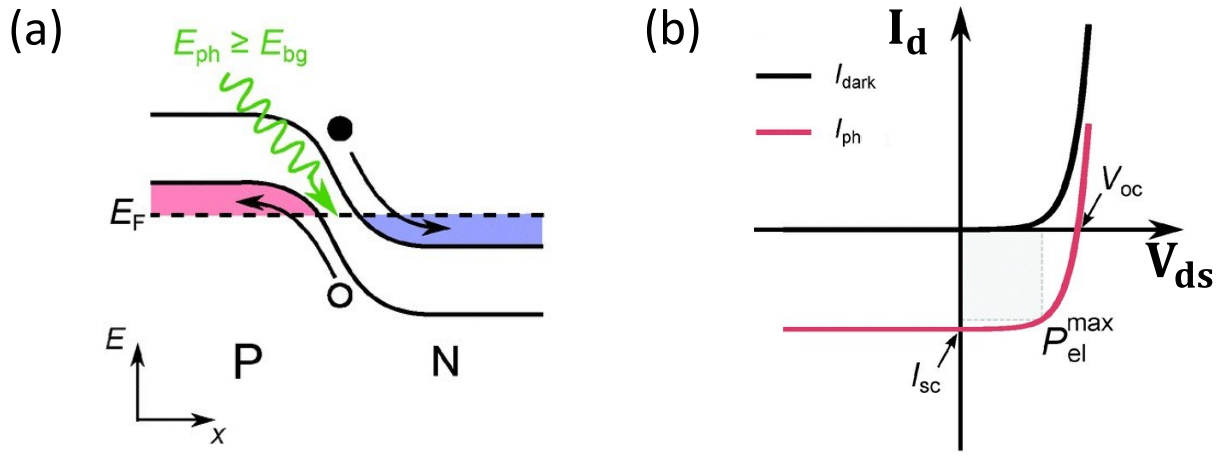


Figure 1.20: Schematic of the photovoltaic effect. (a) Band alignment in a pn- junction. The dashed line represents the common Fermi level for the p-doped and the n-doped semiconductor. (b) I-V characteristic in the dark (solid black line) and under illumination (solid pink line). The illumination results in a short-circuit current and an open-circuit voltage. P_{el}^{max} is the point of maximum power generation. Partially reproduced with permission from Royal Society of Chemistry.[86]

Photovoltaic-based detectors generally operate in photovoltaic mode or photoconductive mode. The photovoltaic mode (V_{ds} = 0 V) is characterized by the lowest possible dark current, which significantly enhances the device's detectivity (detailed in the next section). However, because there is no internal gain mechanism, unlike the photogating effect, the absolute responsivity is typically

lower. The photoconductive mode consists of the application of a reverse bias. Applying a reverse bias increases the width of the depletion region and reduces junction capacitance, which facilitates higher operational speeds. Under high reverse bias, the intensified electric field can trigger impact ionization or avalanching. In such avalanche photodiodes, a single photogenerated carrier can trigger a cascade of secondary carriers, providing a large internal gain that allows for the detection of extremely low-power optical signals.

Unlike the photoconductive or photogating effects, which rely on modulating a pre-existing current, the photovoltaic effect offers the unique advantage of self-powered operation, making it an essential component for energy-autonomous 2D electronic systems.

1.4.4.4 Photocurrent generation driven by thermal mechanisms

Beyond the direct separation of electron-hole pairs, photocurrent can also be generated or modulated through thermal processes induced by light absorption. These mechanisms are particularly relevant in 2D materials where the electronic properties are highly sensitive to temperature and local heating.

The photo-thermoelectric effect arises when non-uniform illumination creates a temperature gradient (ΔT) across the semiconductor channel. This gradient is converted into a voltage difference (ΔV) through the Seebeck effect, which is also known as thermoelectric effect.[90] A temperature gradient typically stems from either localized illumination, such as a focused laser spot smaller than the device, or a significant difference in light absorption across distinct parts of the device under global illumination. The resulting photovoltage (ΔV_{PTE}) is proportional to the difference in the Seebeck coefficients (S) of the materials and the temperature difference: $\Delta V_{PTE} = (S_2 - S_1)\Delta T$. In metal-semiconductor-metal FETs, the contribution from the metal is often negligible ($S_{metal} << S_{semiconductor}$), simplifying the response to $\Delta V_{PTE} \approx S_{semiconductor}\Delta T$. ΔT can be estimated via finite element simulations or measured with on-chip thermometers. Once ΔT is known, it is possible to estimate the Seebeck coefficient of the semiconductor material.[91] ΔV_{PTE} generally ranges from tens of μV to tens of mV. Efficient charge transport within the device necessitates the formation of low-resistance ohmic contacts at the metal-semiconductor interfaces. In a homogeneous semiconducting channel, focused illumination fails to produce a net photocurrent in the absence of an external bias. This is due to the lack of a driving force, such as a built-in potential or a significant thermal gradient, required to direct the motion of photogenerated carriers.

Unlike the photo-thermoelectric effect, which relies on a temperature gradient, the photo-bolometric effect is driven by a homogeneous change in the material's temperature due to photon absorption. The heating of the entire channel leads to a change in the material's electrical resistivity. The magnitude of the bolometric response depends on the temperature-induced conductance variation and the total temperature increase caused by laser heating. This mechanism is the fundamental principle behind many high-performance detectors in the mid- and far-infrared spectrum, where direct electron-hole excitation is less efficient.[92]

1.4.4.5 Figures of merit of a photodetector

To provide a rigorous framework for evaluating the performance of photodetectors working with different principles and realized with different materials and geometries, it is essential to define the key figures of merit that characterize photodetector performance. In the context of 2D materials,

hwere light-matter interactions and charge transport mechanisms differ significantly from bulk semiconductors, these metrics must be reported with particular attention to standardization.

PHOTOCURRENT The most fundamental metric is the photocurrent (I_{ph}), defined as the additional electrical current generated in a device upon exposure to incident light. It is calculated by subtracting the dark current (I_{dark}), measured in the absence of illumination, from the total current under illumination (I_{light}):

$$I_{ph} = I_{light} - I_{dark} \tag{1.7}$$

RESPONSIVITY The responsivity (R) quantifies the efficiency of the photodetector in converting incident optical power (P_{inc}) into an electrical signal. A large responsivity indicates a large electrical output signal for a defined optical excitation power. For a current-based response, it is expressed as:

$$R = \frac{I_{ph}}{P_{inc}} = \frac{I_{ph}}{\left(\frac{P_\lambda A_{device}}{A_{spot}}\right)} \tag{1.8}$$

Where P_λ is the nominal laser power at a given wavelength λ, A_{device} is the active area of the device and A_{spot} is the area of the laser spot.

TIME RESPONSE The response speed of a photodetector is typically characterized by the rise time (τ_{rise}) and fall time (τ_{fall}), which represent the time required for the signal to transition between the 10% and 90% of its peak value. Physically, τ_{rise} gives information on the generation and separation of carriers, while τ_{fall} accounts for the recombination or extraction of these carriers once the light source is removed. In 2D materials, slow response times (from the milliseconds to seconds) often indicate the presence of long-lived trap states or photogating mechanisms, whereas fast responses (in the range from ns to μs) are typical of photovoltaic or bolometric mechanisms. In the presence of trap states, a double exponential fit for a 2D material photodetector's light pulse response typically models the rise and decay of photocurrent, revealing different carrier dynamics like fast photogating/trapping (short time constant, τ_1) and slower recombination/detrapping from defects or interfaces (long time constant, τ_2), essential for understanding performance bottlenecks like slow fall times, especially in heterostructures, and optimizing devices for high-speed optical communications or imaging. The general double exponential model is expressed as:

$$I_d = A_1 e^{-\frac{t}{\tau_1}} + A_2 e^{-\frac{t}{\tau_2}} \tag{1.9}$$

where A_1 and A_2 are the amplitudes of the exponential components, and τ_1 and τ_2 are the time constants, with $\tau_1 < \tau_2$. The fast component is often linked to direct electron-hole recombination, rapid photogating, fast carrier collection, contributing to quick response times, whereas the slow component is frequently attributed to slower processes like defect-mediated trapping/detrapping, charge accumulation at interfaces or carrier recombination, which can limit the overall speed. [93,94]

SPECIFIC DETECTIVITY The specific detectivity (D^*) is a normalized figure of merit that characterizes the sensitivity of a detector, accounting for the device area and the noise equivalent power (NEP), which is the minimum illumination power that delivers a unity signal-to-noise ratio at 1Hz bandwidth. D^* is measured in Jones, where 1 Jones = 1 cm $Hz^{1/2}$ W^{-1}, and is defined as:

$$D^* = \frac{\sqrt{A\Delta f}}{NEP} = \frac{R\sqrt{A}}{i_n} \tag{1.10}$$

where Δf is the bandwidth and i_n is the noise current. When the noise is assumed to be dominated by shot noise from the dark current $\left(i_{shot} = \sqrt{2qI_{dark}}\right)$, equation 1.10 can be simplified to[95]:

$$D^* = \frac{R\sqrt{A}}{\sqrt{2qI_{dark}}} \quad (1.11)$$

EXTERNAL QUANTUM EFFICIENCY The external quantum efficiency (EQE) represents the ratio of the number of collected charge carriers to the number of incident photons. It is a dimensionless quantity related to responsivity by the following relation:

$$EQE = R\frac{hc}{q\lambda} \quad (1.12)$$

Where h is the Planck's constant, c is the speed of light, q is the elementary charge, and λ is the incident wavelength. While EQE accounts for the spectral dependence of photodetection, it does not account for internal losses such as reflection or transmission, which are instead captured by the internal quantum efficiency (IQE). This last figure of merit is defined as the number of measured charge carriers divided by the number of absorbed photons.

1.4.5 Artificial synaptic devices

The transition from traditional Von Neumann architecture toward neuromorphic computing is driven by the need for energy-efficient, parallel-processing systems capable of handling the demands of artificial intelligence and big data. Central to this paradigm shift is the development of artificial synaptic devices, i.e. electronic components that can emulate the signal transmission and memory functions of biological synapses. 2D materials provide an ideal platform for implementing these functions by using different strategies based on electronic and optoelectronic features. By exploiting charge-trapping mechanisms and light-matter interactions, 2D-based devices can replicate the complex plasticity of the human brain, offering a path toward ultra-compact, low-power neuromorphic hardware.

To establish a framework for the synaptic performance of our devices, we first examine the mechanisms of biological synapses and their electronic counterparts that exploit the persistent photoconductivity and the floating-gate architecture of the device.

1.4.5.1 The biological synapse: signal transmission and plasticity

Neurons are the specialized functional units of the nervous system, designed to process and transmit information via complex electrical and chemical signalling. Morphologically, a typical neuron consists of a central cell body (soma), containing the nucleus and essential organelles, an elaborate arborization of dendrites that receive incoming signals, and a single axon that propagates output signals toward other cells. The communication between neurons occurs at specialized junctions known as synapses, which connect the axon terminal of a presynaptic neuron to the dendrites (or soma) of a postsynaptic neuron. Synapses are broadly categorized into two types: electrical and chemical synapses. Electrical synapses are characterized by gap-junction channels that provide direct physical continuity between the cytoplasm of adjacent neurons, allowing for the rapid, bidirectional passage of ions.[96] In chemical synapses, which are the most abundant type in the

mammalian nervous system, no direct physical contact exists. Instead, a synaptic cleft separates the communicating cells.

The signalling process in a chemical synapse is initiated when an action potential reaches the presynaptic terminal, triggering the opening of voltage-gated Ca^{2+} channels. The resulting influx of Ca^{2+} ions drives synaptic vesicles to fuse with the presynaptic membrane and release neurotransmitters into the cleft. These molecules diffuse across the gap and bind to specific receptors on the postsynaptic membrane, modulating the permeability of ion channels (Figure 1.21).[97] The excitability of a neuron is governed by the electrochemical potential difference across its membrane, maintained by the unequal distribution of ions: K^+ is sequestered inside the cell, while Na^+ and Cl^- are more concentrated in the extracellular fluid. This gradient establishes a resting potential of approximately -70 mV. Depending on the neurotransmitter-receptor pairing, the synapse can be excitatory or inhibitory. Excitatory synapses typically depolarize the postsynaptic membrane, bringing its potential closer to the threshold for firing an action potential. They usually open cation channels, such as Na^+ or Ca^{2+}, generating an excitatory postsynaptic potential (EPSP). On the contrary, inhibitory synapses hyperpolarize or stabilize the membrane, making it less likely to reach the action-potential threshold. They commonly open Cl^- or K^+ channels, producing an inhibitory postsynaptic potential (IPSP). These potentials are integrated at the axon hillock, which is the initial segment of axon adjacent to the soma; if the cumulative stimulus surpasses a specific threshold, a new action potential is initiated.[98,99] While these mechanisms describe how signals are transmitted across synapses, the strength and efficacy of synaptic connections are not fixed. The capacity of these connections to strengthen or weaken over time in response to neuronal activity is known as synaptic plasticity. This process underlies learning and memory and is classified as either short-term plasticity or long-term plasticity, corresponding to transient or enduring changes in synaptic strength, respectively. Both forms can manifest as potentiation or depression, reflecting an increase or decrease in the postsynaptic potential. Short-term potentiation (STP) arises from repeated or rapid stimulations that temporarily increase synaptic strength. When the stimulation is sufficiently intense or sustained, STP can evolve into long-term potentiation (LTP), a lasting increase in synaptic efficacy. Analogously, when synaptic strength decreases, the process is referred to as short-term depression (STD) or long-term depression (LTD).

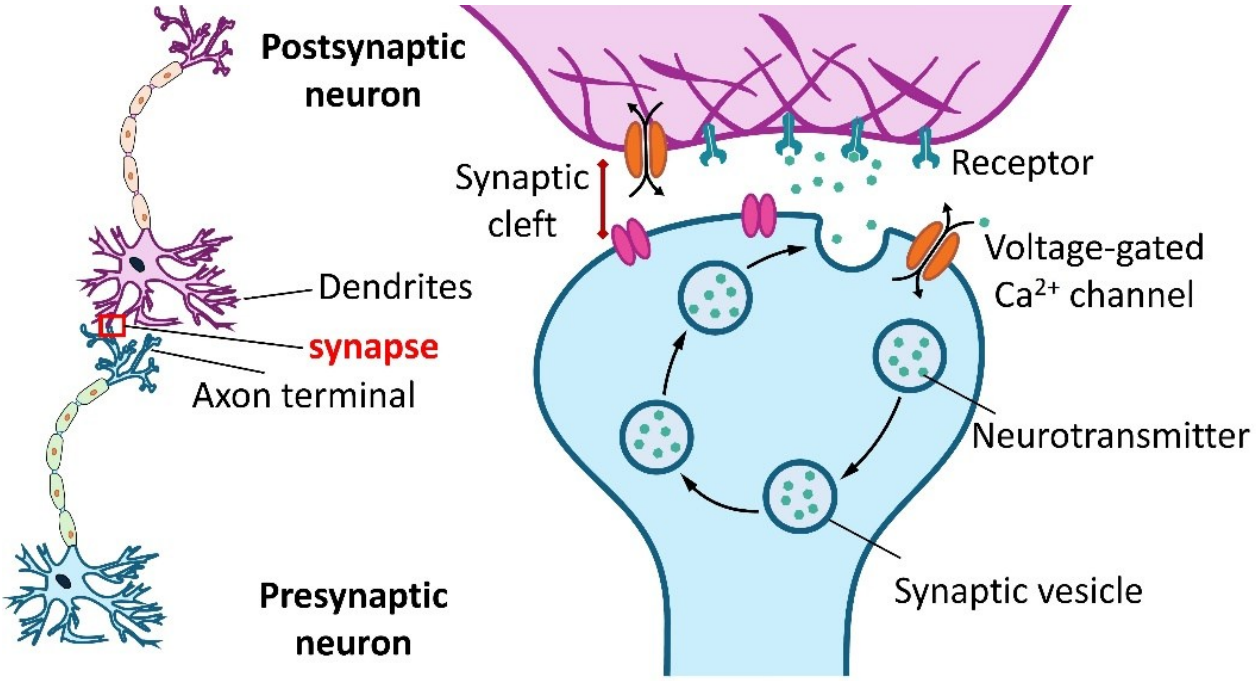


Figure 1.21: Schematic of a biological synapse.

1.4.5.2 Synaptic functions in floating-gate architectures

To replicate the synaptic functions in a solid-state device, floating-gate FETs are employed. In these architectures, a conductive or semiconductive gate is sandwiched between a tunnel oxide and a blocking oxide, isolated from the rest of the circuit. By applying a voltage pulse to the control gate, charge carriers are injected into or ejected from the floating gate via Fowler-Nordheim tunnelling or hot-carrier injection. The amount of stored charge in the floating gate shifts the threshold voltage of the transistor, thereby modulating the channel conductance.[100] This conductance represents the synaptic weight. Just as the brain adjusts synaptic strength through neurotransmitter flow, the floating-gate FET adjusts its weight through precise charge storage, enabling the emulation of LTP and LTD. The synaptic weight, i.e. the strength of the connection between neurons, is dynamic rather than fixed. It is constantly changing, adapting to past synaptic activity and other influences. This dynamic nature is the foundation for how the brain learns, forms memories, and adapts. The long-term synaptic relative weight change is associated with the change in the device conductance due to electrical pulses on the control gate electrode; so, it is defined[101] as:

$$\frac{\Delta W}{W} = \frac{I_n - I_0}{I_0} \qquad (1.13)$$

where I_n is the EPSC after the n-th pulse and I_0 is the baseline current.

1.4.5.3 Synaptic functions in 2D FETs with PPC

In optoelectronic devices, the temporal dynamics of biological synapses are often emulated through persistent photoconductivity (PPC). PPC is a phenomenon where the conductivity of a material remains higher that its dark state value for a prolonged period after the light source is removed. In 2D heterostructures, PPC typically originates from the slow recombination oh photogenerated carriers, often due to the presence of deep-level trap states or the spatial separation of electron-hole pairs at a vdW interface. When a device exhibiting PPC is triggered by a light pulse (the presynaptic stimulus), the resulting increase in conductance does not vanish instantly. The slow

decay characteristic of PPC naturally mimics the forgetting curve of the human brain. By adjusting the intensity, duration, or frequency of light pulses, one can transition the device from short-term memory (STM), where the conductance returns to baseline, to long-term memory (LTM), where the persistent state remains stable over time.[93,102]

2. EXPERIMENTAL TECHNIQUES AND METHODOLOGY

Building upon the theoretical framework of 2D semiconductors ad vdW heterostructures established in the previous chapter, this chapter details the experimental protocols and technical methodologies employed throughout this research. The transition from fundamental material properties to functional optoelectronic devices requires a multi-stage approach characterized by high precision and reproducibility.

The experimental workflow described herein is organized into three primary pillars. First, the material preparation techniques are discussed, focusing on the production of high-quality 2D crystals via mechanical exfoliation and chemical vapor deposition (CVD), as well as their assembly into heterostructures via dry transfer methods. Second, the nanofabrication procedures are detailed, covering the lithographic and metallization steps necessary to define device architectures. Finally, the characterization techniques, ranging from morphological investigations to specialized electrical and optoelectronic measurements under controlled environmental conditions, used to evaluate the performance of the realized devices are described.

This chapter serves not only as a record of the specific parameters used in this work but also as a foundational methodology for the experimental results presented in the subsequent chapters.

2.1 Device fabrication

The transition from a raw 2D crystal to a functional FET or optoelectronic device is a fundamental stage that dictates the ultimate performance and reliability of the device. Unlike conventional silicon-based electronics, where processes are highly standardized and automated, the fabrication of 2D materials-based devices remains a meticulous, often manual process where the quality of the interfaces play a key role. I conducted the fabrication processes detailed in the following subsections for the realization of bP/MoS_2 heterostructures (Chapter 3) at the University of Duisburg-Essen, in Germany, and for the realization of WS_2/$PdSe_2$ heterostructures (Chapter 4) at the Instituto de Ciencia de Materiales de Madrid, in Spain, where I spent a seven-month research stay.

A recurring challenge throughout this fabrication workflow is the achievement of high reproducibility. Because 2D materials are composed entirely of surface atoms, they are extremely susceptible to their immediate environment. The introduction of extrinsic impurities, such as polymer residues from transfer processes, atmospheric adsorbates, or interfacial bubbles, can significantly alter doping levels and carrier mobility. Achieving a clean interface is therefore the primary objective for the used protocols, which begin with the preparation of high-quality flakes. To achieve this, we employed both top-down techniques (mechanical exfoliation[103]) and bottom-up strategies (atmospheric pressure chemical vapor deposition[104], APCVD) to ensure a controlled supply of high-quality flakes. In the following subsections, the specific fabrication methodologies and process flows for each device architecture are detailed.

2.1.1 Fabrication of bP/MoS_2 heterostructures

The bP/MoS_2 heterostructures were fabricated at the University of Duisburg-Essen during a short-research stay, following a multi-stage protocol that combines bottom-up synthesis and top-down assembly. Within the scope of this same collaboration, individual bP and MoS_2-based FETs were realized as reference devices. These FETs were fabricated using the identical procedures described below, specifically bP flakes were mechanically exfoliated and MoS_2 flakes were obtained through

APCVD, to ensure a consistent baseline for evaluating the synergistic effects within the heterostructures.

The process commenced with the preparation of p-type silicon (Si) substrates capped with a 285 nm thermally grown silicon dioxide (SiO_2) layer. The specific SiO_2 thickness serves as a dual purpose: facilitating the optical identification of 2D flakes through interference effects and enabling efficient channel modulation via high gate voltages. To ensure an ultra-clean surface for growth and exfoliation, the substrates underwent a rigorous solvent cleaning protocol. The chips were immersed in an acetone bath for 15 minutes to remove organic contaminants, followed by a thorough rinse in isopropanol (IPA). Finally, the substrates were dried using a high-purity nitrogen (N_2) flux to prevent the formation of water marks or residues.

MoS_2 flakes were synthesized using APCVD in a two-zone split-tube furnace, following an optimized variation of the procedure described by Pollman et al.[105,106] This bottom-up approach allows for the growth of high-quality crystalline domains. A small droplet of the molybdenum precursor, ammonium heptamolybdate (AHM), was placed near the edge of the cleaned substrates. The chips were then pre-heated at 300°C for 24 minutes to stabilize the precursor. To facilitate a high nucleation density, a seeding promoter (CAS) was applied via spin-coating at 60 rps for 40 seconds, creating the necessary sites for MoS_2 growth. The substrates were placed in the second zone of the quartz tube, while 100 mg of sulphur powder was placed in a crucible in the upstream zone. Before heating, the tube was purged with an Argon (Ar) flux for 15 minutes to create an inert environment. The growth was conducted by heating the sulphur zone to 170 °C and the AHM/substrate zone to 750 °C for 30 minutes. After the growth period, the furnace was opened, and the samples were allowed to cool naturally for 40-60 minutes. To maintain system purity, the crucibles were subsequently cleaned under oxygen flux at high temperatures to remove any residual sulphur ore precursor traces. Figures 2.1a-c show the growth of MoS_2 flakes on Si/SiO_2 substrates.

Following the successful growth of MoS_2 flakes, the heterostructure was completed using mechanical exfoliation and dry-transfer techniques. Few-layer bP flakes were mechanically exfoliated from bulk crystals onto separate, clean Si/SiO_2 substrates, as schematized in Figure 2.1d. Selected bP flakes were identified via optical microscopy and transferred onto the MoS_2 flakes using an aligned transfer platform (HQ Graphene). A polypropylene carbonate (PPC) film was employed as the carrier layer, enabling a dry-stacking[107] process that avoids the interfacial contamination associated with wet transfer methods (Figure 2.1e).

The final device architecture was defined through maskless UV lithography and metal evaporation. A micro-UV light maskless (Smartprint UV) was used to define the source and drain contact patterns. This maskless approach provides high flexibility for aligning contacts to irregularly shaped exfoliated flakes. To form the electrodes, Cr/Au (10/110 nm) bilayers were deposited. Chromium was utilized as an adhesion layer, while the gold layer provided high conductivity and chemical stability. The deposition was performed using a combination of thermal and electron-beam evaporation to ensure low contact resistance at high-fidelity patterns. The resulting devices, featuring a FET architecture, were then ready for the electrical and optoelectronic characterization described in Section 2.4. the successful integration of the heterostructure and the metal electrodes is evidenced in Figure 2.1f, which shows an optical image of a completed device architecture.

To mitigate the high environmental sensitivity of bP, the devices were encapsulated with an approximately 60 nm layer of poly(methyl methacrylate) (PMMA) immediately following the fabrication process. This protective coating acts as a passivation layer, inhibiting the rapid oxidation and degradation of the bP flakes upon exposure to ambient moisture and oxygen, which is critical for maintaining stable electronic characteristics.

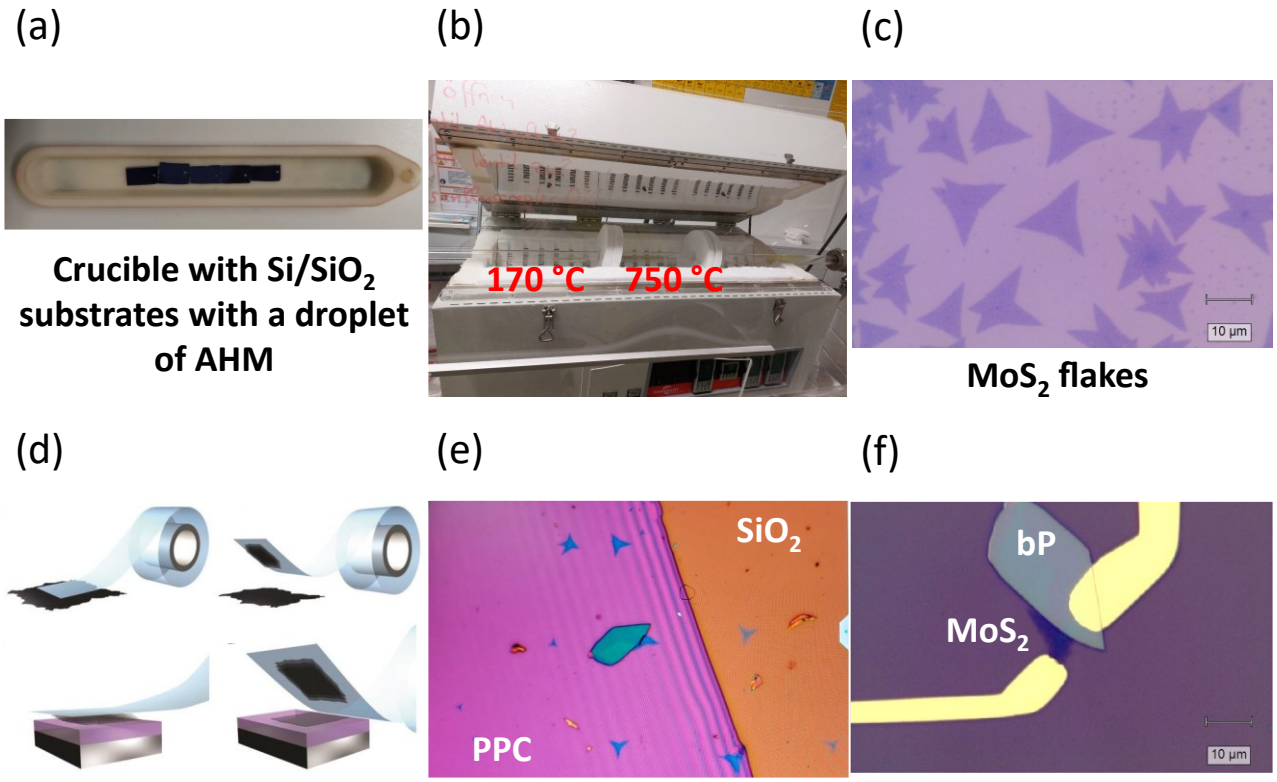


Figure 2.1: (a) Two-zone split tube furnace for APCVD of MoS_2. (b) Crucible with substrates with AHM droplets for the growth of MoS_2. (c) Optical image of a Si/SiO_2 substrate with grown MoS_2 flakes. (d) Mechanical exfoliation of bP with scotch tape on Si/SiO_2 substrates. (e) Transfer and alignment of bP flakes on substrates with MoS_2 flakes via a dry transfer method using PPC as carrier. (f) Optical image of a fabricated bP/MoS_2 heterostructure.

2.1.2 Fabrication of $WS_2/PdSe_2$ heterostructures

The $WS_2/PdSe_2$ heterostructures were fabricated at the Instituto de Ciencia de Materiales de Madrid (ICMM-CSIC) during a seven-month research stay. Within the scope of this project, individual WS_2 and $PdSe_2$-based FETs were also realized as reference devices, utilizing the same fabrication protocols as those employed for the heterojunctions to ensure experimental consistency. Unlike the top-contacts approach used for the bP/MoS_2 heterostructures, these devices were realized using a pre-patterned substrate architecture, which requires a high degree of spatial precision during the deterministic transfer of the 2D layers.

Before initiating the lithography process, $n^{++}Si/SiO_2$ substrates (290 nm oxide thickness) underwent a rigorous cleaning procedure identical to the one described in Section 2.1.1 to ensure a surface free of organic and particulate contaminants. Once cleaned, the substrates were prepared for electrode patterning. To achieve a high-quality lift-off and ensure sharp electrode edges, a bilayer resist

procedure was employed. A first layer of a lift-off resist (LOR) was spin-coated at 3000 rpm (40 s) and baked at 180 °C for 3 minutes. This was followed by a second spin coating of AZ1505 resist at 4000 rpm (40 s) and then baked at 100 °C for 1 minute. The pattern was defined using the SmartForce SmartPrint maskless system (Figure 2.2a). The internal architecture and operational mechanism of the maskless lithography system are illustrated in Figure 2.2b. The process follows a digital-to-optical conversion pathway. The electrode geometry was defined via a digital layout, which was subsequently translated into a spatially modulated UV light pattern and projected through a high-resolution objective onto the photoresist. Following the UV exposure, the substrates underwent a precisely controlled two-stage development process to define the contact architecture. The samples were first immersed in AZ 726 MIF developer for approximately 20 seconds to resolve the top imaging resist, followed by a through rinse in deionized (DI) water to stop the chemical reaction. To stabilize the resist profile and prepare the lower layer for controlled lateral etching, a post-bake was performed at 120 °C for 2 minutes. A second, 25-second immersion in the developer was then conducted to selectively etch the underlying LOR layer. This step is critical as it produces a controlled undercut (overhang) of approximately 300 nm.

This overhang profile is vital for the subsequent thermal evaporation of the metal electrodes; by creating a physical discontinuity between the metal deposited in the channel and the metal on top of the resist, the undercut prevents winging and ensures a clean break during the lift-off process. This results in electrodes with high edge-fidelity and minimal residue, which are essential for low-noise electrical injection in 2D heterostructures. The process concluded with a final DI water rinse and N_2 drying. With the bilayer resist pattern and undercut successfully defined, the substrates were moved to the metallization stage to form the source and drain electrodes.

The deposition of the metal contacts was performed using a thermal evaporation system under high vacuum conditions at a pressure on the order of 10^{-6} mbar (Figure 2.2c). A bilayer of Cr/Au (5/45 nm) was deposited sequentially. The chromium layer serves as an essential adhesion promoter between the SiO_2 surface and the gold, while the 45 nm Au layer provides a highly conductive and chemically inert contact for electrical injection (Figure 2.2d). The line-of-sight nature of thermal evaporation, combined with the previously engineered 300 nm undercut, ensures that the metal film remains discontinuous at the resist sidewalls, facilitating a clean lift-off. To reveal the final electrode geometry, an efficient lift-off process was employed. Because the LOR layer is chemically engineered to be resistant to many common solvents, the samples were immersed in a bath of Dimethyl Sulfoxide (DMSO). The DMSO effectively strips the LOR/resist stack, allowing the sacrificial metal layer to float away without the need for mechanical agitation that could damage the delicate features. Following the lift-off, the substrates underwent a final sequential solvent cleaning to ensure a surface free of residues. An acetone rinse was used to remove any remaining traces of imaging resist and DMOS (Figure 2.2e). An IPA rinse was performed to remove the acetone and prevent the formation of organic residues. The substrates were then dried with a high purity N_2 flux. A representative optical image of the electrodes fabricated via this protocol is presented in Figure 2.2f. After the preparation of the prepatterned electrodes, the 2D materials were integrated.

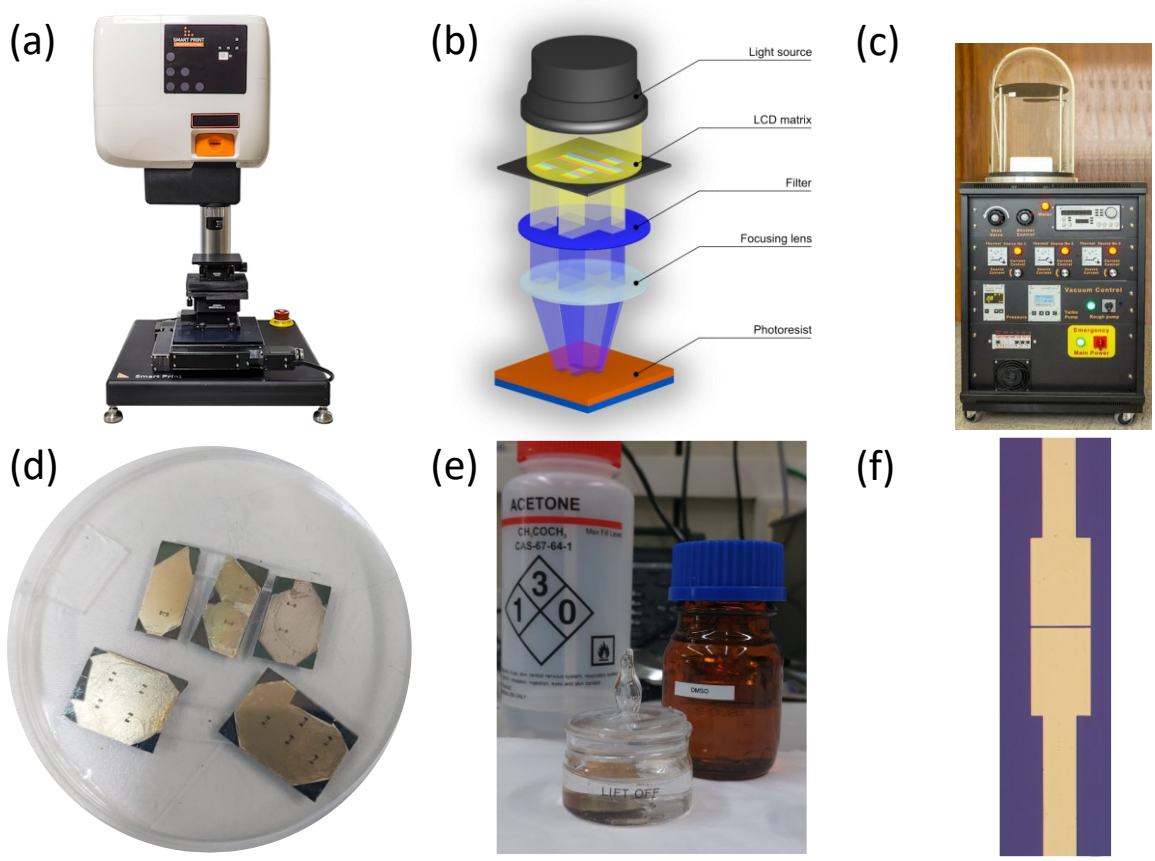


Figure 2.2: Overview of the fabrication of the prepatterned electrodes. (a) Smartprint maskless lithography system (Smart Force Technologies). (b) Schematic representation of the operational principle of the maskless UV projection system. (c) Thermal evaporation system (Tecuum ag) utilized for the deposition of Cr/Au bilayers. (d) Si/SiO_2 substrates after the Cr/Au metallization process. (e) Illustration of the solvent-based lift-off procedure. (f) Optical image of the finalized electrodes.

WS_2 and $PdSe_2$ flakes were mechanically exfoliated onto polydimethylsiloxane (PDMS) stamps and inspected via transmission-mode optical microscopy. This allowed for the identification of high-quality, homogeneous flakes based on their optical contrast[108] (Figure 2.3a-b). Using a home-built deterministic transfer station[109], the WS_2 flake was first aligned and lowered onto the electrodes, with a portion of the flake in contact with the gold (Figure 2.3c).[107] Subsequently, the $PdSe_2$ flake was transferred over the WS_2, creating the vertical heterojunction (Figure 2.3d). The all-dry nature of this PDMS-based transfer ensures that no significant residues are trapped between the two semiconductive layers, preserving the integrity of the vdW interface.

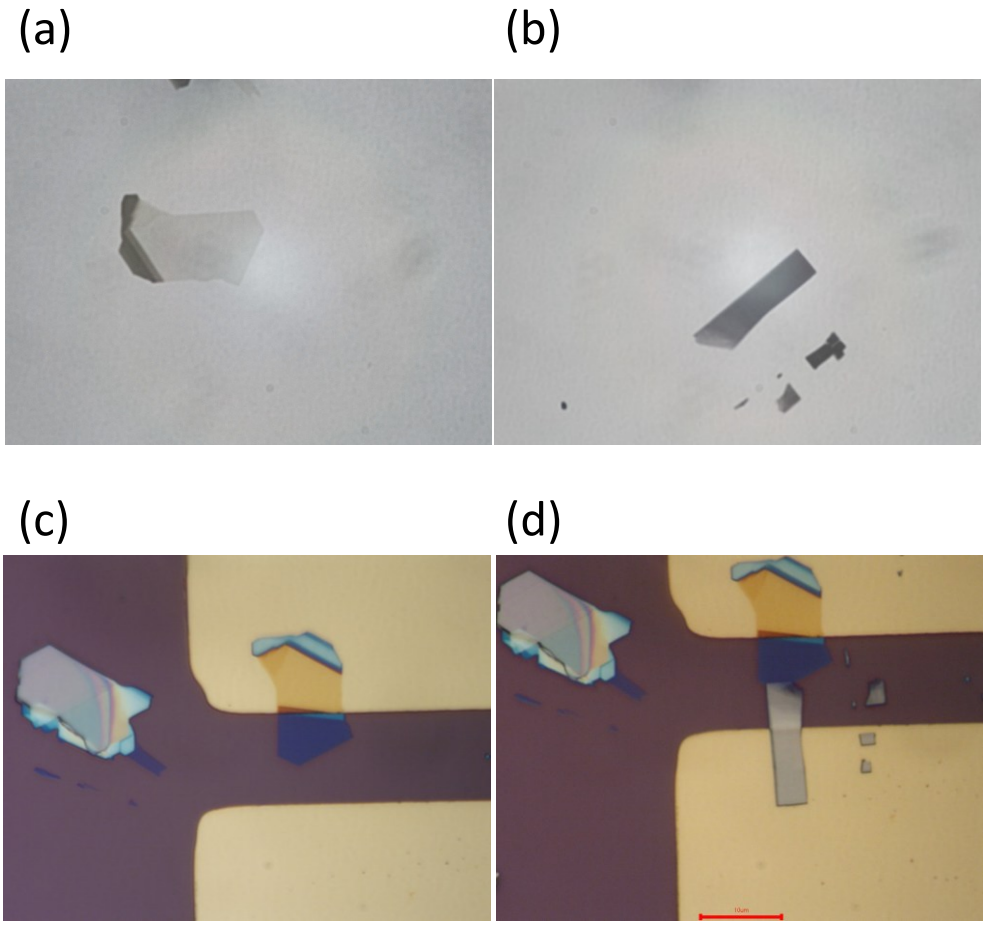


Figure 2.3: Overview of the transfer of 2D flakes for obtaining a $WS_2/PdSe_2$ heterostructure. Optical image of a (a) WS_2 and a (b) $PdSe_2$ flake onto a PDMS stamp. The optical contrast with the underneath 290 nm-SiO_2 gives information about the thickness and homogeneity of the materials. Optical image of the device (c) after the transfer of the first flake (WS_2) and (d) after the transfer of the second flake ($PdSe_2$).

2.1.3 Fabrication of $MoSe_2$ devices

The $MoSe_2$ complementary FET (cFET) was fabricated at the Liaoning Academy of Materials in Shenyang, China. The primary objective of this architecture was to realize a single-channel device with spatially defined p-type and n-type regions and a floating-gate structure. This was achieved by utilizing chromium oxide chloride (CrOCl) to induce p-type behaviour in specific regions of the $MoSe_2$ flake.

To enable independent electrostatic control of the channel, a local gate was first fabricated on a clean Si/SiO_2 substrate (300 nm oxide) by electron-beam lithography (EBL) and thermal evaporation of a Cr/Au bilayer (5/30 nm) (Figure 2.4a). First, hBN flakes were obtained by mechanical exfoliation and transferred onto the Au local gate using a dry-transfer method, with polypropylene carbonate (PPC) stamps serving as carriers (Figure 2.4b). PPC residues were removed by cleaning the substrates with acetone. Subsequently, CrOCl flakes were mechanically exfoliated and transferred onto the hBN layer using polydimethylsiloxane (PDMS) stamps, partially covering the underlaying hBN flake (Figure 2.4c). Finally, $MoSe_2$ flakes were mechanically exfoliated and transferred on top of the vertical structure, such that one portion of the flake rested on the hBN/CrOCl stack, while the other part was

in direct contact with the hBN layer (Figure 2.4d). Multiple metal electrodes were patterned via EBL and Ti/Au (5/50 nm) bilayers were deposited via e-beam evaporation (Figure 2.4e). After the final lift-off processes, the completed device was annealed at 320 °C to improve the contacts.

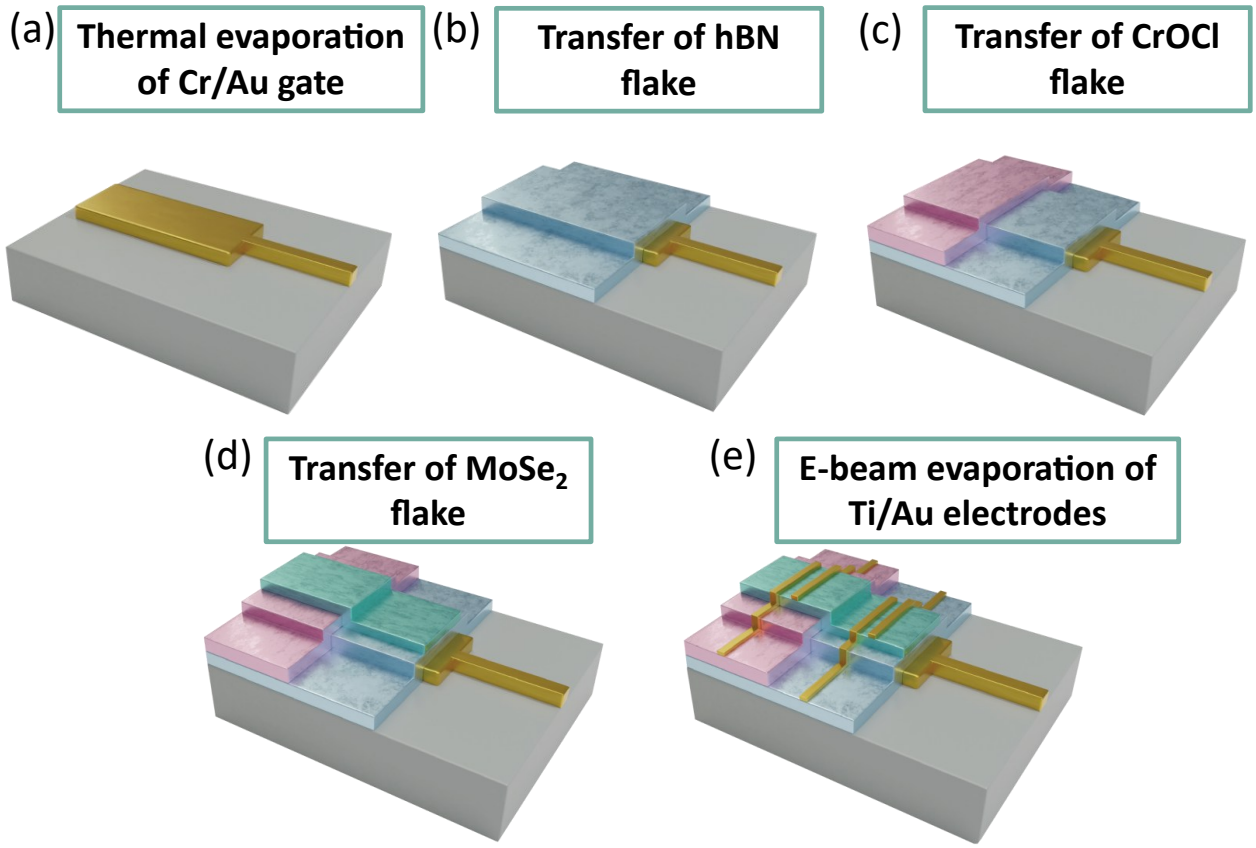


Figure 2.4: Schematic representation of the fabrication process of a $MoSe_2$ cFET. (a) Thermal evaporation of Cr/Au for obtaining a local gate. (b) Transfer of a hBN flake. (c) Transfer of a CrOCl flake, overlapping a portion of the hBN flake. (d) Transfer of a $MoSe_2$ flake, partially overlapping the CrOCl layer. (e) E-beam evaporation of multiple Ti/Au electrodes.

2.2 Morphological and structural characterization

Following the isolation or growth of 2D flakes and their assembly into heterostructures, a rigorous characterization protocol is essential before proceeding to electrical measurements. Since the electronic properties of 2D semiconductors, such as carrier mobility, bandgap, and screening effects, are generally dependent on the number of layers and the crystalline quality, morphological and structural validation represent an indispensable prerequisite within the experimental workflow, ensuring that the material properties are fully defined before proceeding to device integration.

Morphological characterization allows for the determination of flake thickness and surface cleanliness, while structural and optical spectroscopy provide a fingerprint of the material's integrity. In this work, we employed Atomic Force Microscopy (AFM), Raman spectroscopy, and photoluminescence (PL) microscopy. These non-destructive techniques allow us to correlate the physical state of the material with the electrical performance observed in the final device.

2.2.1 Atomic Force Microscopy

AFM is the primary technique employed for the topographical characterization of the 2D flakes and heterostructures. In this work, measurements were carried out using a NaioAFM by Nanosurf AG system. The AFM offers sub-nanometer vertical resolution, which is critical for determining the layer thickness of exfoliated and CVD-grown materials and for evaluating the cleanliness of the vdW interfaces.

The fundamental operation of the AFM relies on a probe consisting of a flexible cantilever/tip assembly. This assembly consists of a very sharp tip (typical radius of curvature at the end for commercial tips is 5-10 nm) that hangs off the bottom of a long and narrow cantilever (Figure 2.5a). AFM cantilever material typically consists of silicon or silicon nitride. While silicon probes are standard for high-resolution imaging in air, silicon nitride is often preferred for applications requiring softer cantilevers with lower spring constants, such as force spectroscopy or imaging in liquid environments. As the probe interacts with the sample surface through a raster scanning motion, the forces between the tip and the atoms on the surface cause the cantilever to deflect. This mechanical displacement is monitored using an optical lever system: a laser beam is reflected off the back of the cantilever onto a position-sensitive photodetector (PSPD). The PSPD tracks both the vertical and lateral motion of the probe, transducing the deflection into a voltage signal (Figure 2.5b). To obtain quantitative topographical data, the deflection sensitivity of the detector is calibrated, establishing the precise correlation between the measured voltage and the physical displacement in nanometres. The force of interaction between the tip and the sample surface is governed by the stiffness of the cantilever, i.e. its spring constant, $\mathrm{k} = \frac{\mathrm{Ewt}^3}{4\mathrm{L}^3}$, where w, t and L are the cantilever width, thickness, and length, respectively, and E is the Young's modulus of the cantilever material.

The constant interaction between the tip and the sample is achieved through a feedback loop, a control system analogous to a thermostat. Just as a thermostat adjusts a heater to maintain a temperature setpoint, the AFM adjusts the Z-piezo to maintain a specific physical parameter at a constant setpoint. In this work, the AFM was operated in contact mode, which is also known as static mode. In this regime, the feedback parameter is the physical deflection of the cantilever. In this case, the tip remains in continuous contacts with the surface. As the probe encounters topographical features, the cantilever deflects; the feedback loop then moves the Z-piezo up or down to restore the deflection to its original setpoint. The vertical movement of the Z-piezo required to maintain this constant deflection is recorded as the height information.

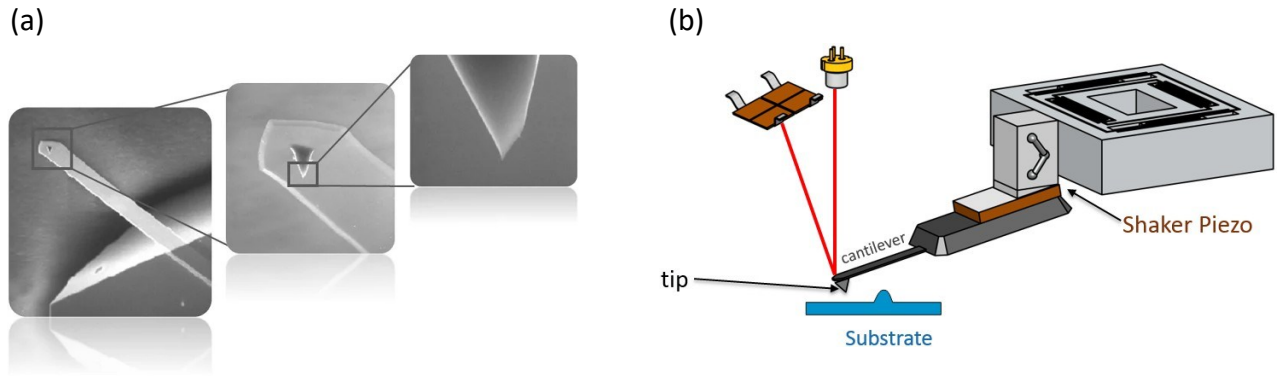


Figure 2.5: (a) Scansion electron microscope (SEM) image of typical AFM cantilevers. (b) Schematic of the principle of how AFM works.

2.2.2 Raman spectroscopy

Raman spectroscopy is employed to probe the structural and vibrational properties of the 2D flakes. This technique is particularly powerful for vdW materials, as the vibrational modes (phonons) are highly sensitive to the number of layers, the presence of strain, and the degree of electronic doping. The Raman effect is based on the inelastic scattering of monochromatic light, typically from a laser source. When the incident photons interact with the phonon modes of the crystal lattice, the vast majority undergo Rayleigh scattering, where the scattered photons have the same energy as the incident ones. However, a small fraction (approximately 1 in 10^7 photons) undergoes an energy shift due to the exchange of energy with the lattice vibrations. This shift in energy, known as the Raman shift, is measured in wavenumbers (cm^{-1}) and is defined by $\Delta w = \frac{1}{\lambda_{incident}} - \frac{1}{\lambda_{scattered}}$, where $\lambda_{incident}$ and $\lambda_{scattered}$ are the incident and scattered wavelengths. The process is categorized as Stokes scattering when the photon excites a phonon and loses energy, resulting in a lower frequency (red shift); this is the most measured signal at room temperature. When the photon absorbs energy from a pre-existing phonon, resulting in a higher frequency (blue shift), the process is categorized as anti-Stokes scattering. In this thesis, Raman measurements were performed with a Renishaw InVia Raman microscope (Chapter 3) and with a MonoVista CRS+ system (Spectroscopy and Imaging GmbH) (Chapter 4). These systems allow for a high spatial resolution (sub-micron), suitable for studying small exfoliated or CVD-grown flakes. These systems consist of a laser source, a confocal microscope, and a spectrometer and detector. It is typically selected a green (532 nm) or red (633 nm) laser source. The choice of wavelength is critical to avoid strong fluorescence and to potentially exploit resonance effects in TMDs. A high-numerical-aperture objective, i.e. 100x, is used to both focus the laser onto the sample and collect the back-scattered light. The collected light is passed through a notch filter to block the intense Rayleigh signal and into a grating spectrometer, which disperses the light onto a charge-coupled device (CCD) detector.

In the context of 2D TMDs, the two most prominent Raman-active modes are the in-plane modes (E^1_{2g}), associated with the opposite vibration of the metal and chalcogen atoms within the layer plane, and the out-of-plane modes (A_{1g}), associated with the vibration of chalcogen atoms out of the layer plane.

2.2.3 Photoluminescence spectroscopy

PL spectroscopy is a fundamental optical technique used to investigate the electronic band structure and radiative recombination mechanisms of 2D semiconductors. While Raman spectroscopy probes the vibrational lattice, PL provides a direct window into the electronic transitions and the nature of the energy bandgap. The PL process begins when a material absorbs a photon with energy greater than its bandgap. This absorption promotes an electron from the valence band to the conduction band, leaving behind a hole. Due to the reduced dielectric screening and strong quantum confinement in 2D materials, the electron and hole remain bound together by Coulombic attraction, forming a quasiparticle known as exciton. The subsequent radiative recombination of these excitons results in the emission of a photon. The energy of this emitted light typically corresponds to the optical bandgap of the material (minus the exciton binding energy). In TMDs, the PL spectra are often dominated by the so-called A and B excitons, which arise from the spin-orbit splitting of the valence band.[110] Most TMDs possess an indirect bandgap, meaning that the valence band maximum and conduction band minimum occur at different points in the Brillouin zone. Consequently, radiative recombination requires the assistance of a photon to conserve momentum, leading to very weak PL intensity. However, as the material is thinned to a monolayer, the bandgap transitions from indirect to direct at the K-points of the Brillouin zone. This transition leads to a massive enhancement in PL quantum yield. For this reason, PL spectroscopy serves as a golden tool for monolayer identification and material quality assessment. The experimental setup for PL is integrated into the same Raman system described previously, utilizing a confocal microscope to achieve sub-micron spatial resolution.

2.3 Electrical characterization

The final stage of the experimental workflow is the evaluation of the electronic transport and optoelectronic properties of the fabricated devices. These measurements are fundamental for determining key parameters such as field-effect mobility, threshold voltage, and photo-responsivity and for testing several electronic and optoelectronic applications exploiting specific materials' properties.

Electrical measurements were conducted using a probe station (Janis probe station for measurements in Chapter 3, Lakeshore probe station for all the other electrical measurements), depicted in Figure 2.6a, connected to a semiconductor characterization system (SCS) Keithley 4200 (Figure 2.6b). This instrument is a modular, fully integrated parameter analyzer capable of sourcing and measuring current and voltage simultaneously with a current and voltage sensitivity of 0.1 pA and 2 μV, respectively. Beyond standard transfer and output characterization, the system was configured to demonstrate advanced electronic functionalities.

To investigate the light-matter interaction and the photo-responsive properties of the 2D heterostructures, the electrical characterization setup was integrated with a high-performance optical excitation suite. This configuration allows for the simultaneous application of electrical bias and optical stimuli, enabling the measurement of the figures of merit of photodetectors. The light is delivered to the measurement chamber via a high-stability optical fiber coupled directly to the probe station (Figure 2.6c). The fiber output can be precisely aligned and focused onto the active channel of the 2D device via external manipulators. This spatial precision is critical given the micrometre-scale dimensions of the 2D flakes. The primary light source utilized in this work is a SuperK Compact

(NKT Photonics), a broadband supercontinuum white laser (Figure 2.6d). Unlike standard single-wavelength lasers, the SuperK Compact provides a high-brightness output across a vast spectral range, from 450 to 2400 nm. To achieve precise wavelength selection, the laser output is coupled into a Sciencetech 0.25 m Fast monochromator (Figure 2.6e). This instrument features a motorized triple-grating turret, allowing for high-resolution spectral tuning from the ultraviolet to the near-infrared. By sweeping the wavelength via software control, the spectral responsivity of the devices can be characterized to determine their peak sensitivity and bandgap-related transitions. The excitation parameters, including optical power and pulse duration, are managed through specialized control software. To investigate the temporal response and switching speeds of the photodetectors, the system can be coupled with an oscilloscope. Indeed, by modulating the laser to produce square-wave optical signals, the rise and fall times of the photocurrent can be observed. Furthermore, the oscilloscope captures the high-speed transient behaviour of the device, which is fundamental for understanding the recombination kinetics of electron-hole pairs and other more complex mechanisms that can occur.

A critical consideration in the study of 2D materials is their extreme sensitivity to environmental conditions. Due to their atomic thickness and high surface-to-volume ratio, 2D materials are highly susceptible to atmospheric adsorbates, which can act as unintentional dopants or scattering centres. To ensure that the experimental results accurately capture the intrinsic physics of the 2D flakes, all fundamental studies were performed under vacuum conditions. The environmental control was achieved using a vacuum system comprising a rotary pump for initial draw-down and a turbomolecular pump for high vacuum levels, reaching pressure of 10^{-5} mbar. This vacuum system was used for demonstrating pressure sensing (Chapter 4).

To gain a deeper understanding of the charge transport mechanisms and the nature of the electronic states in the fabricated devices, we performed extensive temperature-dependent electrical measurements. These studies are essential for distinguishing between different conduction regimes, such as thermionic emission and phonon-limited scattering. The probe station was equipped with a specialized thermal stage that allows for precise control over the sample environment. To facilitate high-temperature characterization, the experimental setup integrates a dedicated thermal control system. For measurements above room temperature, up to 400 K, heating is provided by a resistive element managed by a Scientific Instruments Model 9700 temperature controller. The primary features and operational principles of the heating system include a heater output and resistive load, thermal resistors as sensor feedback, a PID control algorithm, and a safety and power management. The controller provides a fail-safe, current-controlled heater output of up to 50 W. This power is delivered to a resistive heating element, typically with a resistance between 25 and 50 Ω, which is integrated into the sample stage. Precise temperature monitoring is achieved through dedicated sensor inputs that support various sensing elements, including thermal resistors and diodes. The controller provides constant current excitation, ranging from 10 µA to 1 mA, to these sensors to measure resistance or voltage changes accurately. To reach and maintain the target set point with high stability, the instrument utilizes an industry-standard PID (Proportional-Integral-Derivative) control algorithm. This closed loop system continuously adjusts the heater power based on the error between the measured temperature and the desired set point. To prevent damage to delicate 2D heterostructures or the heater itself, the system allows for a software-defined limit on the maximum heater power. Additionally, a hardware-controlled bar graph on the front panel provides a real-time

visual indication of the power being applied to the sample stage. On the other hand, to investigate the electronic transport properties in the cryogenic regime, the system is configured for low-temperature measurements utilizing liquid nitrogen. This cooling stage is essential for suppressing thermally activated carrier hopping and phonon scattering, thereby allowing for the observation of intrinsic phenomena such as quantum confinement or localized state transport in the 2D materials and heterostructures.

The cooling process is facilitated by a pressure-driven cryogen transfer system. In this configuration, a high-capacity cryogenic dewar containing liquid nitrogen is used as the primary reservoir. To initiate the flow, the headspace of the dewar is pressurized by introducing gaseous nitrogen. This controlled increase in internal pressure creates a differential that drives the liquid phase through a vacuum-insulated transfer line directly into the heat exchanger, also known as cold finger, located within the measurement chamber. By modulating the gaseous nitrogen pressure and the exhaust flow rate, the rate of liquid nitrogen delivery can be precisely tuned to achieve a stable thermal equilibrium at a base temperature of approximately 77 K. This flow-through mechanism ensures that the sample stage is continuously cooled while the device remains under high vacuum conditions, preventing the condensation of atmospheric moisture on the 2D interface. Furthermore, the coupling between this system and the temperature controller allows for the temperature stabilization at different intermediate stage between 77 and 400 K. This setup provides a stable environment for conducting temperature-dependent transfer and output characteristics, which are fundamental for extracting the activation energies of the charge carriers. Additionally, the rigorous monitoring of device performance through integrated temperature and pressure sensors is essential to validate the operational stability and reliability of these 2D heterostructures in extreme regimes. Demonstrating robust functionality under such diverse conditions is a critical prerequisite for the deployment of 2D material-based electronics in demanding fields such as aerospace engineering, satellite communications, and high-performance industrial sensing, where components must endure significant thermal fluctuations and varying atmospheric pressures without compromising performance.

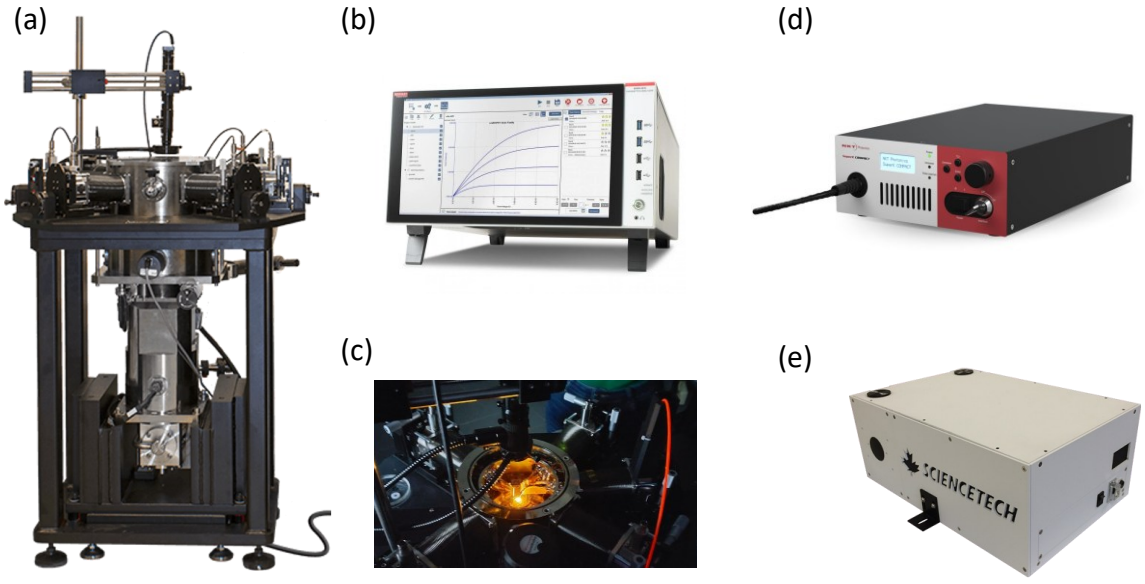


Figure 2.6: (a) Probe station, Lakeshore. (b) Semiconductor characterization system, Keithley 4200. (c) Supercontinuum white light laser, SuperK Compact, NKT Photonics. (d) Monochromator, Sciencetech.

3. BLACK PHOSPHORUS/MOLYBDENUM DISULPHIDE HETEROSTRUCTURES

This chapter is dedicated to the study of bP and its integration into vertical vdW heterostructures with MoS_2. The fabrication and stacking processes, detailed in Section 2.1.1, enable the development of a material platform that synergistically combines the high charge carrier mobility and narrow bandgap of bP with the robust n-type characteristics and visible-range bandgap of MoS_2. To establish a rigorous baseline, the chapter first evaluates the performance of individual bP-based FETs. We utilize the Y-function method to decouple intrinsic channel properties from contact resistance, an essential step for accurately assessing the carrier mobility. Furthermore, we explore the potential of bP in specialized architectures, including non-volatile memory devices and photodetectors.

The second part of the chapter focuses on the bP/MoS_2 vertical heterostructure. Pairing the p-type nature of bP with the n-type MoS_2 results in a type-II staggered band alignment. This configuration is highly advantageous for optoelectronic applications, as the built-in electric field at the interface facilitates the efficient separation of photogenerated electron-hole pairs. Gate-tunable p-n diodes based on bP/MoS_2 vertical heterostructures have demonstrated significant rectification.[111–115] BP/MoS_2 heterojunctions have been exploited for the realization of tunnel field effect transistors (FETs).[116,117] Furthermore, bP/MoS_2 heterojunctions have shown promising properties for photodetection. Photoresponsivities from few mA/W to A/W have been achieved with few-layer bP/MoS_2 heterojunctions.[112,113,115]

We provide a detailed electrical characterization of these heterojunctions, analyzing their behaviour under varying temperature and illumination conditions. Finally, we demonstrate the device's capability in self-powered (photovoltaic) mode, highlighting the potential of the bP/MoS_2 system for next-generation energy-efficient sensors and photovoltaic cells.

3.1 Black phosphorus

To investigate the intrinsic transport properties of bP, multilayer bP flakes were mechanically exfoliated from high-purity bulk crystals (Smart Elements) on $p^{++}Si$/ SiO_2 substrates (90 nm oxide), following the fabrication procedure detailed in Section 2.1.1.

Given that the performance of bP FETs is critically dependent on the metal-semiconductor interface, two distinct batches of devices were fabricated to optimize the electrical injection. The first batch utilized Ni/Au contacts, while the second batch employed a NiCr (50:50 alloy)/Au metallization. This comparison was intended to evaluate whether the addition of Cr could improve adhesion or modulate the Schottky barrier height at the contact region. Immediately prior to transferring the samples into the vacuum chamber for electrical characterization, the 60 nm thick PMMA layer was removed using a sequential rinse in acetone and ethanol. This cleaning protocol ensured that the bP surface remained pristine, minimizing the formation of phosphoric acid species that would otherwise degrade the device mobility and increase the contact resistance.

Figure 3.1a shows an optical image of a device from the Ni/Au contacts batch after the removal of PMMA. The AFM analysis was conducted after the electrical measurements to avoid the exposure to ambient conditions that could have damaged the performance of the device. Figure 3.1b reports the AFM image of the same device. The thickness of this flake is around 20 nm, as shown in Figure 3.1c. A schematic of fabricated devices with the electrical setup used for the two-probe

configuration electrical measurements is reported in Figure 3.1d. The highly doped Si substrate, covered by conductive silver paste, served as the gate electrode of the transistor, while Ni/Au metal contacts were used as the source and drain electrodes. The channel current was monitored while applying voltage biases between source and drain and between the gate and source. Before performing the electrical characterization of the devices, the gate current, I_g, through the oxide layer was measured to verify the integrity of the dielectric. All the electrical measurements were performed in vacuum to avoid the interaction of the bP surface with ambient O_2 and moisture.

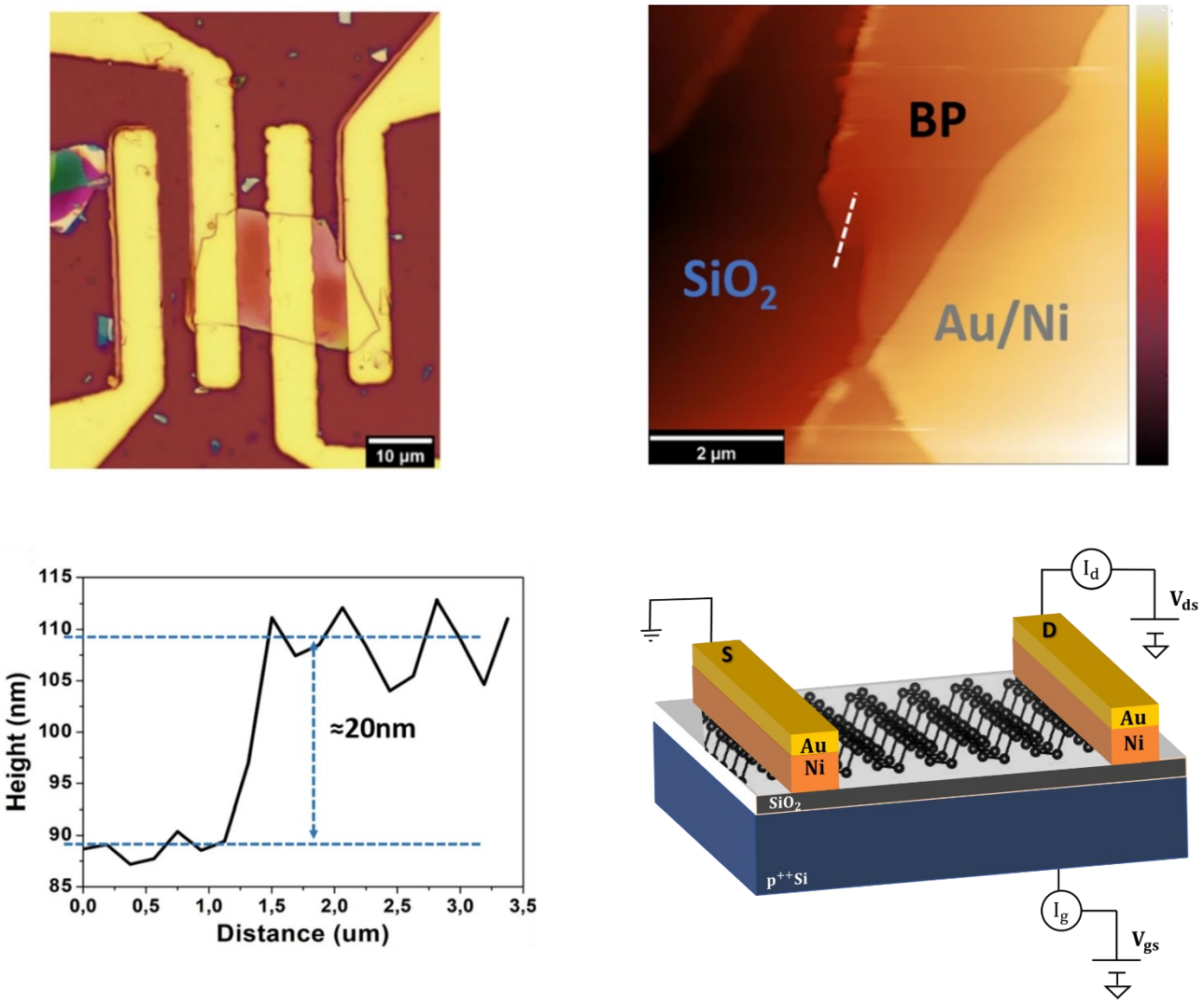


Figure 3.1: (a) Optical image of a Bp FET with Ni contacts. (b) AFM image of such bP device. (c) Height profile of the bP flake. (d) Schematic representation of the bP device.

3.1.1 Extraction of contact resistance with Y-function method

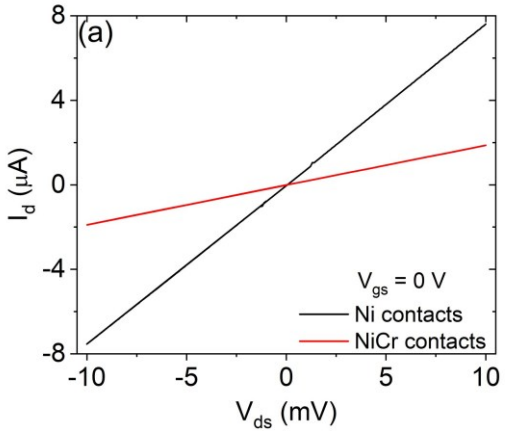
An important challenge common to many 2D materials is the selection of suitable contact metals and the optimization of the contact resistance between the semiconductor and the electrodes. To achieve good ohmic behaviour, several studies have investigated the alignment of the Fermi level of bP with different metals. Telesio et al.[118] examined the role of nickel, titanium, and chromium as contact metals in bP-based FETs, finding that chromium yields more resistive contacts than nickel. Before performing the complete study on devices employing nickel as an adhesion layer, a

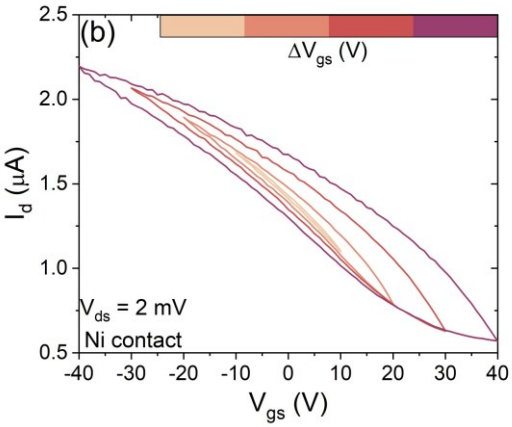
preliminary comparison was carried out between devices with Ni/Au and NiCr/Au contacts. The NiCr alloy (50:50 composition) was deposited by e-beam evaporation, analogously to the pure Ni layer.[8]

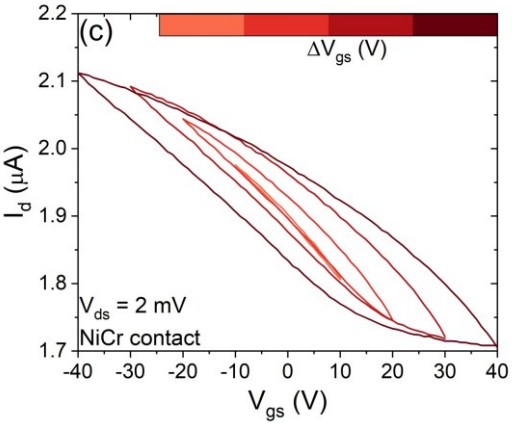
The electrical characterization was conducted in vacuum at a pressure of 2 mbar to prevent degradation of the channel material. Figure 3.2a shows the current-voltage (I-V) characteristics at V_{gs} = 0 V of the transistors with Ni and NiCr contacts. The linear behaviour of the I-V characteristics indicates ohmic contacts in both cases. The two-terminal resistance is $R_{tot} \approx 1.3$ kΩ for Ni contacts and $R_{tot} \approx 5.2$ kΩ for NiCr contacts. R_{tot} includes the contributions from the channel and the contacts, $R_{tot} = 2\,R_c + R_{ch}$, where R_c is the contact resistance between the metal and bP and R_{ch} is the bP channel resistance. Since the channel resistance is comparable for both devices, the higher R_{tot} in the NiCr-contacted transistors indicates that NiCr contacts are more resistive than Ni contacts. Further investigation was performed to separate the two contributions. Figure 3.2b-c show the transfer characteristics of the devices with Ni and NiCr contacts, respectively, under a drain bias of 2 mV, for increasing gate voltage sweep ranges (ΔV_{gs}) from ±10 V to ±40 V. The transfer curves exhibit p-type conduction, with higher drain currents at negative gate biases. At fixed V_{gs} and V_{ds}, the current in devices with Ni contacts is approximately one order of magnitude higher in those with Ni contacts, confirming the superior performance of Ni-contacted FETs. Moreover, the Ni-contacted devices exhibit better switching behaviour, with on/off current ratios up to 4, compared to 1.2 for NiCr-contacted devices.

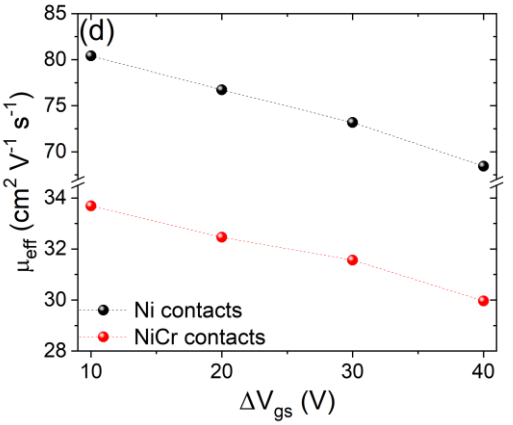
The charge carrier mobility, shown as a function of the gate voltage range in Figure 3.2d, displays a slight dependence on ΔV_{gs}, commonly reported for 2D materials and organic semiconductor-based devices.[119–121] The transistor with Ni contacts exhibits a mobility of 80 $cm^2\,V^{-1}\,s^{-1}$, compared to 34 $cm^2\,V^{-1}\,s^{-1}$ for the NiCr-contacted device. For similar devices with bP flakes thicker than 20 layers, reported mobilities are typically below 100 $cm^2\,V^{-1}\,s^{-1}$.[122] In this case, the relatively low mobility is mainly attributed to interfacial and intrinsic defects, as well as the number of layers. Impurities located at the bP/SiO_2 interface and intrinsic defects can act as scattering or trapping centres, reducing carrier mobility. The field-effect mobility extracted from the transfer curves may be underestimated since it includes the effect of the contact resistance R_c. Thus, the Y-function method, detailed Section 1.2.4, was used to extract R_c and to estimate the intrinsic mobility μ_0, unaffected by R_c.

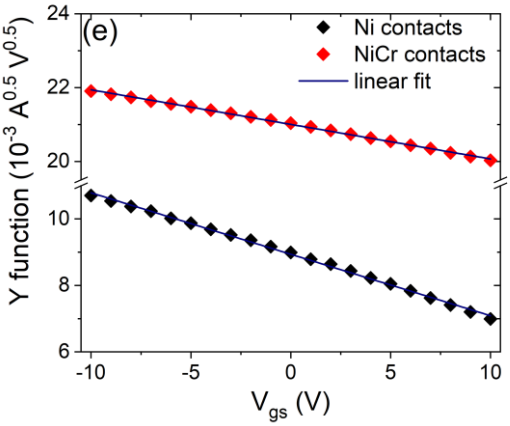
The Y-function was obtained from all the measured transfer curves with different ΔV_{gs}. Figure 3.2e shows the Y-function corresponding to the transfer curves with ΔV_{gs} = 10 V for both Ni- and NiCr-contacted devices. The extracted μ_0 as a function of gate voltage sweep is reported in Figure 3.2f, showing a maximum mobility of 112 $cm^2\,V^{-1}\,s^{-1}$ for bP with Ni contacts and 40 $cm^2\,V^{-1}\,s^{-1}$ for bP devices with NiCr contacts. Eliminating the contact resistance results in an over 30% increase in the estimated mobility, in agreement with results reported on MoS_2 – based FETs.[123] From the linear fit of $1/\sqrt{g_m}$ vs V_{gs} (Figure 3.2g), the contact resistance was extracted. As shown in Figure 3.2h, Ni contacts exhibit a contact resistance approximately three times lower than their NiCr counterpart, with specific contact resistance of 6.3 kΩ µm and 18.1 kΩ µm, respectively. The value obtained at V_{gs} = 10 V is lower than the 5.5 kΩ µm reported by Du et al. for bP devices with Ni contacts, extracted using the transfer length method.[124]

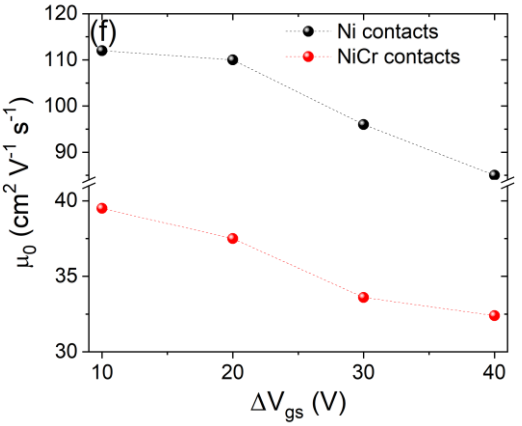

(a)
I_d (μA)
V_{ds} (mV)
V_{gs} = 0 V
Ni contacts
NiCr contacts

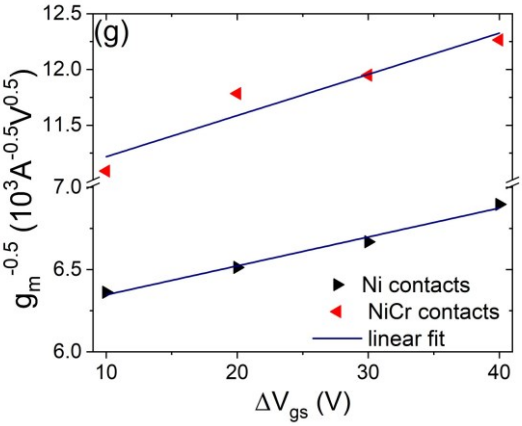

(b)
ΔV$_{gs}$ (V)
I_d (μA)
V_{ds} = 2 mV
Ni contact
V_{gs} (V)


(c)
ΔV$_{gs}$ (V)
I_d (μA)
V_{ds} = 2 mV
NiCr contact
V_{gs} (V)


(d)
μ_{eff} (cm^2 V^{-1} s^{-1})
Ni contacts
NiCr contacts
ΔV$_{gs}$ (V)


(e)
Ni contacts
NiCr contacts
linear fit
Y function (10^{-3} A$^{0.5}$ V$^{0.5}$)
V_{gs} (V)


(f)
Ni contacts
NiCr contacts
μ_0 (cm^2 V^{-1} s^{-1})
ΔV$_{gs}$ (V)


(g)
Ni contacts
NiCr contacts
linear fit
$g_m^{-0.5}$ (10^{3}A$^{-0.5}$V$^{0.5}$)
ΔV$_{gs}$ (V)

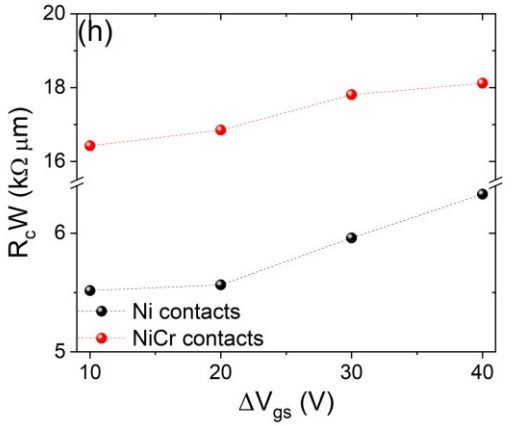

(h)
R_cW (kΩ μm)
Ni contacts
NiCr contacts
ΔV$_{gs}$ (V)

Figure 3.2: (a) I-V characteristics in vacuum at room temperature with V_{gs} = 0 V of the bP devices with Ni contacts (black line) and NiCr contacts (red line). Transfer curves in vacuum at room temperature with V_{ds} = 2 mV and different V_{gs} sweeps of the bP devices with (b) Ni and (c) NiCr contacts. (d) Field-effect mobility of the bP devices as a function of ΔV_{gs}. (e) Y-function and (f) mobility without contact resistance effects of the bP devices with Ni and NiCr contacts. (g) $1/\sqrt{g_m}$ versus ΔV_{gs} plots and (h) specific contact resistance as a function of ΔV_{gs} for Ni and NiCr contacts.

3.1.2 Temperature dependent electrical properties

Temperature-dependent electrical characterization provides valuable insight into the transport mechanisms, contact behaviour, and activation processes of 2D material devices. By monitoring the current evolution over the temperature range of 150-340 K, it becomes possible to distinguish between different scattering regimes, identify the dominant charge injection processes (thermionic emission or tunnelling), and assess the influence of trap and impurity states.

The study was conducted on bP devices with Ni contacts. Figure 3.3a shows the output curves measured at room temperature in vacuum at a pressure of 2 mbar, with V_{gs} varying from -50 to 50 V in steps of 10 V. The higher current at positive V_{gs} values indicates a p-type conduction. Figure 3.3b displays the corresponding transfer curves with ΔV_{gs} up to ±50 V, revealing a clear hysteretic behaviour.

The hysteresis width of transfer characteristics is defined as the horizontal separation between the forward and backward sweep branches. This effect originates from the presence of charge traps, where charge carriers become trapped or detrapped during the gate voltage sweep. During the forward sweep, traps gradually fill with charge carriers; in the backward sweep, they are released with a finite relaxation time. As a result, some charges remain trapped, leading to the observed hysteresis. Similar hysteretic behaviour in low dimensional materials-based FETs has been previously attributed to several mechanisms, including adsorption of water molecules, oxide traps near the semiconductor conduction band, interface traps at the oxide/semiconductor interface, intrinsic structural defects, and gate bias stress effects. In terms of energy levels, these traps correspond to localized states within the semiconductor bandgap that interact with charge carriers, thus alterating the device's ideal transfer characteristic.[119]

In this work, the hysteresis width (H_w) of the transfer characteristics is defined as the V_{gs} difference corresponding to the average current between the on and off states of the device, $I_m = (I_{on}+I_{off})/2$. Since the measurements were conducted in vacuum, adsorbates, which usually contribute significantly to the hysteretic behaviour of transfer curves, do not play a major role in this case. The observed hysteresis width is mainly attributed to charge trapping at the SiO_2/bP interface. The increase in H_w with larger ΔV_{gs}, as shown in the inset of Figure 3.3b, further confirms that charge storage occurs at the oxide/channel interface.

To further investigate the hysteresis width of transfer curves of bP-based devices, the electrical characterization was conducted in the temperature range from 150 to 340 K. Figure 3.3c shows the transfer curves at V_{ds} = 2 mV at different temperatures. The bP FET maintains its unipolar p-type conduction across the entire temperature range. As the temperature increases from 150 to 340 K, the conductance decreases, whereas the hysteresis width increases (Figure 3.3d, left axis), indicating enhanced thermally assisted trapping and de-trapping processes.[125] Moreover, in addition to the nearly ideal non-hysteretic transfer curve, the enhanced hole conduction observed at temperatures

lower than room temperature suggests the promising potential of bP for low-temperature electronic applications.

Figure 3.3d (right axis) reports the field-effect mobility as a function of temperature. Two competing phenomena typically govern the semiconductor mobility: at low temperatures, mobility increases with temperature due to the activation of charge carriers and the reduction of Coloumb scattering from impurities; at higher temperatures, phonon scattering becomes dominant, leading to a mobility decrease.[126] For bP transistors, the influence of charged impurities scattering is expected below 150 K. As the temperature increases from 150 to 340 K, the hole mobility of bP decreases from 283 to 33 $cm^2\ V^{-1}\ s^{-1}$.

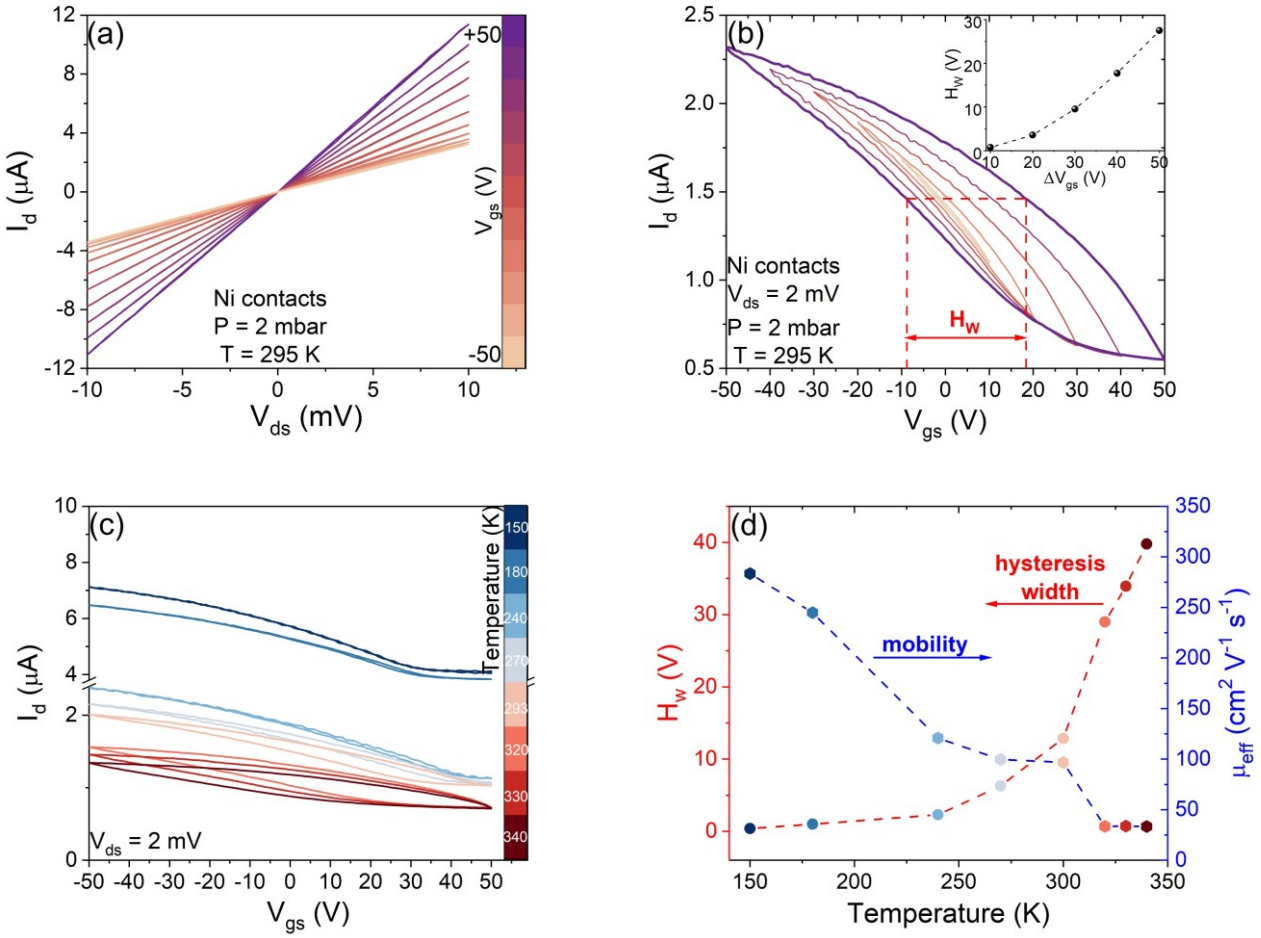


Figure 3.3: (a) Output curves of the bP devices with Ni contacts in vacuum and room temperature. (b) Transfer curves in vacuum and room temperature at V_{ds} = 2 mV and growing ΔV_{gs}. (in the inset: hysteresis width of the transfer curve as a function of ΔV_{gs}) (c) Transfer curves of the bP device in vacuum at V_{ds} = 2 mV at different temperatures from 150 to 340 K. (d) Hysteresis width and carrier mobility as a function of temperature.

3.1.3 bP FETs as memory devices

The presence of trap states is generally detrimental to transistor performance, as it leads to hysteresis and instability. However, these same traps can be advantageously exploited for the realization of non-volatile memory devices. In particular, the charge trapping at the bP/SiO_2 interface enables memory functionality without the need for an additional charge-storage layer, relying on the intrinsic traps present at the interface. Figure 3.4a shows the transfer characteristic of a bP

device in vacuum at room temperature. An evident hysteretic behaviour is observed, with a current window of approximately 0.3 µA. The current window (ΔI_d) is defined as the difference between the current values measured at V_{gs} = 0 V during the backward (I_{up}) and forward (I_{down}) sweeps, such that $\Delta I_d = I_{up} - I_{down}$. As shown in the inset of Figure 3.4a, the current window increases with increasing ΔV_{gs}. To preserve the 90 nm-thick oxide layers, the memory behaviour was tested using ±30 V gate voltage pulses. Figure 3.4b illustrates a single program/erase cycle: the memory is set by applying a positive gate voltage pulse, then read at V_{gs} = 0 V, and subsequently reset by applying a negative gate voltage pulse. The two current levels recorded at V_{gs} = 0 V correspond to the logic one and zero states. The switching between the two states can be repeated without degradation, indicating good endurance and operational stability (Figure 3.4c).[127]

Since the hysteresis width of transfer curves increases with temperature, the memory behaviour was also investigated at elevated temperatures. Figure 3.4d presents the memory measurements from room temperature to 340 K, showing the two well-separated and stable current states at V_{gs} = 0 V. The inset of Figure 3.4d reports the separation between the two states as a function of temperature, demonstrating its progressive increase with increasing temperature.

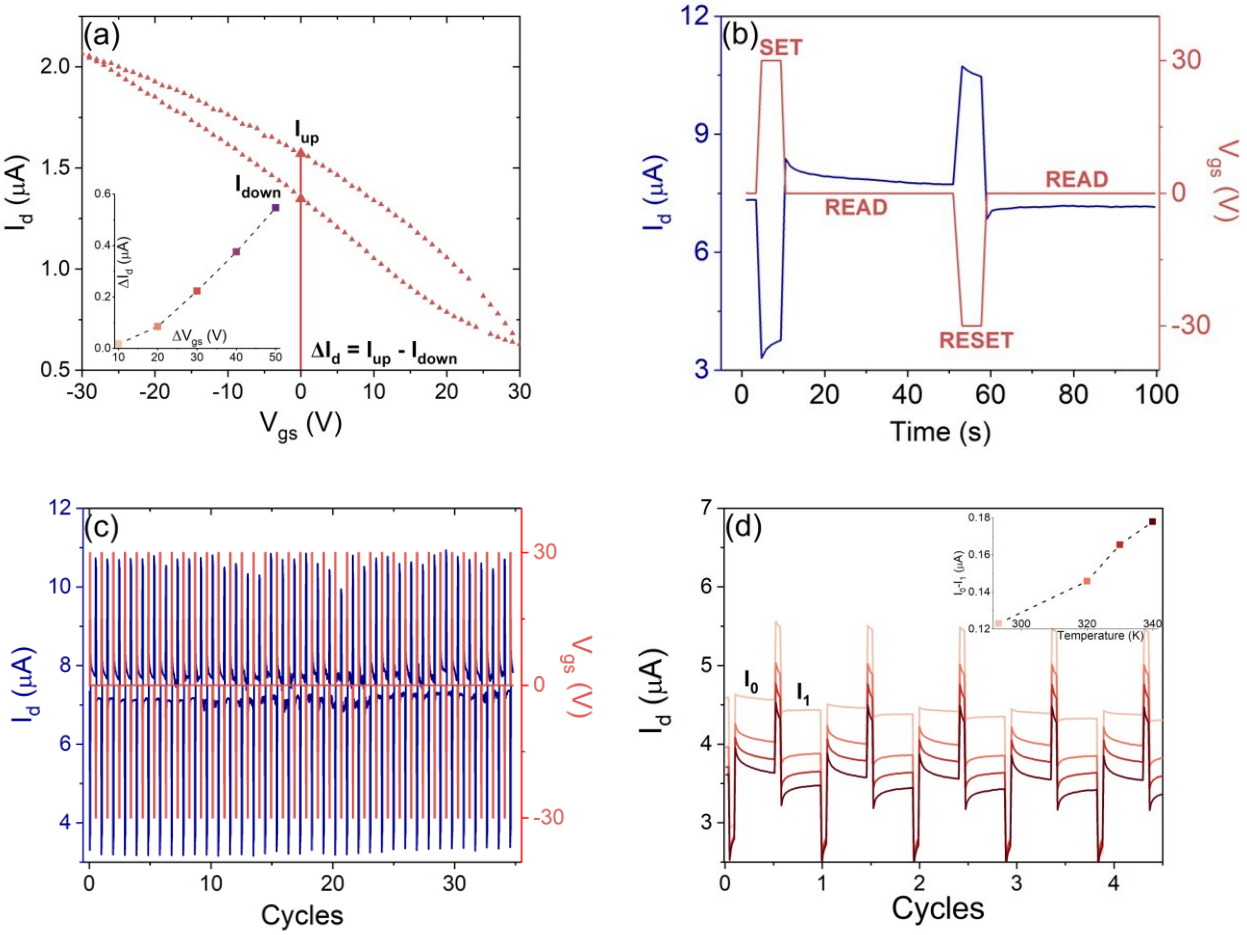


Figure 3.4: (a) Transfer curve of bP device in vacuum at room temperature. I_{up} and I_{down} are the current level at V_{gs} = 0 V. (in the inset: current window as a function of the gate voltage range) (b) One-cycle of memory behaviour of the bP device. (c) Multiple cycles of memory behaviour of the bP device. (d) Memory behaviour of the bP device at different temperatures higher than room temperature. (in the inset: current separation between the zero and one logic states as a function of temperature)

3.1.4 bP FETs as photodetectors

The fabricated bP device was tested as a photodetector in vacuum and at room temperature, with V_{ds} = 2 mV and V_{gs} = 0 V. Time-resolved photoresponse measurements were performed under white light illumination at different incident optical powers and exposure times. Figure 3.5a shows the device response to light pulses with incident optical powers ranging from 2.5 to 12.6 µW. The photocurrent is plotted as a function of incident power in the inset of Figure 3.5a. At higher powers, I_{ph} exhibits a linear dependence on the incident optical power, whereas at lower powers this dependence becomes less evident. The inset of Figure 3.5b presents a series of light pulses recorded at a fixed incident optical power of 12.6 µW and different exposure times, from 3 to 10 minutes. Figure 3.5b shows the exponential fitting of the decay branch of the light pulse measured under a 10 min-exposure. The very slow decay of the photocurrent suggests that the photoresponse is dominated by charge excitation from trap sites, rather than by conventional electron-hole pair generation.

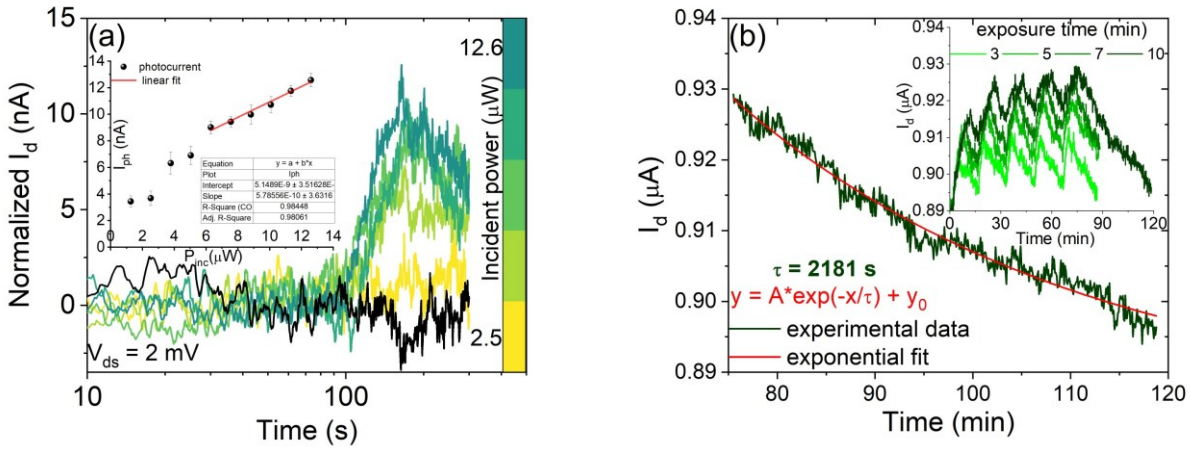


Figure 3.5: (a) Normalized light pulses at V_{ds} = 2 mV and V_{gs} = 0 V at different incident optical powers from 2.5 to 12.6 µW. The dark line is the curve in dark conditions, while the coloured ones are under white light illumination. (in the inset: photocurrent as a function of the incident optical power, with linear fit (red line) at high powers). (b) Current decay and exponential fit of the current after 10 min laser exposure time. (in the inset: light pulses at different exposure times)

3.2 Black phosphorus/molybdenum disulphide heterostructures

Building upon the fabrication methodology established in Section 2.1.1, this chapter presents a systematic investigation into the electrical and optoelectronic properties of bP/MoS_2 vdW heterostructures. To isolate the intrinsic transport mechanisms from environmental influences, the devices were characterized in a controlled vacuum environment, soon after the removal of the PMMA coating layer. The study evaluates the heterojunction's performance across a wide range of operating temperatures and under varying optical illumination, providing insight into the charge transfer and carrier dynamics at the bP/MoS_2 interface.

3.2.1 Materials characterization

Figure 3.6a shows a false-colour AFM image of a device from this batch of fabrication. To estimate the thickness of the bP and MoS_2 flakes, multiple profiles were extracted from the region indicated with a black dotted line. Representative height profiles are reported in Figure 3.6b, indicating a bP

thickness of approximately 151 nm (left graph), and a MoS_2 thickness of around 1.9 nm (right graph). The measured MoS_2 thickness is typical for a monolayer, despite the apparent difference to its nominal thickness, which is 0.7 nm; this difference can be attributed to process residues and ubiquitous water layers.[128,129] To further confirm the MoS_2 monolayer nature and the successful formation of the heterojunction, we performed Raman spectroscopy of the single flakes and at their interface.

Figure 3.6c shows the Raman spectra of the MoS_2 flakes acquired before and after the fabrication process. All the spectra exhibit the characteristic peaks of monolayer MoS_2 at 383 and 408 cm^{-1}, corresponding to the $E_{2g}{}^1$ and A_{1g} phonon modes, respectively. The preservation of these features confirms that the fabrication procedure does not induce measurable damage to the material. The peak separation of approximately 21 cm^{-1} agrees well with reported values for monolayer MoS_2 and lies within the expected experimental uncertainty of about 0.5 cm^{-1}.[130,131] Furthermore, the Lorentzian fits of the two main peaks indicate that the analyzed MoS_2 flakes predominantly exhibit a polycrystalline structure. Figure 3.6d shows the Raman spectrum of the multilayer bP flake, and the analysis at the bP/MoS_2 interface. The black line indicates the bP spectrum with the main peaks at around 361 cm^{-1}, 439 cm^{-1}, and 466 cm^{-1}, corresponding to the $A_g{}^1$, B_{2g}, and $A_g{}^2$ phonon modes of bP. The Raman spectrum (green line) of the overlapping region, acquired at the bP/MoS_2 interface, presents both the bP and MoS_2 peaks, consistently with what obtained from the individual flakes. This signals the high quality of the flakes and the formation of the bP/MoS_2 heterojunction. Figure 3.6e illustrates the PL from the MoS_2 flake and the bP/MoS_2 heterojunction. The reduction in the peak intensity can be attributed to exciton dissociation and charge transfer at the bP/MoS_2 interface.[132]

The PMMA layer was removed using a sequential rinse in acetone and ethanol prior to the electrical measurements that were performed in two-probe configuration using the bP side as the forcing electrode of the transistor (Figure 3.6f).

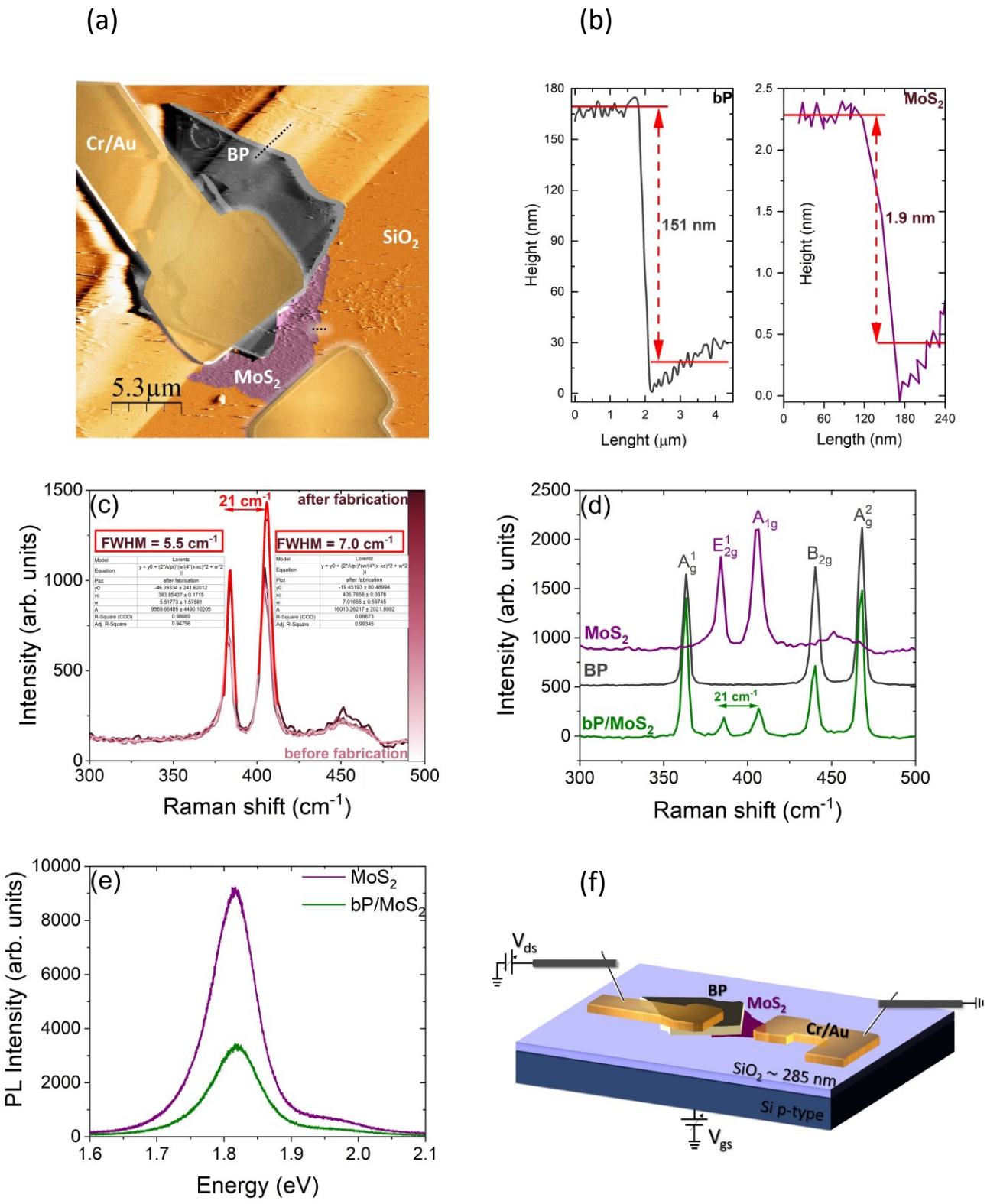


Figure 3.6: (a) AFM image (false color) of the bP/MoS_2 heterostructure contacted with Cr/Au bilayers. (b) AFM profiles of bP and MoS_2 flakes. (c) Raman spectra of MoS_2 flake before and after the fabrication process. (d) Raman spectra of bP (black line), MoS_2 (violet line), and heterojunction (green line). (e) Photoluminescence spectra of MoS_2 and bP/MoS_2 heterojunction. (f) schematic of the bP/MoS_2 heterostructure.

3.2.2 Electrical characterization of individual bP and MoS_2 FETs

Before analysing the charge transport of the bP/MoS_2 vertical interface, it is essential to characterize the individual constituents. To ensure the highest possible consistency, the single-flake FETs discussed in this section were fabricated using flakes from the same exfoliation and APCVD batches as those used for the heterostructures. Furthermore, they underwent identical lithography and metallization processes, allowing these devices to serve as an accurate baseline for the materials intrinsic properties and contact quality.

A key consideration in the fabrication of bP/MoS_2 heterostructures is the selection of a contact metal that can efficiently inject carriers into both the p-type bP and the n-type MoS_2. In our preliminary study on bP contact optimization (Section 3.1.1), we observed that Ni provided the lowest contact resistance for bP due to its high work function ($\phi_{Ni} \approx 5.1$ eV) aligning well with the bP valence band. However, for the heterostructure batch, Cr/Au was selected as the contact metallization. The decision was based on a dual-optimization strategy: bP compatibility and MoS_2 efficiency. While Cr ($\phi_{Cr} \approx 4.5$ eV) presents a slightly higher barrier for hole injection into bP compared to Ni, experimental results confirmed that bP FETs maintained Ohmic behaviour with acceptable current levels.[127,133] Moreover, it has been reported that, due to possible pinning effect, the electron barrier formed by Cr with multilayer BP can decrease below 0.1 eV with the increasing number of layers.[134] MoS_2 is a prototypical n-type semiconductor with a work function of approximately 4.2 eV. Using Ni would result in a significant Schottky barrier for electrons, leading to high contact resistance and non-linear transport.[135] Cr, with its lower work function, provides a much better alignment with the MoS_2 conduction band, ensuring efficient electron injection. The combination of MoS_2 and Cr results in the formation of a Schottky contact for electrons, characterized by a barrier that is 0.4-0.5 eV.[136,137]

Figure 3.7a-b show the optical image of an individual bP and MoS_2 FET, respectively. All the measurements were performed at room temperature and in vacuum at a pressure of 0.7 mbar. These conditions allow a meaningful comparison with the measurements carried out with the bP/MoS_2 heterostructure, detailed in the following sections. As shown in Figure 3.7c-d, the bP device exhibits the expected p-type behaviour. The output characteristics remain linear at low bias, confirming that the Cr/Au interface maintains ohmic-like injection for holes in bP. In contrast, the MoS_2 FET displays unipolar n-type conduction (Figure 3.7e-f), with current modulation spanning seven orders of magnitude.

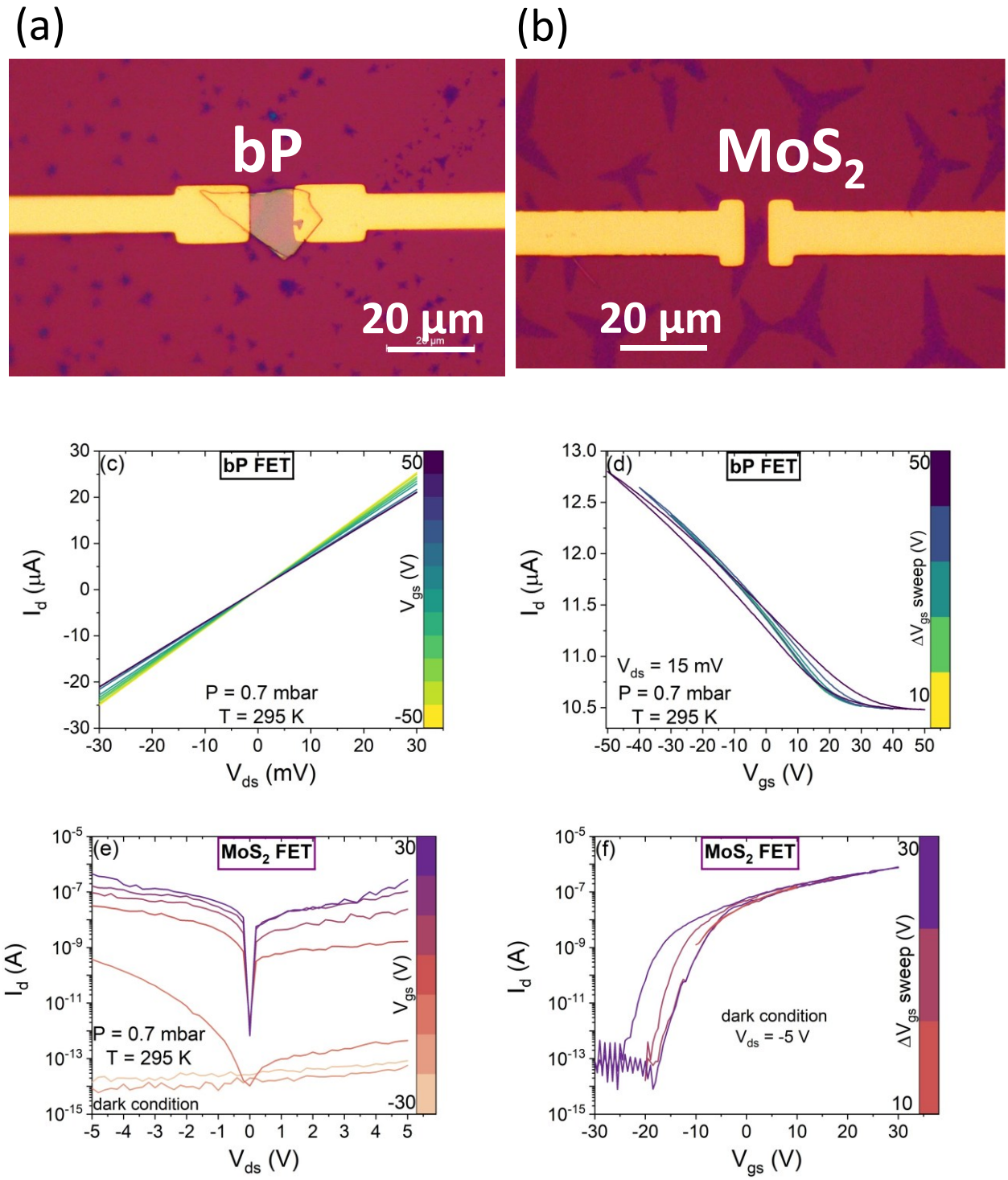


Figure 3.7: (a) Output and (b) transfer characteristics at V_{ds} = 15 mV at different ΔV_{gs} ranges of the bP FET. (c) Output and (d) transfer characteristics at V_{ds} = -5 V at different ΔV_{gs} ranges of the MoS_2 FET.

To accurately determine the intrinsic performance of the individual flakes and the impact of the metal-semiconductor interface, the Y-function method was applied to the transfer characteristics of both the bP and MoS_2 devices. The characteristic plots of the Y-function method are depicted in Figure 3.8. The analysis was performed using the sets of transfer curves obtained at different V_{gs} sweeps, as reported in Figure 3.7d-f. By decoupling the effect of contact resistance from the channel

transport, we extracted the low-filed mobility μ_0. The maximum values obtained for the baseline devices are 269 $cm^2 V^{-1} s^{-1}$ for bP and 0.58 $cm^2 V^{-1} s^{-1}$ for MoS_2.

The contact resistance per unit width was subsequently determined to evaluate the efficiency of the Cr/Au metallization. The extracted values are 8.9 kΩ µm for the Cr/bP interface and 2000 kΩ µm for the Cr/MoS_2 interface. As expected, the contact resistance for Cr/bP interface falls between the values previously observed for pure Ni and NiCr alloy contacts. This result is consistent with the work function alignment: while Ni provides the most favourable alignment for hole injection into the p-type bP, Cr offers an intermediate barrier height that is higher than Ni but remains significantly lower than that of the NiCr alloy. Thus, the Cr/Au metallization provides a balanced electrical platform, maintaining high mobility in bP while ensuring the necessary electron injection for the MoS_2 component of the vertical heterojunction.

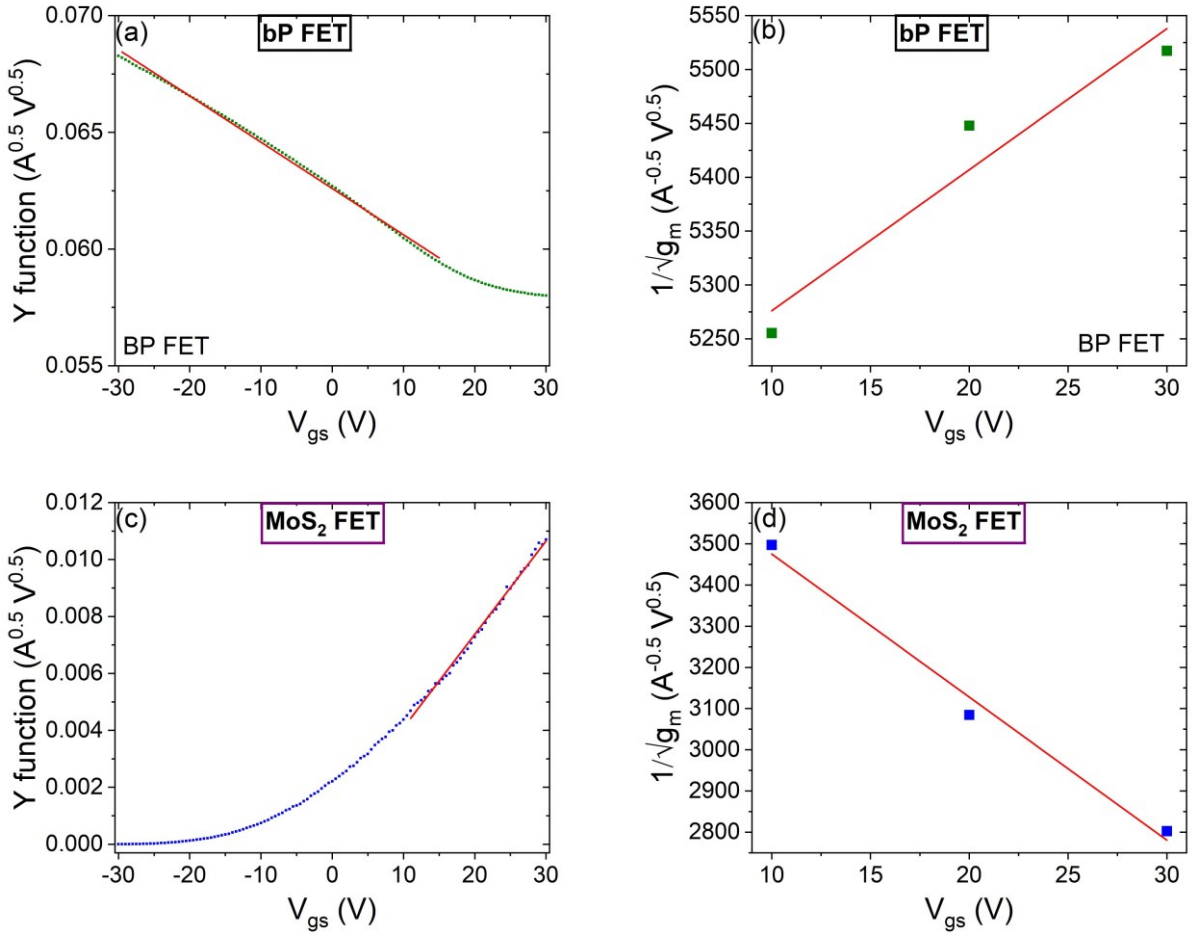


Figure 3.8: (a) Y-function vs V_{gs} and (b) 1/√gm vs V_{gs} for the bP device. (c) Y-function vs V_{gs} and (d) 1/√gm vs V_{gs} for the MoS_2 device. The red lines indicate linear fit of experimental data. The extracted values are 8.9 kΩ µm for the Cr/bP interface and 2000 kΩ µm for the Cr/MoS_2 interface.

3.2.2 Electrical characterization and band diagram model

Figure 3.9 show the output characteristics of the bP/MoS_2 heterostructure under dark conditions with V_{gs} stepping from 0 to 30 V in steps of 10 V. With the drain either on MoS_2 (Figure 3.9a) or bP (Figure 3.9b), I_d rises when V_{gs} increases from 0 to 30 V, indicating the dominant n-type behaviour of the bP/MoS_2 device. The ability of the gate to modulate the current and the rectifying behaviour of

the device is noteworthy; it shows that the gate voltage can affect the Schottky barriers at the interface Cr/MoS_2 in the bP/MoS_2 device and lead to a more balanced bidirectional charge transport.[138]

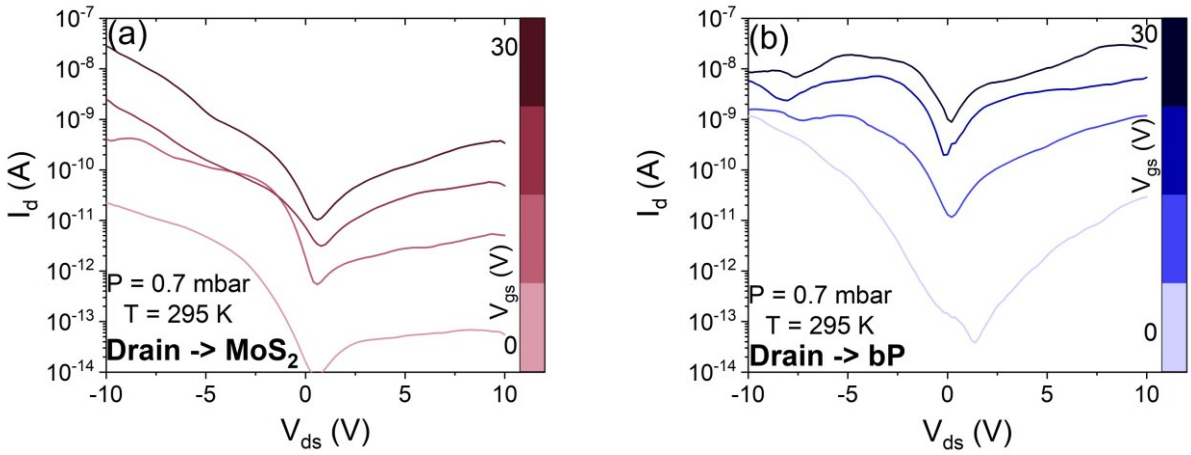


Figure 3.9: Electrical characterization of the bP/MoS_2 heterostructure under dark conditions using the (a) MoS_2 and (b) bP side as the forcing electrode.

The presented electrical behaviour of the bP/MoS_2 heterostructure deviates from the standard rectified transport typically reported in literature.[111–115,139] Most notably, the current reaches its maximum magnitude at negative V_{ds}, regardless of whether the drain electrode is place on the MoS_2 or the bP flake. A similar behaviour has been reported for MoS_2 transistors with asymmetric contacts: the transport is not solely governed by the p-n junction interface but is heavily influenced by the asymmetric injection barriers at the Cr contacts.[140,141] These results can be explained by considering the band alignment of the two involved semiconductors and Cr.

Figure 3.10a depicts the band diagrams of MoS_2 and bP, referring to a common vacuum level at thermal equilibrium. Considering the thickness of the two flakes extracted previously, the work function (ϕ), electron affinity (χ), and energy bandgap (E_{gap}) for MoS_2 are 4.5, 4.2, and 1.8 eV [115,142–144], while for BP, they are 4.2, 4, and 0.3 eV [115,145,146], respectively. According to Anderson's rule, the contact between MoS_2 and bP forms a type-II (staggered) heterojunction, as illustrated in Figure 3.10b. At the bP/MoS_2 interface, a small conduction band offset ($\Delta E_c \approx 0.15$ eV) exists. This barrier is sufficiently small to allow electron thermionic emission and tunneling, meaning it does not significantly impede electron flow. The resulting band bending promotes the accumulation of electrons from MoS_2 and holes from bP at the bP/MoS_2 interface.

When bP is positively biased relative to MoS_2 (Figure 3.10c), the bP bands shift downward, reducing the potential barrier. This facilitates the injection of holes from bP and electrons from MoS_2 into the overlap region, where they recombine. However, in this configuration, the current is limited by the Cr/MoS_2 Schottky barrier (0.4-0.5 eV[136,137]), which limits the supply of electrons into the system. Vice versa, when bP is negatively biased (Figure 3.10d) with respect to MoS_2, the current is primarily composed of electrons injected from the Cr contact into the bP and electron-hole pair generation within the depletion region. Fundamentally, the Cr/bP injection barrier is lower than the Cr/MoS_2 barrier. This disparity explains why the current magnitude is higher at negative V_{ds}: the system can pull more carrier through the Cr/bP interface than it can through the Cr/MoS_2 interface.

Since the lowest energy state for holes is on the bP side and the lowest energy state for electrons is on the MoS_2 side of the heterojunction, charge separation can readily occur, causing also a significative photoresponse (Figure 3.10e).

According to this model, the overall charge flow is dominated by the electron transport in the MoS_2, which acts as the most resistive element in the heterostructure. This accounts for the observed n-type gate modulation of the device. Nevertheless, the narrow bandgap of bP plays a vital role; it acts as the primary site for electron-hole generation and recombination. This contribution is essential for the high-speed photoresponse, and the significant photovoltaic effect observed in the self-powered mode, as the type-II alignment ensures that photogenerated carriers are efficiently separated before they can recombine.

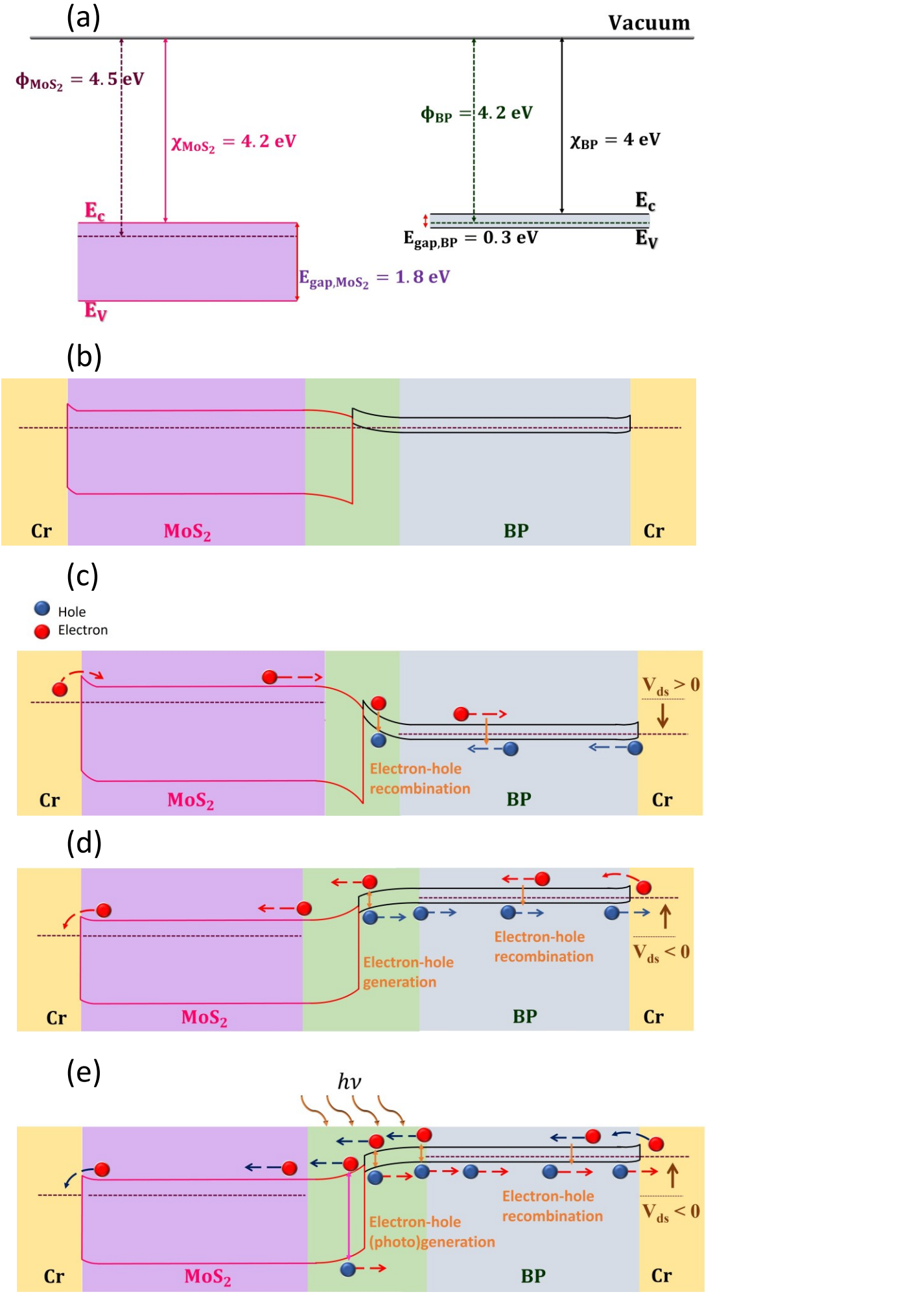

(a)
Vacuum
$\phi_{MoS_2} = 4.5$ eV
$\chi_{MoS_2} = 4.2$ eV
E_c
E_V
$E_{gap,MoS_2} = 1.8$ eV
$\phi_{BP} = 4.2$ eV
$\chi_{BP} = 4$ eV
E_c
$E_{gap,BP} = 0.3$ eV
E_V
(b)
Cr
MoS_2
BP
Cr
(c)
Hole
Electron
$V_{ds} > 0$
Electron-hole recombination
Cr
MoS_2
BP
Cr
(d)
Electron-hole generation
Electron-hole recombination
$V_{ds} < 0$
Cr
MoS_2
BP
Cr
(e)
$h\nu$
Electron-hole (photo)generation
Electron-hole recombination
$V_{ds} < 0$
Cr
MoS_2
BP
Cr

Figure 3.10: (a) Band profiles of MoS_2 (violet) and bP (gray) when the two flakes are separated. The work function and the electron affinity of MoS_2 and bP are referred to the vacuum level. Band alignment of bP/MoS_2 type-II heterojunction and Cr (b) in thermal equilibrium state, (c) with a positive bias on bP, (d) with a negative bias on bP, and (e) with a negative bias on bP under illumination (the Cr contact on MoS_2 is assumed to be grounded).

3.2.3 Optoelectronic characterization

The photoresponse of the bP/MoS_2 heterostructure was evaluated under white light illumination with varying incident optical powers. Figure 3.11a-b present the I-V characteristics with grounded gate and transfer characteristics of the device in dark (black line) and under illumination (coloured lines), respectively. The I-V characteristics (Figure 3.11a) clearly display the reverse rectification behaviour discussed in the previous section, where higher current magnitudes are achieved at negative V_{ds}. As established in our band diagram model, this stems from the fact that the injection barrier at the Cr/bP interface is significantly lower than at the Cr/MoS_2 interface. The light-induced current follows this same trend: while the absolute photocurrent increases with light intensity, the overall shape of the curves remains unchanged. This confirms that the internal field of the heterojunction and the contact barriers are the primary factors directing charge flow, even under high injection levels. The transfer characteristics (Figure 3.11b) confirm that the gated heterostructure maintains a dominant n-type channel conductance, consistent with the model where MoS_2 acts as the primary resistive and transport-governing layer. Upon exposure to white light, a significant enhancement in the drain current is observed across all bias regimes. Notably, the device exhibits a higher photosensitivity, defined as the ratio I_{light}/I_{dark}, at $V_{ds} > 0$ V and in the depletion region. i.e. $V_{gs} < 0$ V. In these regimes, the dark current is effectively suppressed by the Cr/MoS_2 Schottky barrier and the gate-induced depletion of the MoS_2 channel. The introduction of photogenerated carriers significantly lowers these barriers and increases the carrier density, leading to a much higher relative change in current compared to the high-conductance state at $V_{gs} > 0$ V.

To investigate the switching speed and the stability of the photoresponse, we performed time-resolved measurements by modulating the light source at a constant bias. Figure 3.11c-d show the white light pulses measured at $V_{ds} = 5$ V and $V_{ds} = -5$ V, respectively, under exposure to 30 s laser pulses of increasing power from 10 to 50 µW.

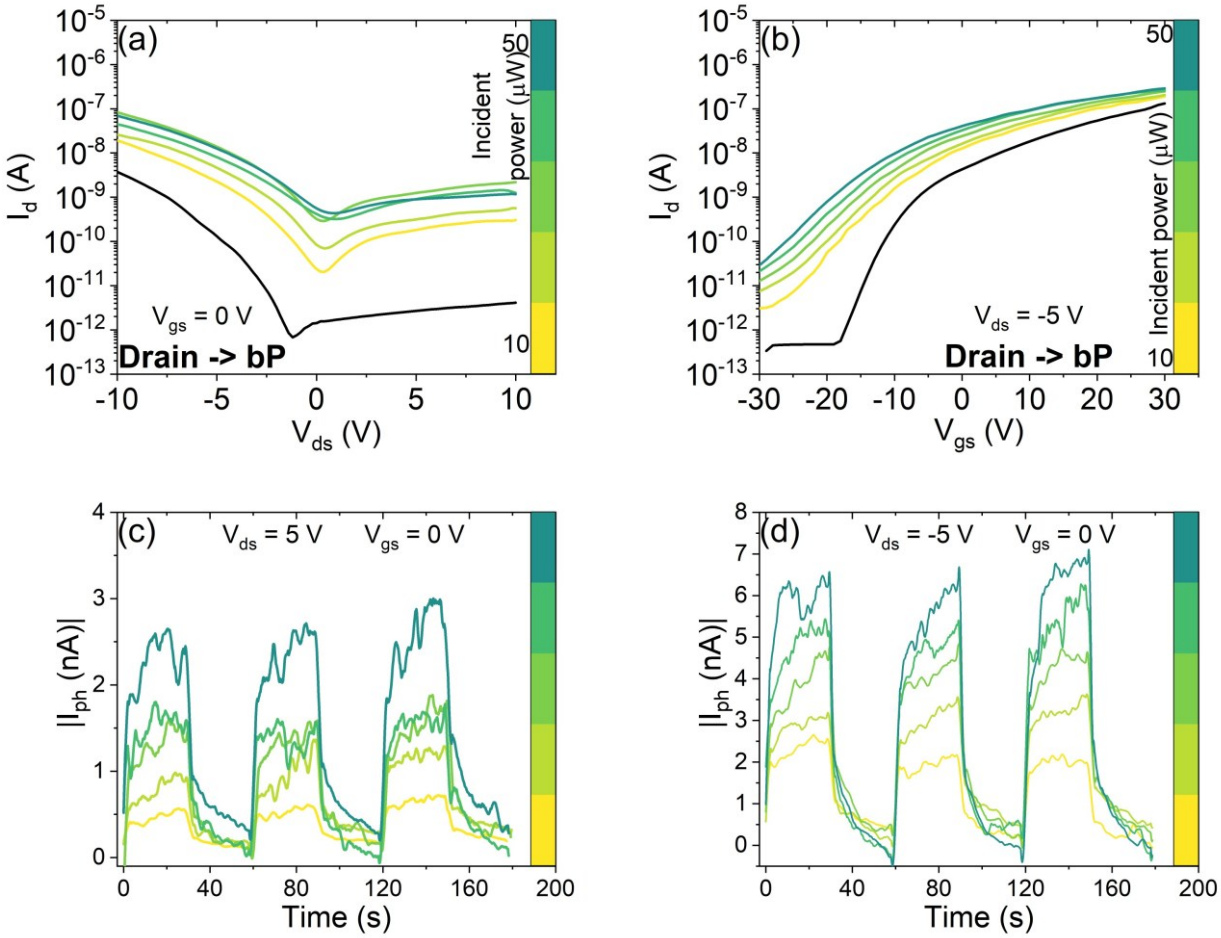


Figure 3.11: (a) I-V and transfer (b) characteristics of the bP/MoS_2 heterostructure in dark (black line) and under white light illumination (colored lines) at different intensities. The I-V characteristics are measured with grounded gate (V_{gs} = 0 V). 30 s white light pulses at (c) V_{ds} = 5 V and (d) V_{ds} = -5 V.

To gain deeper insight into the carrier recombination and trapping dynamics, the time-resolved photocurrent pulses were analyzed using a multi-exponential fitting approach. As shown for a representative pulse at P_{inc} = 30 μW (Figure 3.12a-b), both the rise and decay phases were accurately modelled using a double exponential function: $I_{ph} = I_0 + a_1 \exp\left(-\frac{t-t_0}{\tau_1}\right) + a_2 \exp\left(-\frac{t-t_0}{\tau_2}\right)$. The extraction of two distinct time constants, τ_1 and τ_2, suggests the presence of two competing relaxation mechanisms. The fast component (τ_1) is typically associated with the intrinsic recombination of photogenerated carriers within the overlap region. In contrast, the slower component (τ_2) is indicative of trap-mediated dynamics, likely involving long-lived states at the bP/MoS_2 interface or sulphur vacancies in the MoS_2 flake. This kinetic behaviour confirms that while the heterojunction effectively separates charge, the overall response speed is modulated by the defect distribution inherent to the constituent 2D materials.

The photocurrent exhibits an average characteristic rise time (τ_1) of 300 ms and a decay time (τ_2) of 1400 ms at V_{ds} = 5 V (Figure 3.12c), and a rise time (τ_1) of 200 ms and a decay time (τ_2) of 1000 ms at V_{ds} = -5 V (Figure 3.12d). Notably, both photocurrent rise (τ_1) and decay (τ_2) times are smaller than those observed in recently reported phototransistors with MoS_2 channel.[147] These shorter relaxation times suggest that the faster photoresponse of the bP/MoS_2 device is due to the presence of bP

which has a mobility more than an order of magnitude higher than MoS_2.[146–148] We point out that the response time can be further lowered by reducing the carrier path to the electrodes for instance by reducing the bP or MoS_2 extensions out of the junction region or by changing the device layout to obtain a truly vertical device.

Figure 3.12e-f show that the photocurrent, which results to be higher at negative V_{ds}, depends linearly on the incident laser power (from 10 to 50 μW). This is a desirable feature in a photodetector, related to its ability to distinguish varying light intensities. The linear dependence of photocurrent on the incident laser power aligns with results reported for both phototransistors with 2D single[147,149] or heterojunction channel.[113,139]

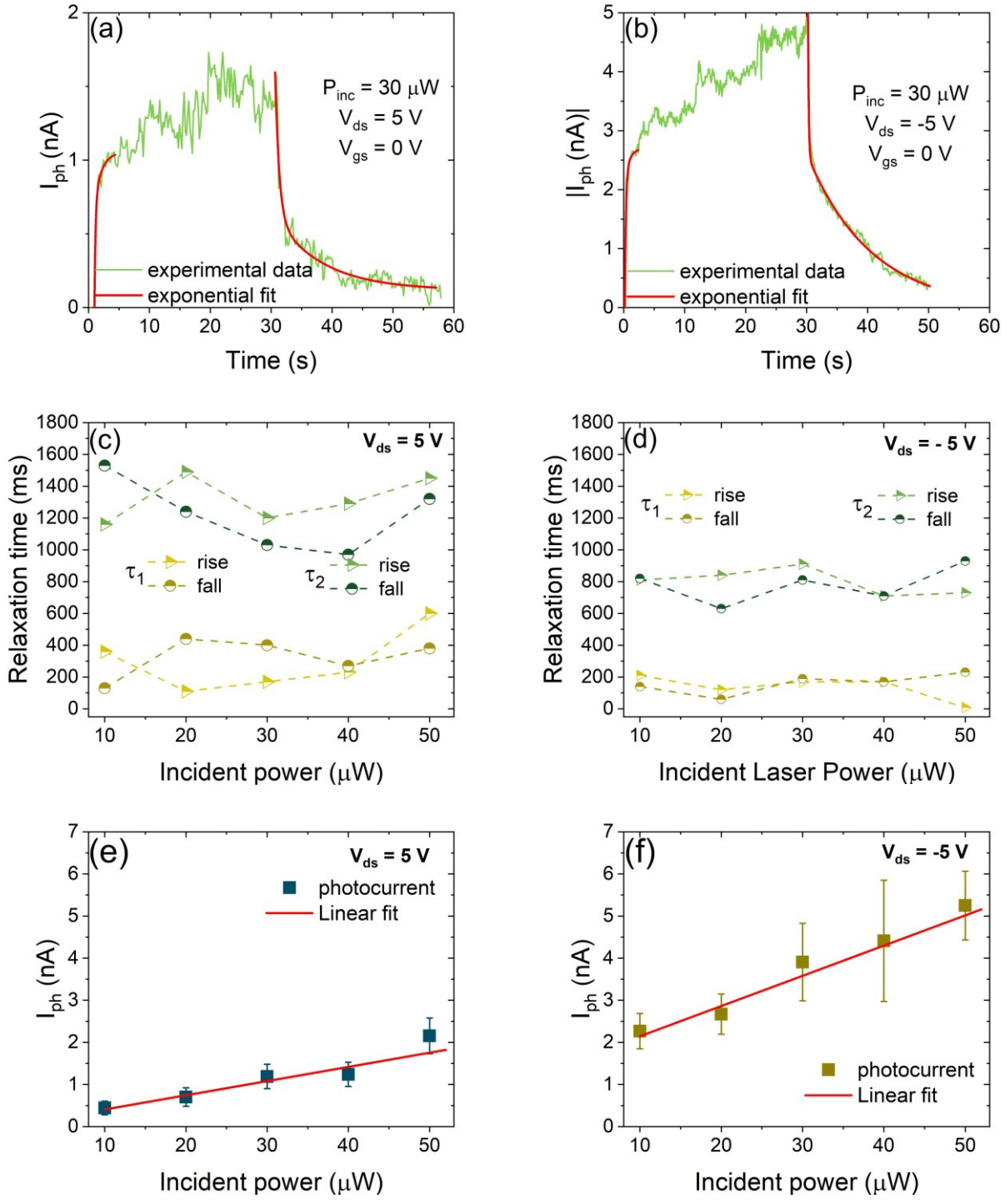


Figure 3.12: 30 s long pulses vs time at T = 295 K and P = 0.7 mbar at P_{inc} = 30 μW at (a) V_{ds} = 5 V and (b) V_{ds} = -5 V fitted by a double exponential growth/decay (red line). Relaxation time as a function of the incident laser power for the rising and falling part of the pulses at (c) V_{ds} = 5 V and (d) V_{ds} = -5 V. Photocurrent as a function of the incident optical power at (e) V_{ds} = 5 V and (f) V_{ds} = -5 V. The red lines represent a linear fit.

Figure 3.13 shows the electrical characterization of the bP/MoS_2 heterostructure, in terms of I-V and transfer characteristics, under different light conditions temperatures below (250 K) and above (350 K) the room temperature. The measurements demonstrate that the overall features of the device, namely rectification, photoconduction and gate modulation, are preserved over a wide range of temperatures, which is a remarkable property of the bP/MoS_2 heterojunction-based devices under

study. It can be observed that, as expected for an energy barrier-controlled device, the rectification ratio and the gate modulation improve while reducing the temperature. Noteworthy, an increase of the current under illumination with enhancing incident optical power is observed both at lower and higher temperatures.

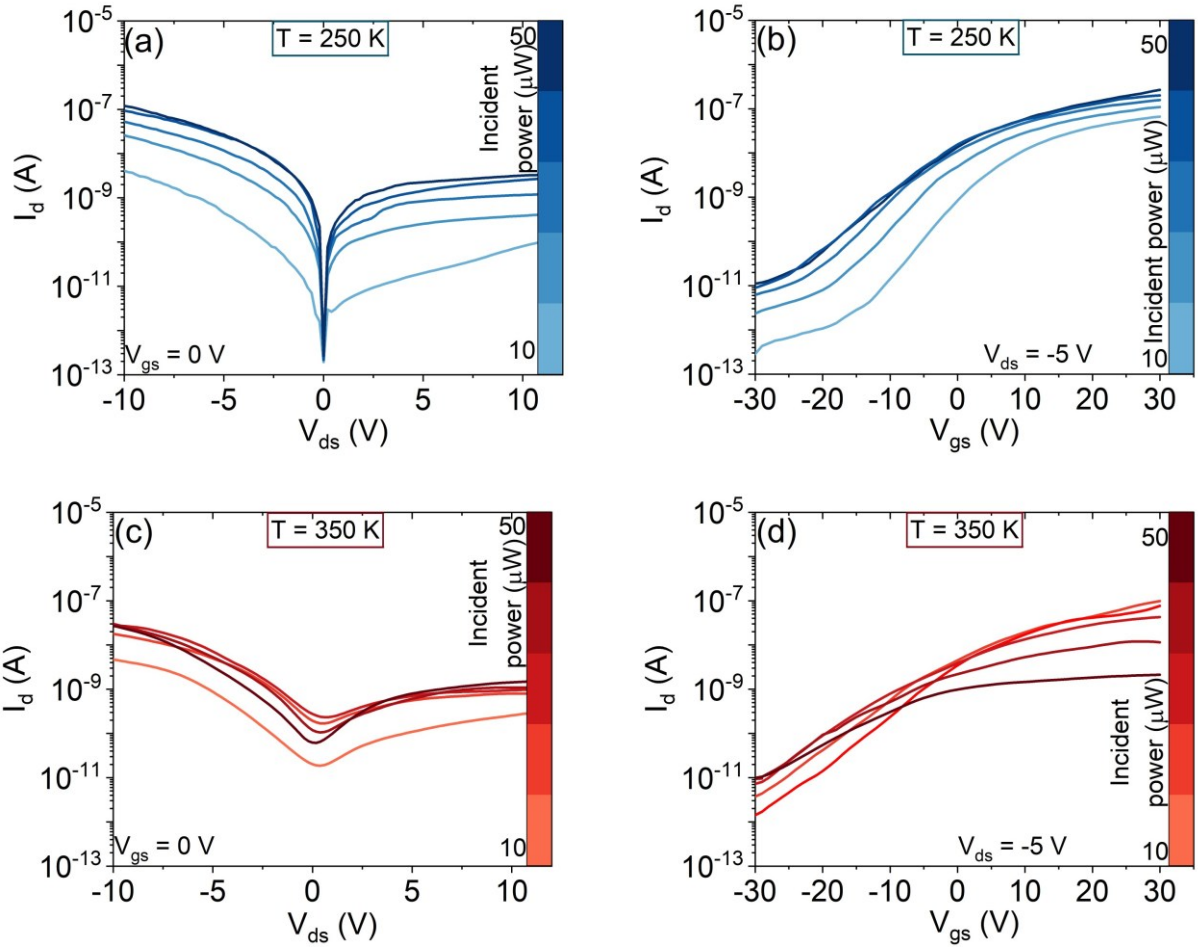


Figure 3.13: I-V (a-c) and transfer (b-d) characteristics of the bP/MoS_2 device under illumination at different incident optical powers and at the temperatures of 250 K (blue) and 350 K (red). The I-V characteristics are measured with grounded gate.

3.2.4 Self-powered photodetector

To further explore the potential of the bP/MoS_2 heterostructure for energy-efficient optoelectronics, we investigated its performance in self-powered mode. Unlike the previously discussed two-terminal FETs, this study utilized a dedicated device in a four-probe configuration (4PP), as shown in the optical image in Figure 3.14a. The device was fabricated using the same fabrication protocols detailed in Section 2.1.1. Figure 3.14b presents a schematic illustration of this measurement setup. For 4PP I-V measurements the inner contacts (V_1 and V_2) were used to measure a varying voltage, $V_d^{4PP} = V_2 – V_1$. On the contrary, for 2PP I-V measurements, the voltage was measured between the source (S) and drain (D) of the transistor, $V_d^{2PP} = V_D - V_S$. The p-doped Si substrate (G) acted as a gate electrode. This geometry allows for a more precise evaluation of the intrinsic transport across the vertical heterojunction by minimizing the influence of longitudinal channel resistance.

The impact of this 4PP configuration is quantified in Figure 3.14c, which compares the I-V characteristics of the bP/MoS_2 heterojunction measured in darkness, at a pressure of 0.3 mbar and ambient temperature, in standard 2PP (red dashed line) and 4PP (black solid line) configurations. The 4PP configuration removes the effect of the contact resistance between Cr and the two 2D materials.[150] Hence, a more conductive device is expected in 4PP configuration. However, Figure 3.14c shows that the 2PP and 4PP curves almost overlap, indicating that the Cr/MoS_2 and Cr/bP contact resistances are negligible compared to the resistance of the bP/MoS_2 channel. Indeed, the contact resistance in these devices is usually dominated by the Cr/MoS_2 interface, because of a Schottky barrier and Fermi level pinning due to interfacial states, as detailed in Section 3.2.2.

The solid yellow curve in Figure 3.14c indicates the I-V characteristic of the bP/MoS_2 device in 4PP under white light illumination at an incident power of 126 µW. Under illumination, the bP/MoS_2 heterostructure is more conductive and the I-V curve undergoes a rightward shift, indicating the presence of a photovoltaic effect (inset of Figure 3.14c).[151] The internal electric field created by the type-II staggered band alignment at the bP/MoS_2 interface enables the separation of photogenerated carriers without the need for an external bias. This produces a short circuit current $I_{sc} \approx 0.12$ nA and an open circuit voltage of $V_{oc} \approx 75$ mV. Figure 3.14d shows the 4PP I-V curves of the heterojunction, under laser light at $P_{inc} = 1.3$ µW at fixed wavelengths in the visible-light range, from 450 to 700 nm. The rectifying behaviour of the heterojunction is reproduced, with conductivity depending on the wavelength of the incident radiation. The photovoltaic effect is still present, with I_{sc} and V_{oc} depending on the wavelength of the incident radiation, as shown by the inset in Figure 3.14d. The wavelength-resolved short circuit current measurements are shown in Figure 3.14e. I_{sc} exhibits a strong dependence on the wavelength, attaining a maximum value of 1.5 pA at the wavelength $\lambda = 600$ nm. The correspondent responsivity at zero bias is equal to R = 1.2 µA/W at 600 nm. The energy of this radiation is close to MoS_2 bandgap energy, indicating that the maximum current I_{sc} is achieved when both 2D materials contribute to photogeneration. The wavelength-resolved open circuit voltage measurements are reported in Figure 3.14f, showing a similar effect for V_{oc}. A maximum value of $V_{oc} = 2.5$ mV is reached at $\lambda = 600$ nm. The above-mentioned responsivity is measured under zero external bias, corresponding to short-circuit conditions. In this regime, the photogenerated carriers are separated solely by the built-in electric field at the heterojunction, without the assistance of an external field. When a finite drain bias is applied, the responsivity increases by more than two orders of magnitude. At $V_{ds} = 0.4$ V, a responsivity of approximately 340 µA/W is obtained under the same illumination conditions. The responsivity is limited by the low thickness of the two materials, which reduces light absorption, and by the presence of intragap states that promote photocarrier recombination.

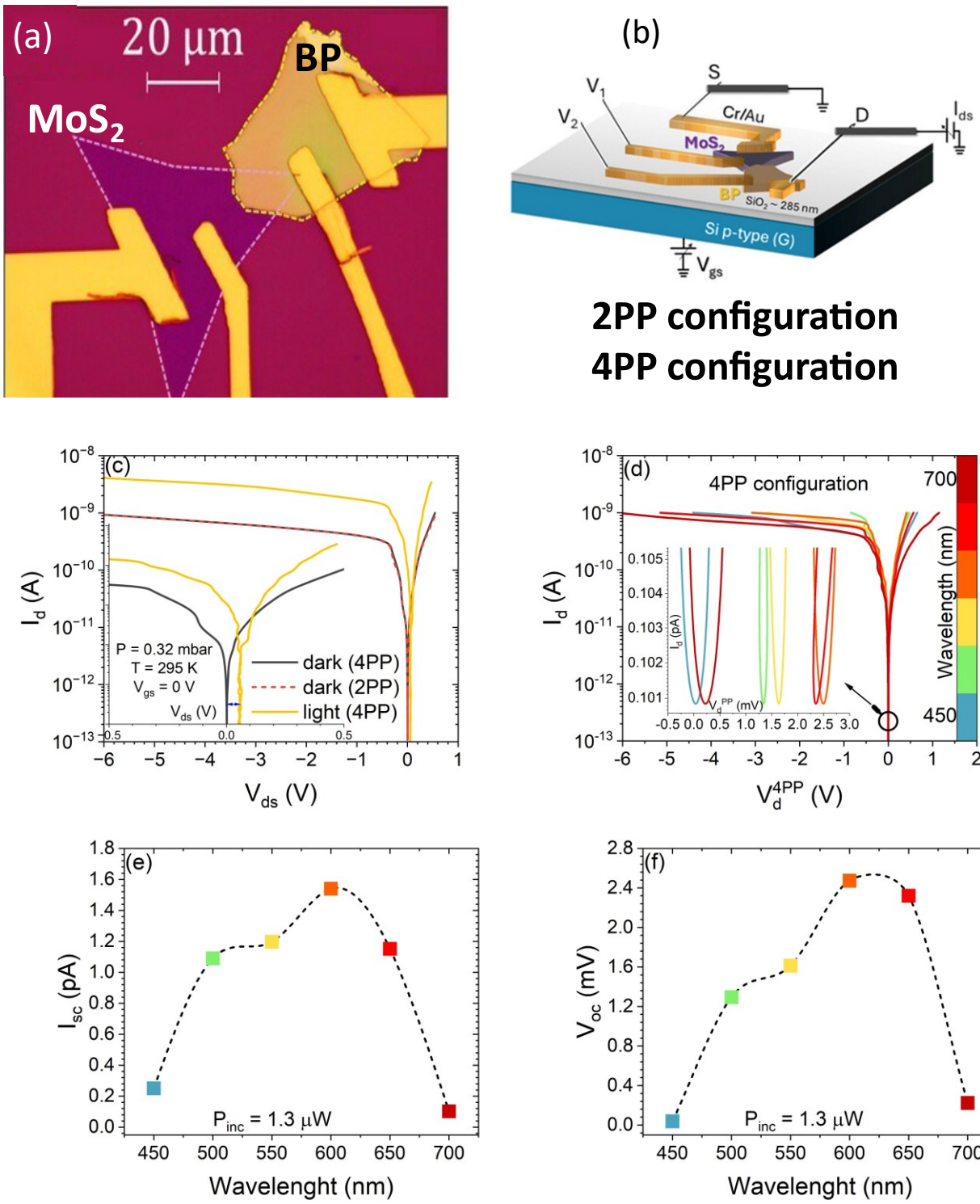


Figure 3.14: (a) Optical image of a four-terminal bP/MoS_2 heterostructure. (b) Schematic of the bP/MoS_2 device with Cr/Au leads with the measurement setup for the 2PP and the 4PP configurations. (c) 2PP and 4PP I-V characteristic at V_{gs} = 0 V at a pressure of 0.3 mbar and ambient temperature in dark (solid black line and dashed red line) and under white light illumination (solid yellow line). (in the inset: zoom of the 4PP I-V characteristics in the V_d range between -0.5 and 0.5 V, highlighting the rightward shift of the curve) (d) I-V characteristics of the heterostructure measured in 4PP configuration under monochromatic laser light with different wavelengths from 450 to 700 nm. (in the inset: magnified plot at zero current). The forcing current is limited to 10 nA, to avoid device damage. (e) Open circuit voltage and (f) short circuit current as a function of the wavelength.

4. TUNGSTEN DISULPHIDE/PALLADIUM DISELENIDE HETEROSTRUCTURES

This chapter focuses on the study of the $WS_2/PdSe_2$ heterostructures, fabricated as detailed in Section 2.1.2. The integration of WS_2 and $PdSe_2$ into vertical architectures enables the formation of vdW heterostructures that synergistically combine the advantageous electronic and optical properties of both constituents. This material platform pairs the wide, tunable, and direct bandgap of WS_2 with the high carrier mobility and narrow bandgap of $PdSe_2$. Fundamentally, both WS_2 and $PdSe_2$ exhibit robust environmental stability, maintaining their performance over time in ambient conditions, a factor that is essential for the transition from laboratory prototypes to real-world technological applications. Consequently, the $WS_2/PdSe_2$ system holds significant promise for a wide range of advanced devices, including high-performance FETs, photodetectors, photovoltaic cells, sensors, and neuromorphic devices. T. Chen et al.[152] leveraged the tunable polarity of a $WS_2/PdSe_2$ heterostructure to demonstrate its use as a reconfigurable rectifier, achieving rectification ratios ranging from 10^{-4} to 10^4. They also developed a logic inverter based on the dual-mode rectification capability of serially connected $WS_2/PdSe_2$ heterostructures. Furthermore, $PdSe_2$ thin films were decorated with WS_2 nanoparticles to enhance their gas-sensing capabilities, leveraging the catalytic effect and n-type doping introduced by the WS_2 nanoparticles. Gas sensors based on $WS_2/PdSe_2$ heterostructures exhibit approximately 2.8 times greater sensitivity and improved selectivity compared to pristine $PdSe_2$.[153]

To fundamentally understand the charge transport and interfacial physics governing this heterostructure, this chapter follows a systematic experimental progression. Before analysing the vertical heterojunction itself, it is necessary to establish the baseline performance of the individual building blocks. Therefore, we first examine the electrical characteristics of individual $PdSe_2$ and WS_2-based FET.

4.1 Palladium diselenide FETs

This section details a comprehensive investigation into the transport mechanisms of fabricated $PdSe_2$ devices. To decouple the intrinsic properties of the channel from the environmental effects, electrical characterization was performed in both vacuum and ambient pressure conditions. Furthermore, the device response was evaluated under exposure to specific gases, including O_2 and Ar, to elucidate the role of surface-mediated doping and trapping. Finally, we address the optoelectronic performance of the $PdSe_2$ channel. Given that the device exhibited no photoresponse under standard room-temperature conditions, a phenomenon also noted in literature for certain illumination regimes, measurements were extended to the low-temperature regime. By suppressing thermal noise at reduced temperatures, we aim to uncover the underlying photocurrent generation mechanisms and assess the potential of $PdSe_2$ for sensitive photodetection.

An optical image of a representative $PdSe_2$ FET is shown in Figure 4.1a. The device was fabricated following the maskless lithography and deterministic transfer detailed in Section 2.1.2 for the $WS_2/PdSe_2$ heterostructures. The optical contrast of the $PdSe_2$ flake against the 290 nm SiO_2 dielectric is indicative of its multilayer nature, which is confirmed via Raman spectroscopy (Figure 4.1b). The Raman spectrum highlights the high crystalline quality of the exfoliated flake, featuring the signature vibrational modes of multilayer $PdSe_2$. Specifically, the peaks observed at 140 cm^{-1}, 203 cm^{-1}, 219 cm^{-1}, and 255 cm^{-1} are attributed to the A_g^1, A_g^2, B_{1g}^2, and A_g^3 internal vibration modes,

respectively.[154–156] The prominent A_g^3 peak, in particular, serves as a reliable fingerprint for identifying the $PdSe_2$ phase and confirming the absence of structural degradation.[157]

Figure 4.1c reports the output curves with V_{gs} sweeping from -50 to 50 V in steps of 1 V. The favourable alignment of the Au Fermi level ($\phi_m \approx 5.1 – 5.3$ eV)[158] with that of $PdSe_2$ ($\phi_s \approx 5.0 – 5.2$ eV)[159–161] leads to the formation of an ohmic contact at the Au/$PdSe_2$ interface, as confirmed by the linear output characteristics. The higher current at positive V_{gs} indicates the n-type conduction of $PdSe_2$ in high vacuum (10^{-4} mbar). This is strongly supported by the transfer curves at V_{ds} = 10 mV reported in Figure 4.1d, with increasing voltage ranges, ΔV_{gs}, from 10 to 50 V. From the transconductance of the transfer curves, the electron mobility was calculated. Compared to the literature[162,163], the electron mobility is one order of magnitude higher, between 12 and 18 $cm^2\ V^{-1}\ s^{-1}$. As reported for similar devices with 2D materials as channel transistor, the mobility slightly depends on the ΔV_{gs}, showing a higher mobility at lower voltage ranges (see inset of Figure 4.1d).

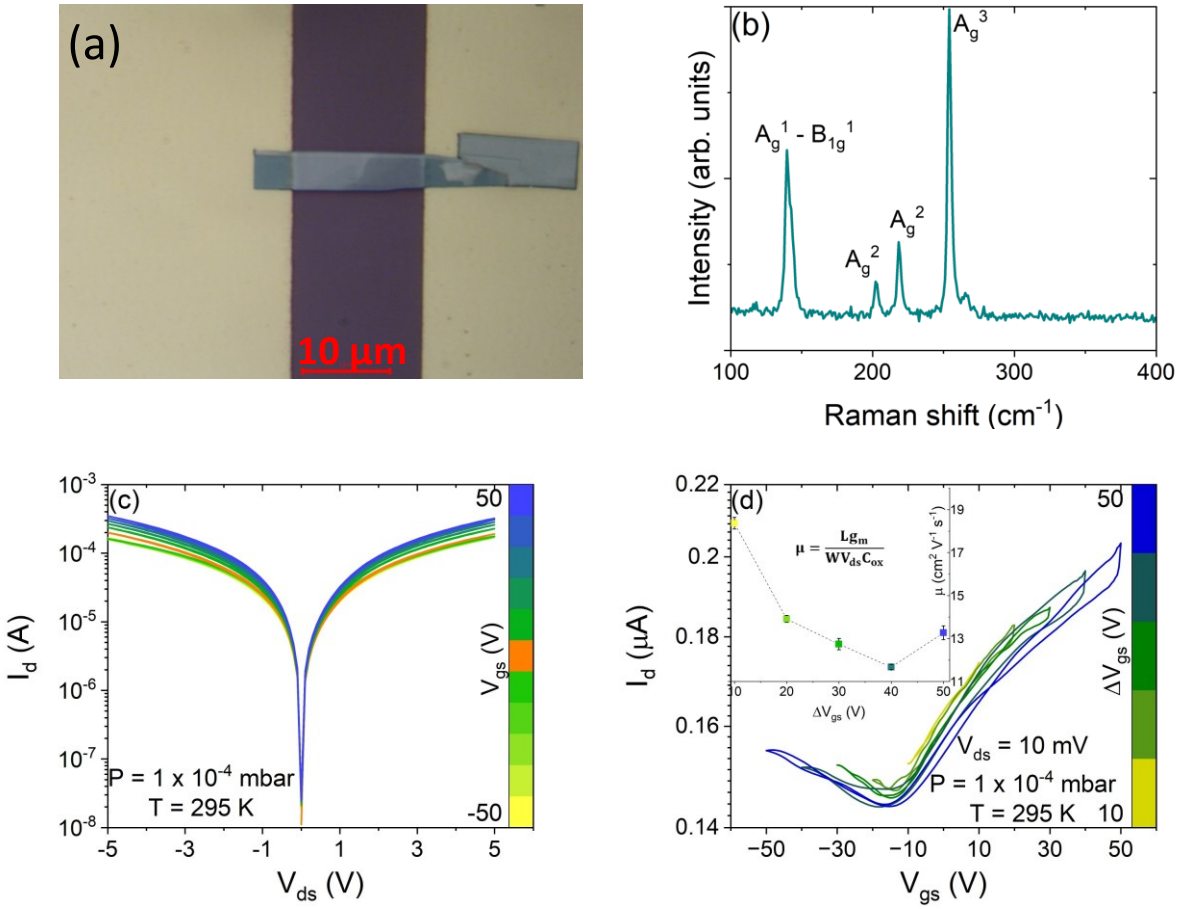


Figure 4.1: (a) Optical image of a $PdSe_2$ FET. (b) Raman spectrum of $PdSe_2$. (c) Output and (d) transfer characteristics of the $PdSe_2$ FET in high vacuum at a pressure of 10^{-4} mbar, under dark conditions (in the inset: the dependence of electron mobility on ΔV_{gs}).

4.1.1 Pressure-dependent conductivity in multilayer $PdSe_2$

The electrical response of the $PdSe_2$ FET was systematically investigated under varying pressure conditions, ranging from high vacuum (10^{-4} mbar) to ambient pressure (10^3 mbar). This analysis elucidates the profound impact of environmental species on the transport properties of the pentagonal $PdSe_2$ lattice.

Figure 4.2a shows the I-V characteristics at V_{gs} = 0 V of the $PdSe_2$ device as the pressure is increased. A significant reduction in channel conductance is observed with increasing pressure. This degradation is attributed to the physisorption of H_2O and O_2 molecules on the $PdSe_2$ surface. These species act as strong electron acceptors, i.e. p-dopants, which deplete the majority electron carriers in the n-type dominated vacuum regime. The transition in conduction polarity is further evidenced by the transfer characteristics shown in Figure 4.2b-c. In high vacuum, the device exhibits predominantly n-type behaviour. As the pressure rises toward ambient conditions, a clear p-type branch emerges at negative gate voltages, resulting in a transition to ambipolar conduction. The adsorption of moisture and oxygen effectively shifts the charge neutrality point toward positive gate voltages, a signal of p-type surface doping.[162] The transfer curves exhibit significant hysteretic behaviour, defined here as the gate voltage divergence between the forward (-50 to 50 V) and reverse (50 to -50 V) sweeps of the transfer curve at fixed I_d values. This hysteresis, which is investigated in more detail in the following, stems from a dual mechanism: intrinsic traps and extrinsic factors. The intrinsic traps are attributed to structural defects within the $PdSe_2$ flake, most notably selenium vacancies that act as localized charge traps. The extrinsic factors are associated with the presence of surface adsorbates, which introduce additional interfacial states. To ensure a high signal-to-noise ratio despite the low carrier mobility at low V_{ds}, the drain-source bias was maintained at V_{ds} = ± 3 V for these measurements. The influence of adsorption processes is evident at both positive (V_{ds} = 3 V) and negative (V_{ds} = -3 V) bias. When the pressure is varied from high vacuum to ambient conditions, the $PdSe_2$ device undergoes a transition from n-type to ambipolar conduction.

The evolution of electron mobility, $\mu_{electrons}$, as a function of pressure is presented in Figure 4.2d. At V_{ds} = 3 V, the mobility remains relatively stable at approximately 43 $cm^2\ V^{-1}\ s^{-1}$ in vacuum before dropping to 25 $cm^2\ V^{-1}\ s^{-1}$ at ambient pressure due to increased scattering and depletion from adsorbates. Interestingly, at V_{ds} = -3 V, the mobility values at low pressure are comparable but show an increase to around 60 $cm^2\ V^{-1}\ s^{-1}$ above 1 mbar. The observed mobility values are consistent with the multilayer nature of the flake. While higher mobilities have been reported for ultra-thin $PdSe_2$ flakes[164,165], the mobility in puckered 2D materials is known to decrease as layer thickness increases due to inter-layer coupling and increased bulk scattering centers.[166,167] The values recorded here are higher than the mobility values reported for $PdSe_2$ devices of similar thickness.[162]

The reversibility of these processes was tested by cycling the pressure from ambient back to high vacuum, recording the I-V characteristics (Figure 4.2e). The current evolution as a function of pressure exhibits a hysteretic behaviour, as shown in Figure 4.2f. The two curves diverge significantly in the transition region (by approximately 60 µA), only converging at the boundary pressures (10^{-4} and 10^3 mbar). This lag is a direct consequence of the different time scales associated with the adsorption and desorption kinetics of gas molecules on the $PdSe_2$ surface; the complete removal of molecules in vacuum is a slower and thermally activated process with respect to the adsorption process at ambient pressure.[168]

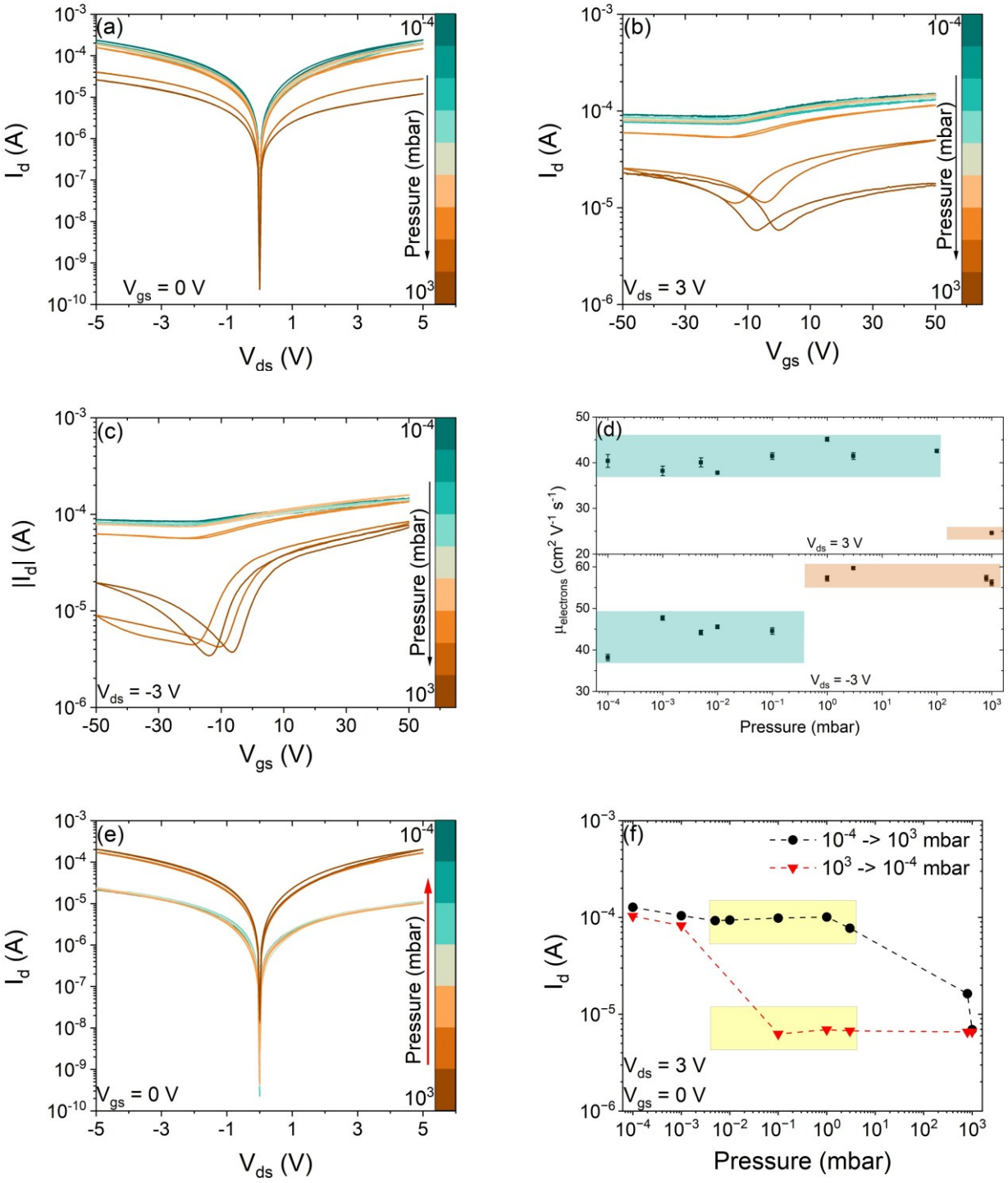


Figure 4.2: Electrical characterization of the $PdSe_2$ FET under different pressure conditions. (a) I-V characteristics of the $PdSe_2$ FET at V_{gs} = 0 V from high vacuum (10^{-4} mbar) to ambient pressure (10^3 mbar). (b-c) Transfer characteristics of the $PdSe_2$ FET with V_{ds} = ± 3 V from high vacuum to ambient pressure. (d) Electron mobility as a function of the pressure at V_{ds} = 3 V (top graph) and V_{ds} = -3 V (bottom graph). (e) I-V characteristics of the $PdSe_2$ device at V_{gs} = 0 V from ambient pressure (10^3 mbar) to high vacuum (10^{-4} mbar). (f) Drain current at V_{ds} = 3 V as a function of the pressure, extracted from the cycles, from ambient pressure to high vacuum and viceversa.

To further investigate the transport mechanisms, transfer characteristics were recorded across a wide range of V_{ds}, from 0.01 to 3 V, under different pressure regimes. The analysis reveals that the

conduction polarity is not only a function of V_{gs} but is also strongly influenced by the contact-channel interface.

In high vacuum (10^{-4} mbar), the device exhibits predominantly n-type conduction with a high degree of symmetry between the positive and negative V_{ds} values (Figure 4.3a). The overlap of these curves suggests that in a clean ambient, the Schottky barriers at the source and drain electrodes are relatively uniform and low enough to allow efficient electron injection from both sides of the channel. In contrast, as the pressure increase to 2 mbar (Figure 4.3b) and 10^3 mbar (Figure 4.3c), a significant asymmetry emerges between the positive and negative V_{ds} regimes. At low bias (V_{ds} = ±10 mV), the curves remain symmetric and ambipolar, reflecting the intrinsic state of the channel. At high positive bias V_{ds} (between 0.5 and 3 V), the device is dominated by p-type conduction, whereas at negative high bias, the device exhibits ambipolar conduction but with a dominant n-type branch. This pressure-dependent asymmetry is attributed to the Schottky barrier (SB) modulation at the metal-semiconductor interfaces. In this device, the $PdSe_2$ flake is transferred onto the prepatterned metal contacts. This architecture is particularly susceptible to the trapping of atmospheric species at the interface between the metal and the 2D material. At ambient pressure, these adsorbates act as local p-dopants and interfacial dipoles that modify the SB height and width. The observed asymmetry indicates that these adsorption processes do not occur uniformly at both contacts, leading to asymmetric Schottky barriers. When V_{ds} is positive, the bottleneck for carrier injection is the contact with the higher barrier for electrons, effectively suppressing the n-type branch and favouring p-type transport. When the bias is reversed (negative V_{ds}), the other contact becomes the primary injector, allowing for a more balanced ambipolar or n-dominated transport. To confirm that this behaviour originates from the contacts rather than the $PdSe_2$ channel itself, the source and drain electrodes were interchanged. As shown in Figure 4.3d, the transfer characteristics overlap when the roles of the electrodes are swapped, confirming that the current is limited by the specific barrier properties of the individual metal-semiconductor junctions. The blue transfer curves represent the first configuration, while the red ones indicate the second configuration. In high vacuum, the removal of these adsorbates restores a more uniform, lower-resistance contact, leading back to the symmetric n-type characteristics observed in Figure 4.3a.

As stated previously, the emergence of hysteretic behaviour in the transfer curves is attributed to the capture and release of charge carriers by localized trap states. To quantify this effect, the hysteresis width can be defined as the gate voltage difference between the forward and reverse sweeps of transfer characteristics. Specifically, as illustrated in Figure 4.3e, $H_w = V_2 - V_1$, where V_1 and V_2 represent the gate voltages at the intersection point of the p- and n-type branches for the two seep directions. The hysteresis width is remarkably sensitive to the environmental pressure but remains largely independent of V_{ds}. At low vacuum of 2 mbar, the H_w is approximately 10 V. In contrast, at ambient pressure (10^3 mbar), the H_w increases sixfold to approximately 62 V. This trend confirms that environmental adsorbates are the dominant contributors to the trapping density, and their removal in vacuum restores a near-ideal, non-hysteretic transport regime. To decouple the effects of total pressure from the chemical nature of the species, we performed controlled gas-injection experiments. Starting from a high-vacuum baseline, the chamber was purged with either Ar, an inert gas, and O_2. As demonstrated in Figure 4.3f, the introduction of Ar does not significantly alter the electrical profile of the device. Aside from minor variation in the absolute current level, likely due to the mechanical displacement of residual molecules, the characteristic n-type

conduction of $PdSe_2$ remains intact. This confirms that Ar does not engage in charge transfer with the $PdSe_2$ surface. Conversely, the introduction of O_2 triggers a dramatic transition to ambipolar conduction with a prominent p-type branch. This confirms that O_2 molecules act as active surface dopants. Upon adsorption, O_2 withdraws electrons from the $PdSe_2$ channel, effectively creating holes and shifting the device's operation into the p-type regime. This gas-selective response highlights the potential of $PdSe_2$ as a sensitive platform for molecular detection, while simultaneously underlining the necessity of vacuum or encapsulation for stable, n-type operation in logic applications.

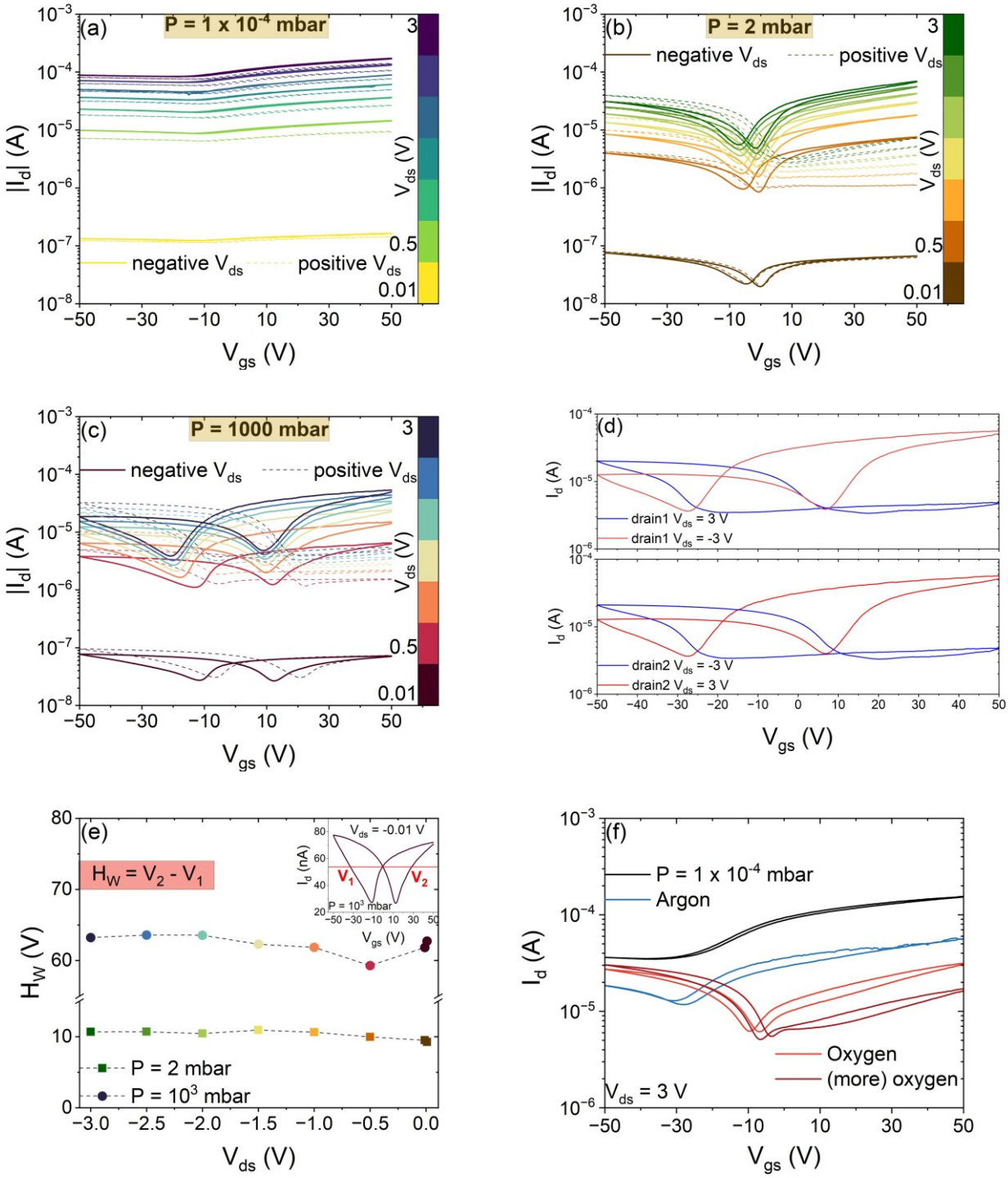


Figure 4.3: Transfer characteristics of the $PdSe_2$ device at negative (solid line) and positive (dashed line) bias in (a) high vacuum (10^{-4} mbar), (b) low vacuum (2 mbar), and (c) ambient pressure (10^3 mbar). (d) Transfer characteristics of the $PdSe_2$ device at V_{ds} = ±3 V interchanging the source and drain electrodes. (e) Hysteresis width of the transfer curves in low vacuum at 2 mbar (coloured squares) and at ambient pressure (coloured circles) as a function of V_{ds}. (in the inset: transfer cuver at V_{ds} = -0.01 V at ambient pressure with the definition of the hysteresis width of the transfer curve). (f) Transfer curves under different gas environments with V_{ds} = 3 V.

To conduct a systematic evaluation of the environmental sensitivity, Figure 4.4 presents a side-by-side comparison of the device's transport characteristics under reactive and inert atmospheres. Figure 4.4a-b display the output curves and the transfer characteristics, respectively, of the $PdSe_2$ FET when exposed to an O_2 environment. For comparison, Figure 4.4c-d show the corresponding electrical characterization performed under a chemically inert Ar atmosphere. This comparative study is essential to isolate the role of surface-mediated charge transfer from purely pressure-related effects, establishing the O_2 molecules as the primary drivers of the observed p-type doping.[169,170]

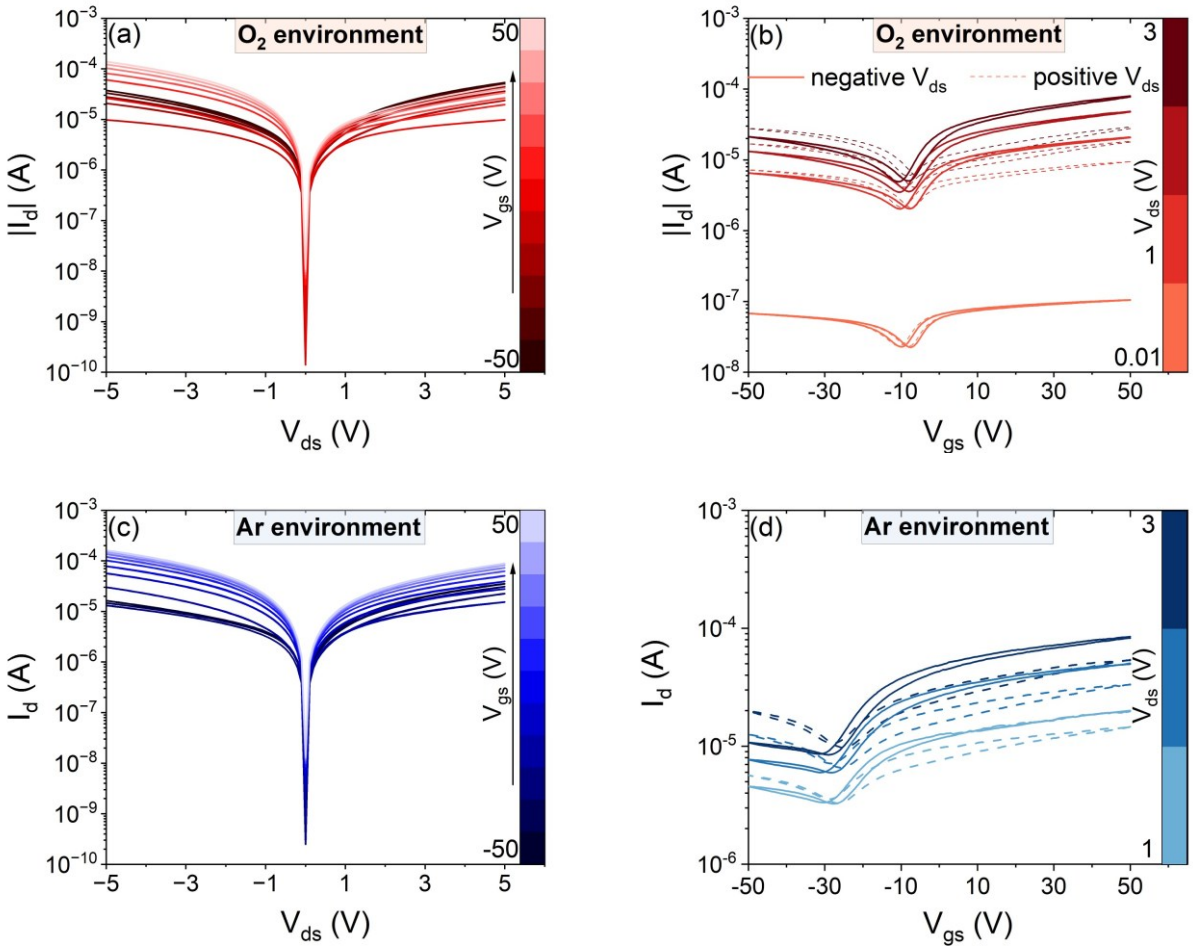


Figure 4.4: (a) Output and (b) transfer characteristics of the $PdSe_2$ device in an O_2 environment. (c) Output and (d) transfer characteristics of the $PdSe_2$ device in an Ar environment.

4.1.2 Low-temperature optoelectronic characterization

The optoelectronic properties of the $PdSe_2$ device were initially evaluated at room temperature; however, no significant photoresponse was detected. This lack of sensitivity under ambient conditions is likely due to high thermal noise and the prevalence of fast recombination centers that dominate the carrier dynamics at 300 K. To overcome these limitations, the device was cooled to 77 K in high vacuum (10^{-5} mbar).

Figure 4.5a presents the output characteristics of the $PdSe_2$ device at 77 K. Notably, the current magnitude is approximately one order of magnitude lower than that observed at room temperature. This reduction is a direct consequence of the suppression of thermionic emission over the Schottky barriers at the contacts and the freezing out of thermally activated hopping transport through trap

states. The device retains n-type conduction for $V_{gs} > -10$ V, while a transition in the transport regime is observed at deeper negative biases. The transfer characteristics (Figure 4.5b) reveal an intriguing evolution of the channel conduction. At high positive bias ($V_{ds} = 3$ V), the device is predominantly n-type but exhibits a distinct conductance valley with $-30 \text{ V} < V_{gs} < -15$ V. This feature becomes significantly more pronounced at negative V_{ds}, where the device displays asymmetric ambipolar-like behaviour. At 77 K, we observe a significant discrepancy in the extracted field-effect mobility: it is about (81.9 ± 0.9) $cm^2 V^{-1} s^{-1}$ at $V_{ds} = 3$ V, dropping to (39.8 ± 0.2) $cm^2 V^{-1} s^{-1}$ at $V_{ds} = -3$ V. This asymmetry can be attributed to the inhomogeneity of the Schottky barriers at the source and drain interfaces. At cryogenic temperatures, the tunnelling probability becomes highly sensitive to the local electric field and the specific height of the barrier.[61] The lower mobility at negative V_{ds} indicates that one of the contacts acts as a more significant bottleneck for electron injection, likely due to a higher local concentration of trapped interfacial charges or structural imperfections at that specific metal-semiconductor junction.

The device demonstrates a clear response to optical stimulation at 77 K. Figure 4.5c shows the I-V characteristics under dark conditions and varying optical power of the laser. The current increases monotonically with incident power (P_{inc}), ranging from 68 to 340 µW. A slight offset in the dark current compared to previous output scans was observed, which can be attributed to gate-bias stress effects or persistent charges from prior sweeps.

Since the photoresponse is more pronounced at $V_{ds} = -3$ V, where the contact barrier likely facilitates more efficient separation of photogenerated pairs, the transfer curves under illumination were recorded at this bias (Figure 4.5d). The $PdSe_2$ device maintains its n-type profile, with the conductance scaling with light intensity. The time-resolved measurements (inset of Figure 4.5e) further confirm the stability and reversibility of photo-switching behaviour of $PdSe_2$ at low temperature. The photocurrent follows the characteristic power law $I_{ph} \approx P_{inc}^{\alpha}$. As shown in Figure 4.5e-f, the extracted exponent is $\alpha = 0.37 \pm 0.02$. In 2D materials, an exponent of $\alpha = 1$ indicates ideal electron-hole pairs photogeneration, separation and collection, whereas $\alpha < 1$ indicates the presence of a complex recombination mechanism involving a high density of localized trap states within the bandgap. An exponent as low as 0.37 suggests that the photocurrent is limited by the filling and emptying of these trap levels, which is consistent with the significant selenium vacancies

previously identified in the $PdSe_2$ structure. Trap states reduce the photocarrier generation rate and lower their collection efficiency by capturing carriers and favouring their recombination.

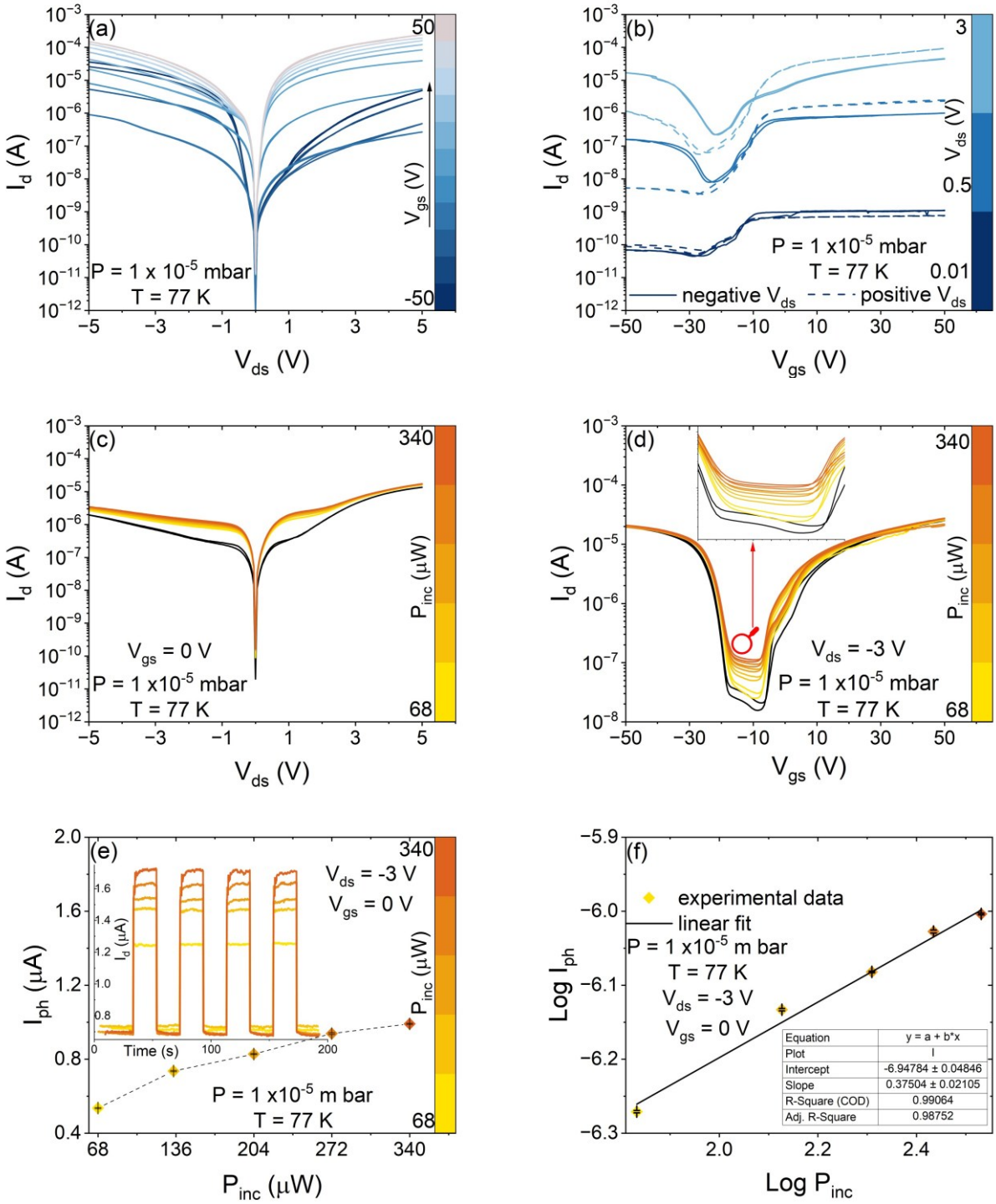


Figure 4.5: (a) Output and (b) transfer characteristics at different V_{ds} in high vacuum at low temperature (77 K). (c) I-V characteristics at V_{gs} = 0 V and (d) transfer curves at V_{ds} = -3 V in high vacuum at 77 K under dark and white light at different powers. (e) Photocurrent as a function of incident optical power at V_{ds} = -3 and V_{gs} = 0 V in high vacuum at 77 K (in the inset: light pulses of 20 s at different incident laser powers). (f) Photocurrent vs incident power in logscale with exponential fit for the estimation of the exponent law α.

The wavelength-dependent photoresponse of the $PdSe_2$ device at 77 K is shown in Figure 4.6a, showing the responsivity of the device as a function of the wavelength in the 530-900 nm range. A prominent peak in the responsivity is observed at approximately 830 nm (≈1.5 eV). At first glance, this energy significantly exceeds the fundamental indirect bandgap of multilayer $PdSe_2$, which approaches 0.1 eV in the bulk limit. However, the presence of this peak can be justified by considering the quasiparticle band structure and the selection rules governing optical transitions.

In 2D TMDs, the photoresponse does not necessarily track the minimum indirect bandgap. Instead, it is dominated by direct optical transitions at k-points where the valence and conduction bands are nearly parallel. At these points, the joint density of states exhibits a Van Hove singularity, leading to a sharp increase in the absorption coefficient and, consequently, a peak in the photocurrent. Referring to first-principles GW calculations by Kim at al.[51], the band structure of monolayer $PdSe_2$ reveals several regions along the high-symmetry lines where the energy separation between the highest valence bands and higher-order conduction bands is approximately 1.5 - 1.6 eV. In these regions, the bands maintain a remarkably parallel curvature over a significant portion of the Brillouin zone. This alignment ensures a high probability of photon absorption, as a large number of states are available for transitions at that specific energy. However, in our device the $PdSe_2$ flake is not a monolayer.

The clarity of this 1.5 eV peak at 77 K can be further enhanced by excitonic effects. Even in multilayer systems, the reduced screening in the 2D limit can lead to the formation of excitons with significant binding energies. At cryogenic temperatures, the thermal energy is insufficient to dissociate these excitons, allowing for the observation of sharp excitonic resonances that would otherwise be broadened or quenched by phonon scattering at room temperature. The peak at 830 nm thus may represent a feature of a direct transition between parallel bands, likely enhanced by an excitonic resonance (see Figure 4.6b). This suggests that while $PdSe_2$ is a narrow-gap semiconductor in terms of its transport properties, its optoelectronic signature is defined by high-energy transitions that provide efficient light-harvesting capabilities in the near-infrared and visible spectrum.[171,172] The temperature-dependent optical characterization of $PdSe_2$ reveals a significant redshift of the central peak energy as the temperature increases. This trend is primarily attributed to the intensification of electron-phonon interactions and thermal expansion of the crystal lattice at higher temperatures. Conversely, as the temperature is reduced, the $PdSe_2$ bandgap exhibits a clear increase, manifesting as a blueshift in the emission spectrum (Figure 4.6c).

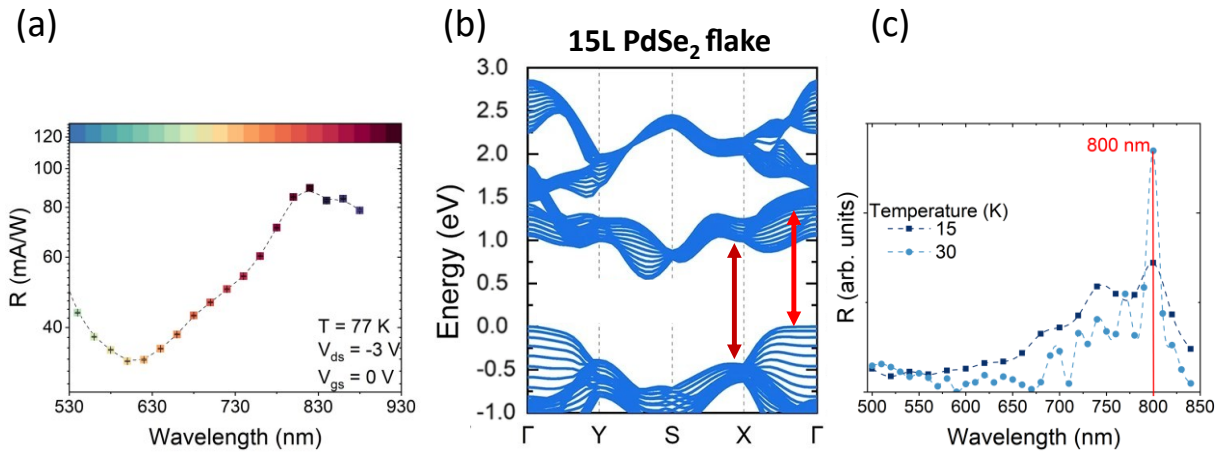


Figure 4.6: (a) Wavelength-dependent responsivity of the $PdSe_2$ device at 77 K. (b) DFT calculated energy band structure of $PdSe_2$ with a red arrow to indicate a possible band transition with an energy of approximately 1.5 eV. Adapted from [173]. (c) Wavelength-dependent responsivity of the $PdSe_2$ device at 15 K and 30 K.

4.2 Tungsten disulphide FETs

Since we have established a comprehensive baseline for the electronic and optoelectronic properties of $PdSe_2$, this section focuses on the second constituent for our $WS_2/PdSe_2$ heterostructures: WS_2. Unlike the relatively new and structurally exotic $PdSe_2$, WS_2 is a widely studied, prototypical TMD characterized by a hexagonal lattice and robust electronic properties. While $PdSe_2$ provides a stable electronic foundation, the high optical quantum yield of WS_2 makes it a synergistic partner for the vertical vdW $WS_2/PdSe_2$ heterostructures discussed later in this chapter.

Figure 4.7a shows the optical image of a WS_2 flake onto Si/SiO_2 (290 nm oxide thickness) prepatterned substrate, following the procedure detailed in Section 2.1.2. The uniform contrast suggests a high-quality monolayer flake, which is confirmed by the Raman spectrum in Figure 4.7b. This spectrum displays the two characteristic first-order Raman modes of WS_2: the $E_{2g}{}^1$ mode (in-plane vibration) at 350 cm^{-1} and the A_{1g} mode (out-of-plane vibration) at 417 cm^{-1}. The frequency difference between these two peaks and their relative intensities are consistent with monolayer WS_2 of high crystalline purity, showing no signs of oxidation or structural defects.[174–176]

The electrical transport of the WS_2 FET was evaluated in both ambient pressure (Figure 4.7c) and high vacuum (Figure 4.7d). The device exhibits n-type conduction, with the current increasing as the gate voltage is swept toward positive values. The transfer characteristics recorded at ambient pressure show a noticeable hysteresis width, which approaches 30 V at $I_d \approx 10^{-11}$ A at V_{ds} = 5 V, and a reduction in the on current when exposed to air. This is due to the adsorption of O_2 and H_2O molecules, which act as electron traps and increase the scattering rate at the WS_2 surface. As it can be observed in Figure 4.7d, under vacuum conditions, the hysteresis width is significantly reduced, indicating that the trapping states are largely extrinsic rather than intrinsic defects. Moreover, the drain current increases by approximately four orders of magnitude under vacuum conditions, as the removal of oxygen species reduces the depletion of the n-type channel. However, it remains strictly n-type across all the pressure regimes.

The field-effect mobility in WS_2 is around 0.01 $cm^2\ V^{-1}\ s^{-1}$ and becomes 5.00 $cm^2\ V^{-1}\ s^{-1}$ in high vacuum.

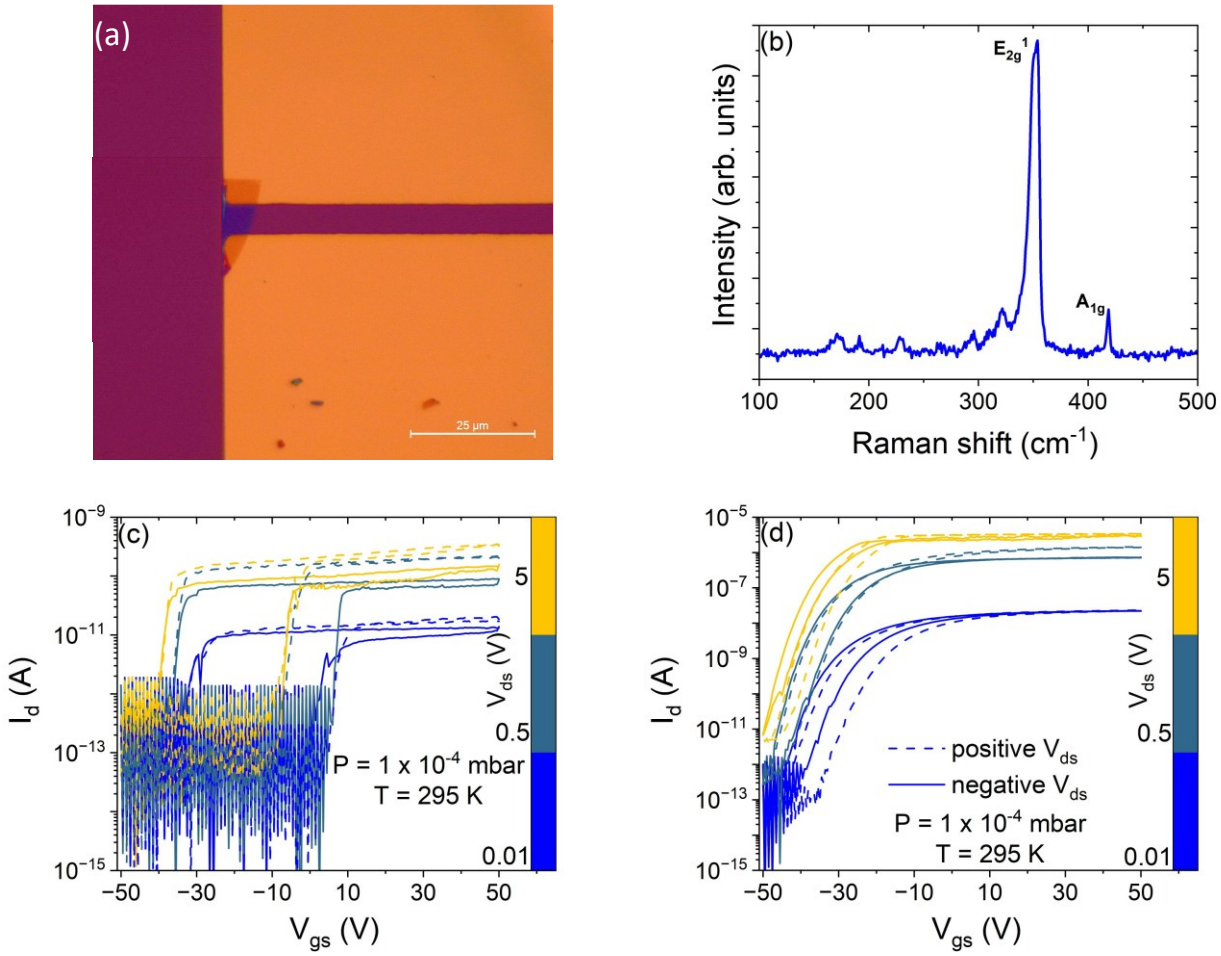


Figure 4.7: (a) Optical image of a WS_2 FET. (b) Raman spectrum of the WS_2 flake. Transfer characteristics of the WS_2 FET (c) at ambient pressure and (d) high vacuum at a pressure of 10^{-4} mbar at different V_{ds}.

4.2.2 Pressure-dependent optoelectronic characterization

The optoelectronic performance of the WS_2 FET was evaluated to establish a baseline for the $WS_2/PdSe_2$ heterostructure at room temperature. Time-resolved photocurrent measurements under white light illumination at different incident optical powers, from 33 to 163 µW, were performed both at ambient pressure and in high vacuum at a pressure of 10^{-4} mbar, as shown in Figure 4.8a-c. The relationship between the photocurrent and the incident light power provides insights into the recombination mechanisms. This relationship typically follows a power law, $I_{ph} \propto P_{inc}^{\alpha}$. At ambient pressure, the exponent α is found to be 0.85 ± 0.04 (Figure 4.8b). This sublinear value indicates a recombination process dominated by a distribution of trap states within the bandgap, primarily due to sulphur vacancies and surface adsorbates. Interestingly, in high vacuum the power law exponent α decreases further to 0.45 ± 0.03 (Figure 4.8d). This more pronounced sublinear regime in vacuum suggests that while current level increases due to the desorption of molecules, the intrinsic defect-mediated recombination becomes the dominant factor limiting the photoresponse efficiency.

To gain further insight into the photophysical mechanisms and recombination kinetics of the WS_2 device, the temporal photoresponse was analysed through multi-exponential fitting of the current

transients. This approach allows for the decoupling of different physical processes governing the generation and relaxation of charge carriers.

All the pulses acquired at ambient pressure were correctly fitted with a double exponential function, $I_d = I_0 + A_1 e^{-\frac{t}{\tau_1}} + A_2 e^{-\frac{t}{\tau_2}}$, both for the rise and decay part, as depicted for the pulse at 98 μW, as an example (Figure 4.8a, black and red lines). The extracted τ_1 and τ_2 time constants, reported in Figure 4.8e, are on the order of the 1 s (10 s) and 40 s (100 s), respectively, for the rise (decay) branch of the acquired light pulses at V_{ds} = 0.5 V at ambient pressure. The rise branch of the pulses in high vacuum was correctly fitted with a double exponential fit (Figure 4.8c, black line) with τ_1 on the order of 1 s, whereas the decay branch was fitted with a single exponential fit (Figure 4.8c, red line) with τ_1 between 35 and 80 s (Figure 4.8f).

While the WS_2 FET provides a clear understanding of the material's main properties and intrinsic limits, this characterization is intended primarily as a comparative baseline. Further detailed analysis of the optoelectronic mechanisms is deferred to the following section, where the $WS_2/PdSe_2$ heterostructure is discussed.

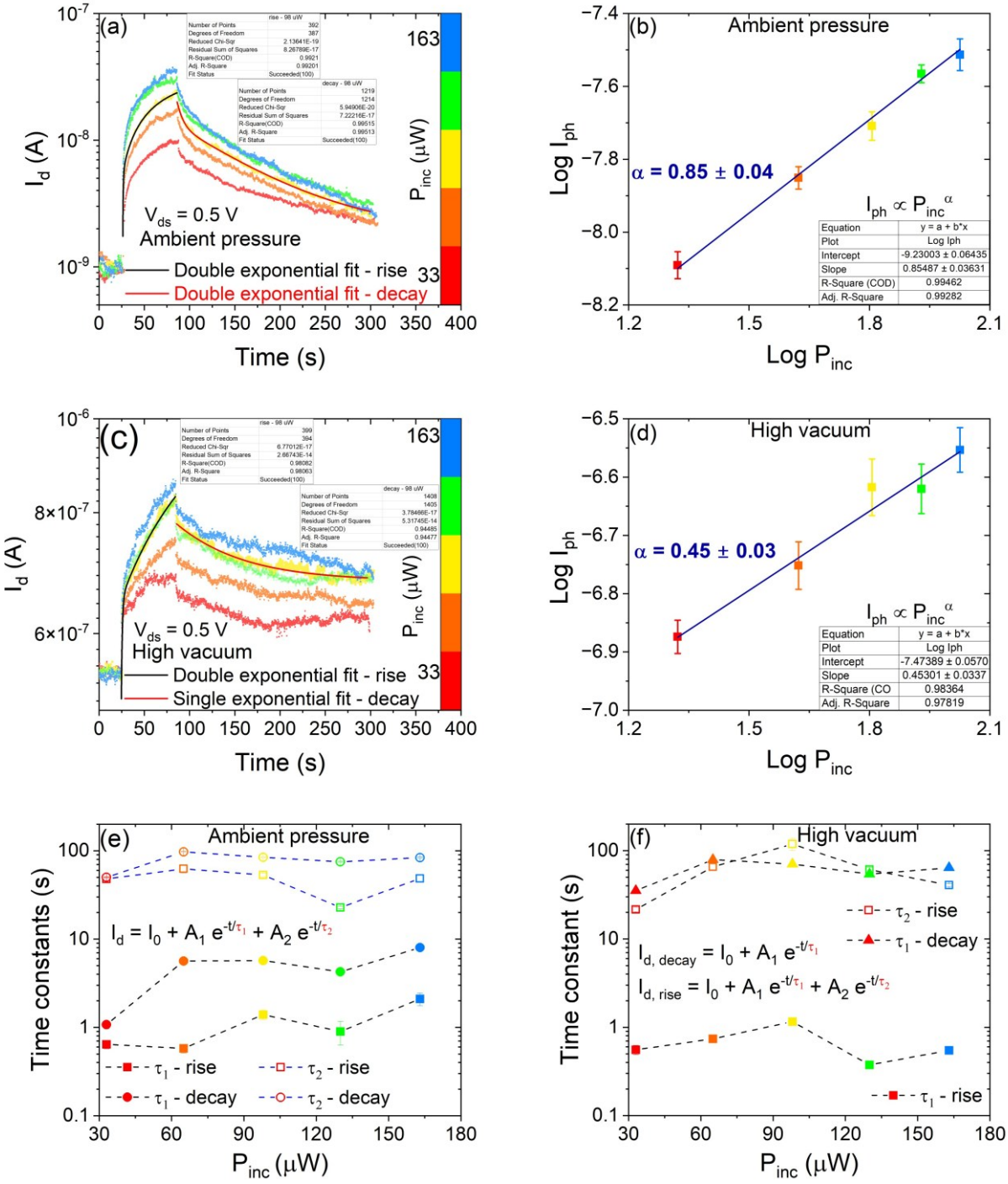


Figure 4.8: Time-resolved measurements of single WS_2 FETs under white light illumination. 60 s long pulses at different incident laser powers, from 33 (red points) to 163 (blue points) μW at (a) ambient pressure and in (c) high vacuum at a pressure of 10^{-4} mbar at V_{ds} = 0.5 V. Exponential fits of the rise (black line) and decay branch (red line) of the light pulses at an incident laser power of 98 μW. Time constants τ_1 and/or τ_2 from a double or single exponential fit of the time-resolved pulses at (b) ambient pressure and in (d) high vacuum at a pressure of 10^{-4} mbar.

4.3 $WS_2/PdSe_2$ vdW heterostructures

Following the baseline characterization of the individual WS_2 and $PdSe_2$ constituents, this section presents a systematic investigation into the electrical and optoelectronic properties of the vertical

$WS_2/PdSe_2$ vdW heterostructure. Building upon the fabrication methodology detailed in Section 2.1.2, we explore how the coupling of these two stable semiconductors results in a material platform with enhanced environmental sensitivity, optoelectronic and memory-like functionalities.

The study examines the interfacial charge transport as a function of environmental pressure, demonstrating the device's potential as a high-sensitivity pressure-modulated sensor. We then transition to the optoelectronic evaluation of the $WS_2/PdSe_2$ heterojunction under visible light, focusing on the interplay between photogeneration and the intrinsic trap-mediated dynamics. An important portion of this analysis is dedicated to the study of persistent photoconductivity, where the charge trapping kinetics at the $WS_2/PdSe_2$ interface are decoupled to understand the long-lived carrier states. Finally, by exploiting these trapping mechanisms, we demonstrate the transition from a traditional photodetector to an optoelectronic synaptic device, showcasing the heterostructure's ability to mimic biological plasticity for neuromorphic applications.

4.3.1 Materials characterization

Figure 4.9a shows an optical image of a $WS_2/PdSe_2$ heterostructure fabricated following the procedure described in Section 2.1.2. Multiple profiles were extracted from the AFM images of the two flakes to estimate the thickness of the two flakes. The WS_2 and $PdSe_2$ height profiles are presented in Figure 4.9b, showing a thickness of 2.5 nm for WS_2 and 16 nm for $PdSe_2$. Despite the WS_2 thickness differing from the nominal 0.6 nm of a single layer of WS_2[128], the monolayer nature of the WS_2 flake is also confirmed by the differential reflectance spectrum, measured while on the PDMS stamp, as shown in Figure 4.9c.[177,178] Raman spectra of the single materials and the heterojunction were acquired under laser excitation of 532 nm and are reported in Figure 4.9d. The violet line corresponds to the Raman spectrum from $WS_2/PdSe_2$ overlapping region. Peaks at around 350 cm^{-1} and 417 cm^{-1} correspond to the in-plane optical mode E_{2g}^1 of WS_2 and out-of-plane vibrations, A_{1g}, of sulphur atoms, respectively. The position of these two peaks confirms that the WS_2 flake is a monolayer.[174–176] Peaks at 140 cm^{-1}, 203 cm^{-1}, 219 cm^{-1}, and 255 cm^{-1} are associated to A_g^1, A_g^2, B_{1g}^2, and A_g^3 modes of $PdSe_2$, respectively. The position of peaks confirm the multilayer structure of the $PdSe_2$ flake.[154–156] Since the $PdSe_2$ multilayers absorb part of the excitation power and Raman signal, the WS_2 signal in the overlapped part of the heterojunction is weaker than the pure WS_2.[179] The Raman spectra confirm the formation of the heterojunction, and the high quality of the single flakes and the overlapped region at the interface. The PL spectra of the $WS_2/PdSe_2$ heterojunction (violet line) and the single WS_2 flake (blue line) at room temperature and ambient pressure are displayed in Figure 4.9e. The absent PL intensity of $PdSe_2$ is due to its indirect bandgap. There is a notable PL quenching in the area of overlap between WS_2 and $PdSe_2$. Because of exciton dissociation and charge transfer at the heterojunction interface, the PL peak intensity in this region is lower than that of the single WS_2 flake. Additionally, the laser penetrating the $PdSe_2$ sheets loses part of its energy, contributing to the decrease in the final PL peak intensity of WS_2.

Figure 4.9f displays a schematic of a device under examination, showing that $PdSe_2$ side serves as the source, while the WS_2 part acts as the drain. The highly doped Si substrate, covered by conductive silver paste, constitutes the back-gate electrode.

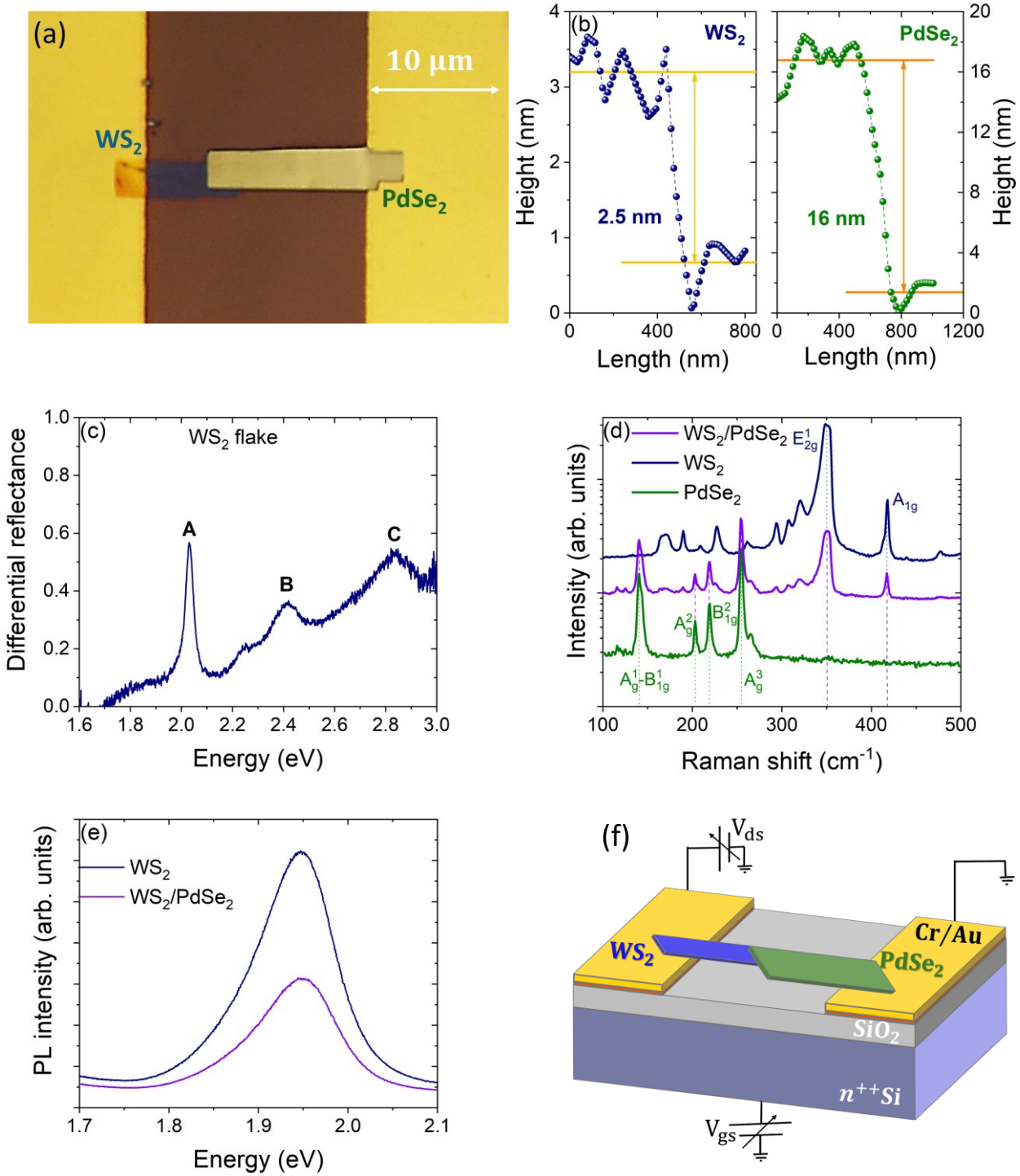


Figure 4.9: (a) Optical image of a $WS_2/PdSe_2$ heterostructure. (b) AFM profiles of the WS_2 (left graph) and $PdSe_2$ (right graph) flakes. (c) Differential reflectance spectrum of the WS_2 flake, highlighting its monolayer nature. (d) Raman spectra of the $WS_2/PdSe_2$ heterojunction (violet line), single WS_2 (blue line) and $PdSe_2$ (green line) flakes. (e) PL spectra of the WS_2 (blue line) and $WS_2/PdSe_2$ (violet line) heterojunction at ambient pressure and temperature. (f) Schematic of a $WS_2/PdSe_2$ heterostructure and measurement setup.

4.3.2 Pressure dependent electrical characterization

This section presents a critical analysis of the $WS_2/PdSe_2$ heterostructure's electrical response in dark under varying environmental pressures. The comparison between the device performance in

ambient conditions and high vacuum allows for decoupling the intrinsic transport properties of the $WS_2/PdSe_2$ heterostructure from the extrinsic effects of surface adsorbates.

The electrical behaviour of the $WS_2/PdSe_2$ heterostructure was monitored across a complete cycle of pressure modulation, from high vacuum (10^{-4} mbar) to ambient pressure (10^3 mbar), denoted by states n = 1 through n = 5. The states represent the progression from the initial ambient state (n = 1), through high vacuum (n = 3), and back to ambient conditions (n = 5).

Figure 4.10a illustrates the I-V characteristics of the $WS_2/PdSe_2$ heterostructure with a grounded gate. The solid blue curve reproduces the electrical behaviour of the device at ambient pressure, n = 1. As the pressure decreases to 10^{-4} mbar, O_2 and H_2O molecules desorb from the surface of the materials, leading to a significant increase in current, surpassing 1 µA at V_{ds} = ±10 V. Additionally, the I-V characteristic becomes less asymmetric (solid green curve), with the current ratio ($I_{d,-10V}/I_{d,10V}$) evolving from 200 at ambient pressure to 4 in high vacuum. Notably, the I-V characteristic goes back to its initial configuration (dashed blue curve) once the chamber returns to ambient pressure. This behaviour underscores the pronounced sensitivity of the $WS_2/PdSe_2$ heterostructure to adsorbed species.

Figure 4.10b displays the transfer curves at a fixed V_{ds} = 5 V, for different system states. These states not only include n = 1, 3, 5 (as described previously), but also n = 2 (dotted green curve), which corresponds to high vacuum at 10^{-4} mbar before complete desorption, and n = 4 (dotted blue curve), which corresponds to ambient pressure before complete adsorption. The transfer curves in all the states present typical n-type conduction. The hysteresis width of the transfer curves, defined as the maximum gate voltage difference between the two branches of the curve (Figure 4.10c), evolves gradually across the states from n = 1 to n = 5. It decreases from 70 V at ambient pressure (n = 1) to 15 V at a pressure of 10^{-4} mbar (n = 3), as depicted in Figure 4.10d (purple dots). This hysteresis width arises primarily from charge trapping at the interface between SiO_2 and the semiconductor materials, as well as residuals from fabrication processes. Indeed, H_2O molecules could contribute to the transfer of electrons from the trap states and/or provide extra traps by weaking some bonds in the top SiO_2 layers.[119,180,181] The dramatic reduction (over 50%) in hysteresis width from n = 1 to n = 3 highlights the dominant role of adsorbates, whose adsorption at selenium and sulphur vacancy sites is favoured especially at positive V_{gs}. The on/off current ratio, defined as the ratio between the maximum and minimum current of the transfer curves at different states (Figure 4.10c), ranges between 10^7 and 10^8 (Figure 4.10d, yellow dots), showcasing a promising characteristic for electronic device applications. The lowest value of the on/off current ratio is observed in high vacuum (n = 3), attributed to the leftward shift of the transfer curve caused by O_2 desorption. The achieved values are at least four orders of magnitude higher than the ones reported in the literature for similar devices.[182] Notably, the $WS_2/PdSe_2$ heterostructure exhibits n-type conduction with a significantly enhanced on/off current ratio compared to individual WS_2 and $PdSe_2$ devices. This is particularly advantageous for electronics applications: the $WS_2/PdSe_2$ heterostructure shows a clear distinction between the on and off states, unlike the $PdSe_2$ device, which shows ambipolar behaviour, making it more challenging to achieve sharp switching characteristics. Thus, while WS_2 layer ensures a robust n-type transport and superior gate control with high on/off current ratios, the high environmental sensitivity of the $WS_2/PdSe_2$ heterostructure, manifested in the significant modulation of current and hysteresis, is fundamentally driven by the $PdSe_2$ layer and its high affinity for surface adsorbates.

Figure 4.10e shows the transfer curves of the $WS_2/PdSe_2$ heterostructure at ambient pressure for different V_{ds}, ranging from -5 to 5 V, while sweeping the V_{gs} from 50 to -50 V, and back to 50 V. Similarly, Figure 4.10f presents the transfer curves at different V_{ds} (from -5 to 5 V) under a high vacuum at a pressure of 10^{-4} mbar. At ambient pressure, the transfer curves for positive and negative V_{ds} exhibit noticeable differences due to the significant asymmetry in the I-V characteristics. In contrast, under high vacuum, the sets of transfer curves with V_{ds} ranging from 0 to 5 V and from 0 to -5 V appear much more similar, reflecting the symmetrisation of the I-V characteristics.

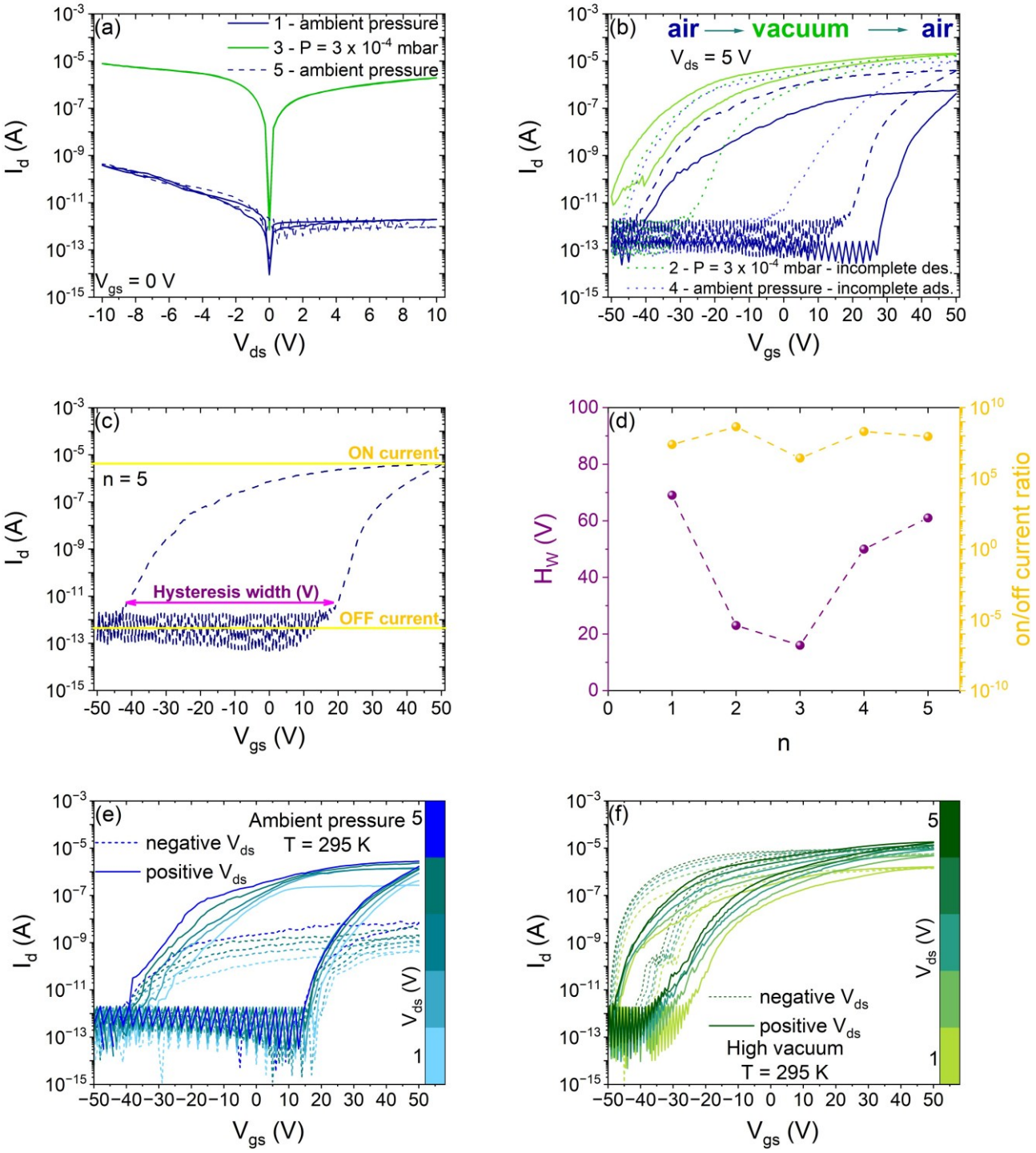


Figure 4.10: (a) I-V characteristic of the $WS_2/PdSe_2$ heterostructure at ambient pressure (solid blue line, n = 1), high vacuum at a pressure of 10^{-4} mbar (solid green line, n = 3), and ambient pressure again (dashed blue line, n = 5) with a grounded gate. (b) Transfer curves of the $WS_2/PdSe_2$ heterostructure at a fixed V_{ds} = 5 V in different states: at ambient pressure (solid blue line, n = 1), high vacuum before complete desorption of molecules from the materials surface (dotted green line, n = 2), high vacuum at a pressure of 10^{-4} mbar (solid green line, n = 3), ambient pressure soon after switching off the pumping system before complete adsorption (dotted blue line, n = 4), and ambient pressure (dashed blue line, n = 5). (c) Transfer curve at n = 5 with the on and off current states indicated in yellow, and the hysteresis width of the transfer curve marked with a magenta line. (d) Evolution of the hysteresis width of the transfer curve (purple dots, left axis) and on/off current ratio (yellow dots, right axis) across the states from n = 1 to n = 5. Transfer curves of the $WS_2/PdSe_2$

heterostructure with V_{ds} ranging from -5 to 5 V at (e) ambient pressure and in (f) high vacuum at a pressure of 10^{-4} mbar.

4.3.3 Optoelectronic characterization (white light)

The integration of the wide-bandgap WS_2 with the narrow-bandgap $PdSe_2$ creates a broadband material platform capable of efficient photon harvesting. To evaluate this, the heterostructure was characterized under white light illumination with varying P_{inc} in both ambient pressure and high vacuum.

To account for the asymmetric I-V characteristics observed at ambient pressure, laser pulses lasting 60 s were acquired at V_{ds} = ±5 V. Figure 4.11a depicts the pulses at ambient pressure at V_{ds} = -5 V (top) and V_{ds} = 5 V (bottom) at increasing $P_{inc,}$ from 48 to 241 µW, with the gate grounded. The photocurrent depends on the incident laser power and follows a power law $I_{ph} \propto P_{inc}^{\alpha}$. The power law exponent α is 0.88 ± 0.06 at V_{ds} = -5 V and 0.71 ± 0.07 at V_{ds} = 5 V (Figure 4.11b), consistently with what reported in the literature.[182] This sublinear relationship between I_{ph} and P_{inc} can be attributed to intricate mechanisms of photo-generated carriers during generation, trapping, and recombination processes.[183] Figure 4.11c shows time-dependent pulses measured in high vacuum at a pressure of 10^{-4} mbar for V_{ds} = -5 V (top) and V_{ds} = 5 V (bottom). As previously mentioned, the I-V characteristic becomes more symmetric as the pressure decreases, leading to photocurrent values at negative and positive voltage biases falling within the same range, (0.5 - 1.2) µA. In Figure 4.11d, the dependence of the photocurrent on the incident laser power continues to follow a power law, with α equal to 0.49 ± 0.08 at V_{ds} = -5 V and 0.55 ± 0.07 at V_{ds} = 5 V. The smaller values of α indicate a more pronounced sublinear regime in high vacuum.[93] The extracted power-law exponents α for the $WS_2/PdSe_2$ heterostructure are remarkably consistent with those obtained for individual WS_2 devices under similar experimental conditions, as described in Section 4.2.2. Specifically, the evolution from a nearly linear regime in ambient pressure to a more pronounced sublinear behaviour in high vacuum closely mirrors the response of pristine WS_2 flakes. This similarity in the α values provides quantitative evidence that the overall optoelectronic behaviour and the associated carrier dynamics of the heterostructure are dominated by the WS_2 layer.

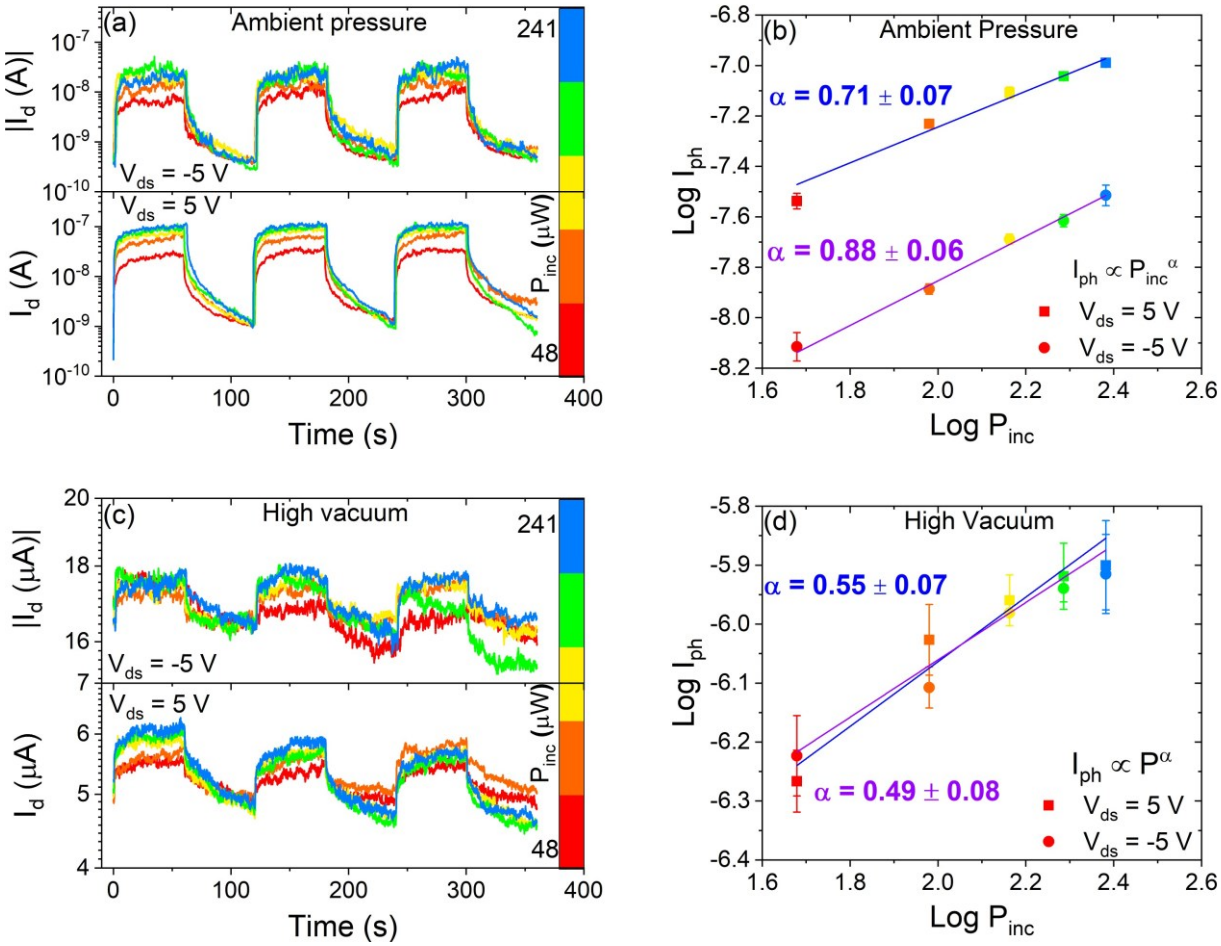


Figure 4.11: Time-resolved measurements of the $WS_2/PdSe_2$ heterostructure under white light illumination. 60 s long pulses at different incident laser powers at (a) ambient pressure and (c) high vacuum at a pressure of 10^{-4} mbar at V_{ds} = -5 V (top) and V_{ds} = 5 V (bottom). Photocurrent as a function of the incident laser power on a logscale at (b) ambient pressure and (d) high vacuum at a pressure of 10^{-4} mbar at V_{ds} = -5 V (coloured circles) and V_{ds} = 5 V (coloured squared). The power law exponent α is extracted from the linear fit of experimental data at V_{ds} = -5 V (violet line) and V_{ds} = 5 V (blue line).

To provide a deeper insight into the underlying response mechanisms and establish a quantitative comparison with individual WS_2 FETs, we extracted the characteristic rise and decay constant times of the photocurrent. The rise and decay branches of the pulses shown in Figure 4.11a-c were analysed using a double exponential fitting function, $I_d = I_0 + A_1 e^{-\frac{t}{\tau_1}} + A_2 e^{-\frac{t}{\tau_2}}$. As shown in the representative fits of the pulses at P_{inc} = 145 μW in Figure 4.12a-d, this model accurately describes the experimental data in both ambient and vacuum conditions. As said previously, the two extracted time constants, τ_1 and τ_2, represent two distinct physical mechanisms: a fats component (τ_1) associated with direct photogeneration, and a slower component (τ_2) related to trap-mediated processes. The relative contribution of these mechanisms is evaluated through the ratio of their amplitudes, A_1/A_2.

At ambient pressure, the weighted average time constants (Figure 4.12b) for the rise branch are on the order of 1 s for τ_1 and 10 s for τ_2. During the decay branch, the response is notably faster, with τ_1 decreasing to approximately 0.2 s while τ_2 remains around 10 s. The fast response is attributed to direct electron-hole generation, likely limited by sulphur vacancies in WS_2 and selenium vacancies in

$PdSe_2$. In the rising branch, the A_1/A_2 ratio is close to 1 (Figure 4.12c), indicating that the photocurrent generation is a well-balanced result of both fast and slow mechanisms. Conversely, in the decay branch, the A_1/A_2 ratio increase significantly, ranging from 10 to 100 as the incident power increases. This suggests that the return to the dark state is heavily dominated by the faster intrinsic recombination. Remarkably, these extracted time constants are at least one order of magnitude lower than those reported for individual few-layer $PdSe_2$ photodetectors[184] and compare favourably with high-performance MoS_2 FETs, which are among the widely studied TMDs-based devices.[93,185]

Upon transitioning to a high vacuum condition, the carrier kinetics undergo a significant shift. For the rise branch, the fast time constant τ_1 decreases by an order of magnitude compared to ambient conditions, while τ_2 remains stable on the order of 10 s (Figure 4.12e). The decay branch of the same light pulses presents longer constant times because of the absence of adsorbates in high vacuum. Despite these changes in speed, the A_1/A_2 ratio in vacuum remains near unity (Figure 4.12f), confirming that both the fast intrinsic and slow trap-mediated mechanism continue to contribute equally to the photocurrent.

By comparing these two regimes, it is evident that while $PdSe_2$ contributes to the high absorption, the overall kinetic signatures of the heterostructure are dominated by the WS_2 layer. The combination of $PdSe_2$ and WS_2 in the heterojunction results in shorter response times compared to single WS_2-based FETs, as described in Section 4.2.2: the higher mobility of $PdSe_2$ compared to WS_2 plays a key role in achieving shorter response times in $WS_2/PdSe_2$ heterostructures.[13]

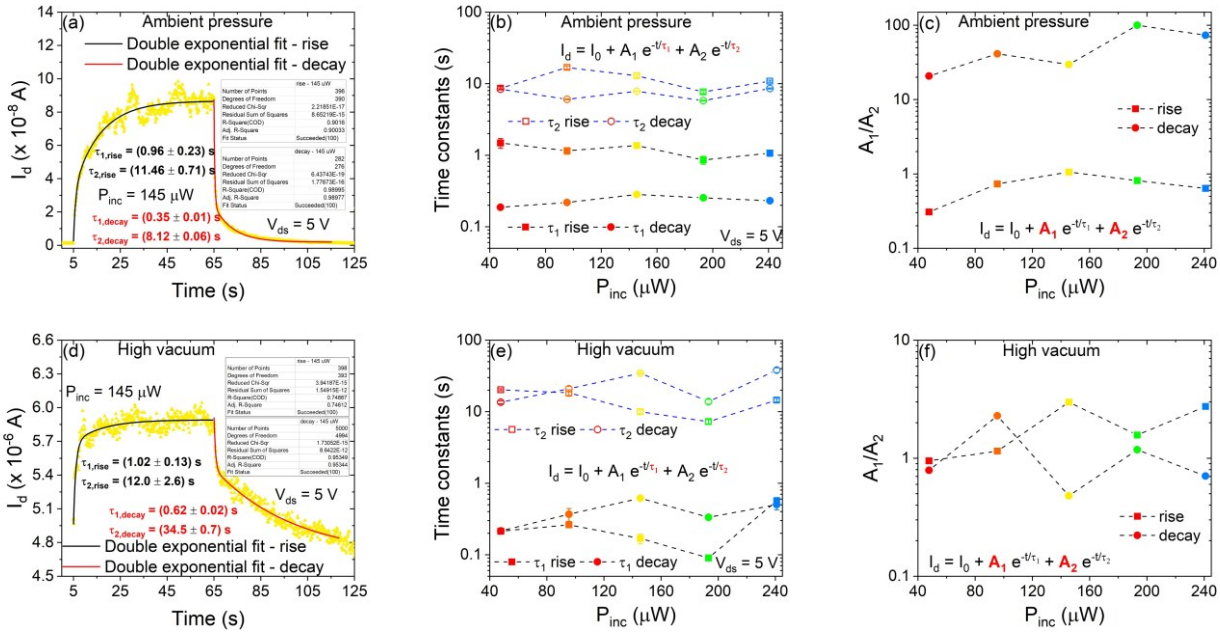


Figure 4.12: Light pulse under white light illumination at an incident laser power of 145 µW for 60 seconds at (a) ambient pressure and in (d) high vacuum at a pressure of 10^{-4} mbar with the rise (black line) and decay branch (red line) fitted with a double exponential function. Time constants τ_1 and τ_2 from a double rise/decay exponential fit of the time-resolved pulses at V_{ds} = 5 V at (b) ambient pressure and in a (e) high vacuum at a pressure of 10^{-4} mbar. A_1/A_2 ratio extracted from the double exponential fits at (c) ambient pressure and in (f) high vacuum at a pressure of 10^{-4} mbar.

The electrical properties of the $WS_2/PdSe_2$ heterostructure under white light illumination were also investigated along with the application of a voltage bias on the gate electrode. Figure 4.13a shows

the I-V characteristics in dark (black line) and under illumination at varying incident white light powers (coloured lines) at ambient pressure, with the gate electrode grounded. Notably, the I-V characteristic becomes more symmetric under illumination, although the current remains slightly higher at negative bias voltages compared to positive. The photoexcitation and photodesorption processes contribute to significantly reduce the Schottky barrier, leading to an increase in the current.[93] Figure 4.13b presents the modulation of the channel current through transfer curves at a fixed V_{ds} = 5 V, with the gate voltage swept from 50 to -50 V and back to 50 V, both in dark (black line) and under illumination at various white light powers (coloured lines). At ambient pressure, the drain current under laser illumination is higher than in dark conditions at each gate voltage. The transfer curve maintains its shape during illumination, having higher current levels for both the off and the on states. In Figure 4.13c, the I-V characteristics in dark (black line) and under illumination at varying incident white light powers (coloured lines) in high vacuum at a pressure of 10^{-4} mbar are depicted. The more symmetric behaviour is maintained both in darkness and under laser. The difference between the dark and illuminated transfer curves gets more pronounced at negative gate voltages, and the transistor does not switch off when illuminated (see transfer curves in Figure 4.13d): the photoexcitation of electrons from the initial off state of the transistor results in a left-shift of the whole transfer curve, not allowing to see the off-state of the device within the same V_{gs} range.[186] The data of Figure 4.13b and 4.13d show that the gate is very effective in controlling the photoresponse. Negative V_{gs} results clearly advantageous to achieve a high signal-to-noise ratio.

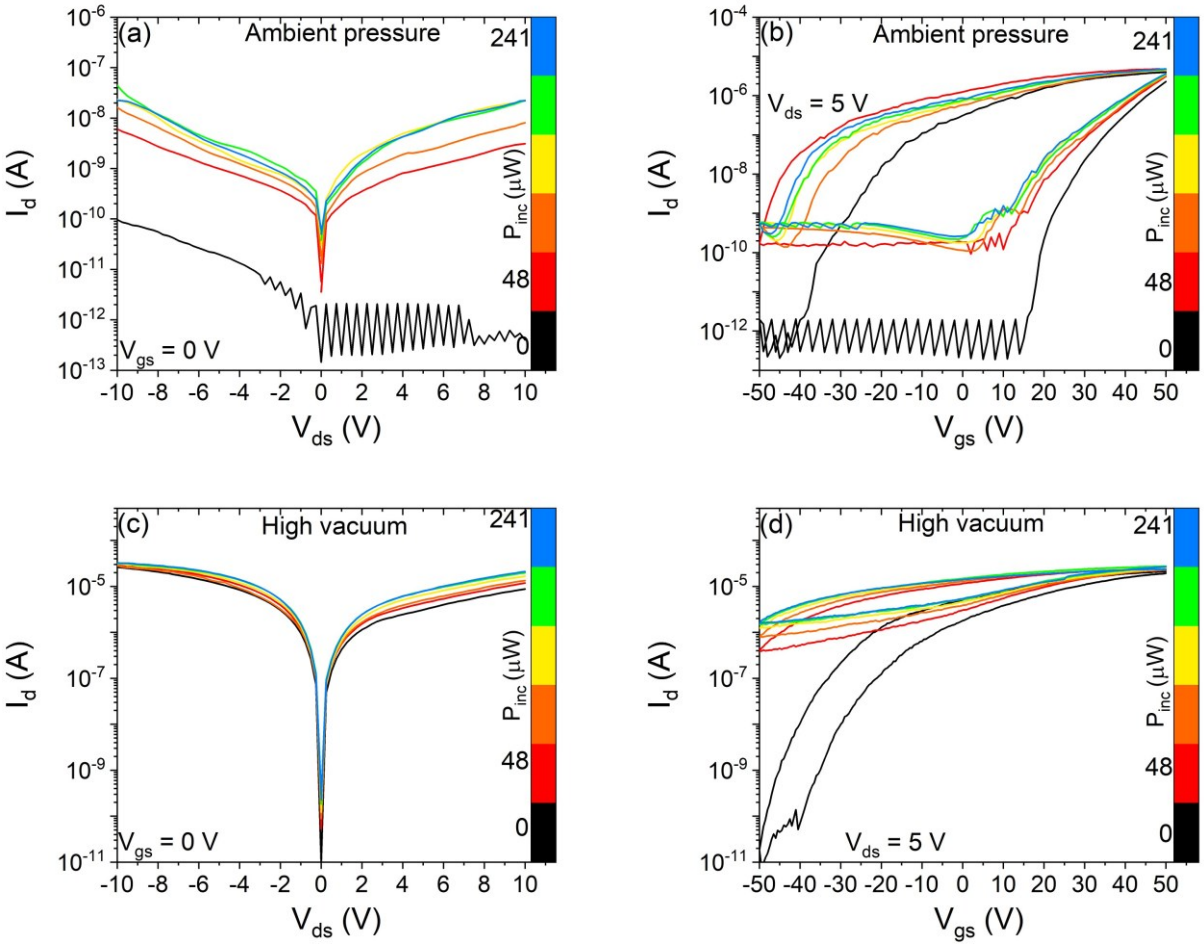


Figure 4.13: Electrical measurements of the $WS_2/PdSe_2$ heterostructure in dark and under white light illumination at (a-b) ambient pressure and in (c-d) high vacuum at a pressure of 10^{-4} mbar.

4.3.4 Visible-light photodetector and pressure optoelectronic sensor

For the evaluation of the $WS_2/PdSe_2$ heterostructure as a visible-light photodetector and a pressure optoelectronic sensor, the characterization was performed under high vacuum at a constant gate bias of V_{gs} = -50 V. This specific operating point was chosen based on the prior electrical analysis, which identified the depletion region at high negative gate voltages as the optimal regime for device performance. By operating at V_{gs} = -50 V, the dark current is minimized, thereby maximizing the photosensitivity and the signal-to-noise ratio. This configuration allows for the most precise detection of photogenerated carriers, and the variations induced by environmental pressure changes.

The spectral dependence of the photoresponse was evaluated to determine the device's efficacy across the visible range. Figure 4.14a illustrates the photocurrent as a function of the incident light wavelength. To quantify the performance, we calculated the spectral responsivity. The $WS_2/PdSe_2$ heterojunction-based device exhibits a peak responsivity of 1.2 A/W at λ = 620 nm. Notably, this value is approximately three orders of magnitude higher than those reported in literature for comparable $WS_2/PdSe_2$ devices[182], highlighting the superior photon-to-electron conversion efficiency of this specific vertical junction. Thus, the high responsivity across the visible spectrum

confirms the $WS_2/PdSe_2$ heterostructure as a highly efficient platform for visible-light optoelectronics.

Building upon the spectral analysis, the $WS_2/PdSe_2$ heterostructure was further evaluated as a pressure optoelectronic sensor. To ensure maximum sensitivity and a high signal-to-noise ratio, the incident light wavelength was fixed at λ = 620 nm, corresponding to the previously identified peak responsivity. Figure 4.14b shows the evolution of the photocurrent during transitions between high vacuum (10^{-4} mbar) and ambient pressure (10^{3} mbar). The half-filled squares represent the photocurrent as the pressure increases from high vacuum to ambient pressure, while the filled diamonds indicate the reverse transition, from ambient pressure to high vacuum. The change in photocurrent is clearly attributed to adsorption/desorption processes occurring on the materials' surfaces, which play a crucial role in modifying the photoresponse of the $WS_2/PdSe_2$ heterojunction. Notably, the return to the initial configuration demonstrates the stability of the materials under varying pressure conditions, highlighting their potential for sensing applications.

The adsorption process is governed by timescales that depend on the materials' structure and the nature of adsorbates. The slight jump in photocurrent at a pressure of around 10^{-2} mbar in the final stage (Figure 4.14b, right panel) may be attributed to a transient phase evolving between 10^{-4} and 10^{-2} mbar or to more complex mechanisms occurring in high vacuum, as previously observed in the sublinear photoresponse.[187] The evolution of the photoresponse of the $WS_2/PdSe_2$ heterojunction under varying pressure conditions was reproduced with analogous results at V_{ds} = -5 V and V_{gs} = -50 V (Figure 4.14c). Interestingly, the photocurrent levels initially observed in high vacuum (at pressures below 10^{-2} mbar) were lower than expected; this is attributed to incomplete desorption processes. The removal of physiosorbed species from the $WS_2/PdSe_2$ surface is a time-dependent phenomenon, with complete desorption occurring on timescales significantly longer than those employed in the initial measurement cycles. To further confirm this explanation, Figure 4.14d compares the photocurrent evolution of the $WS_2/PdSe_2$ heterostructure during the transition from high vacuum to ambient pressure at V_{ds} = - 5 V and V_{ds} = 5 V, acquired under the same pressure cycle. Notably, in both bias configurations, a distinct slight jump in photocurrent is observed at pressures below 10^{-2} mbar, prior to the expected monotonic decrease as the pressure increases toward ambient levels. The subsequent reduction in photocurrent and the overall slowing of the response are likely governed by deep and long-lived trap states, which hinder the desorption kinetics of O_2 and H_2O molecules. These surface states act as persistent barriers, requiring extended periods for the system to reach environmental equilibrium.

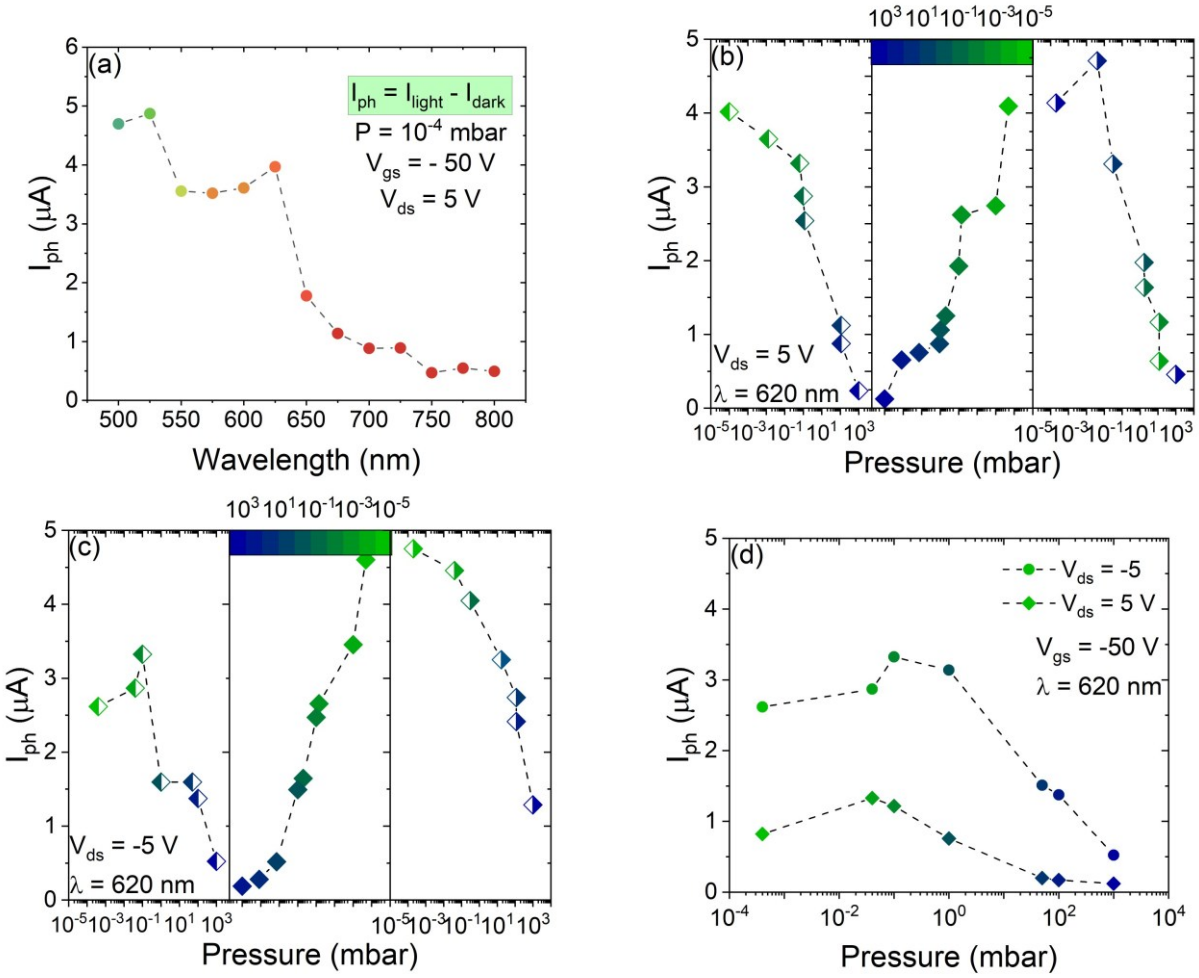


Figure 4.14: (a) Photocurrent of the $WS_2/PdSe_2$ heterostructure in high vacuum at a pressure of 10^{-4} mbar under laser at different wavelengths at V_{ds} = 5 V and V_{gs} = -50 V. (b) Evolution of the photocurrent of the $WS_2/PdSe_2$ heterostructure at λ = 620 nm under pressures from high vacuum at 10^{-4} mbar to ambient pressure. The colour scale in the graph at the middle goes from 10^3 mbar (blue) to 10^{-4} mbar (green). (c) Evolution of the photocurrent of the $WS_2/PdSe_2$ heterostructure at λ = 620 nm under pressures from high vacuum at 10^{-4} mbar to ambient pressure at V_{ds} = -5 V and V_{gs} = -50 V. (d) Comparison of photocurrent as a function of the pressure from high vacuum at 10^{-4} mbar to ambient pressure at V_{ds} = -5 V (coloured circles) and V_{ds} = 5 V (coloured squares).

4.3.5 Persistent photoconductivity

Persistent conductivity (PPC) is a phenomenon in which the electrical conductivity of a material remains significantly higher than its initial dark state for an extended period after the light source has been removed. In 2D semiconductors, PPC is often undesirable for high-speed photodetection; however, it has recently emerged as a cornerstone for neuromorphic engineering. By exploiting the slow relaxation of photogenerated carriers, PPC can be used to emulate the synaptic plasticity of the human brain, enabling the development of optoelectronic synapses and non-volatile memory devices.[12,188,189]

The presence of PPC in the $WS_2/PdSe_2$ heterostructure is shown in Figure 4.15a: the black curve corresponds to the transfer curve recorded in high vacuum at V_{ds} = 5 V under dark conditions, while the yellow curve corresponds to the transfer characteristic acquired in dark under the same experimental conditions after the device was exposed to illumination. The initial dark state (black

curve) is lost shortly after measurements under illumination. The resulting dark characteristic after illumination exhibits a significant leftward shift and an increased current level. The inset of Figure 4.15a shows single one-second light pulses applied to the $WS_2/PdSe_2$ heterostructure at V_{ds} = 5 V and different V_{gs}, ranging from -50 to 25 V with steps of 25 V. The PPC is more evident at V_{gs} = -50 V. This behaviour is a clear signature of the photogating effect. Under illumination, photons excite electrons from the valence band to the conduction band, thereby generating electron-hole pairs. Additionally, electrons can be excited through defect states, contributing to the photocurrent. Under a negative bias (V_{gs} = -50 V), holes may get trapped in interfacial sites, preventing electron-hole recombination. This generates a photogating effect and allows the photogenerated electrons to persist longer in the conduction band. As a result, the conductivity remains higher than the initial dark state even after the light is switched off, leading to PPC. To thoroughly investigate the mentioned PPC, a series of one-second light pulses was applied to the device at V_{gs} = -50 V and V_{ds} = 5 V, with increasing incident laser power, from 31 to 311 µW. The result is shown in Figure 4.15b. The $WS_2/PdSe_2$ heterojunction exhibits an initial high carrier concentration in dark, retained from the previous exposure to light. It can be observed that the current level can be progressively increased with subsequent light pulses, and this can be exploited for optoelectronic applications. As the dark current, which refers to the current level in the dark state before illumination, the peak current, which corresponds to the maximum current achieved under illumination, linearly increases with the incident laser power, as shown in the inset of Figure 4.15b.

Figure 4.15c-e show 30-seconds and 60-seconds light pulses, respectively, at V_{gs} = -50 V and V_{ds} = 5 V, with increasing incident laser power. The PPC is still present; the sublinear dependence of the photocurrent on the incident laser power is shown in Figure 4.15d-f with power law exponents α lower than the unity. This sublinear regime is associated with the dynamics of photo-generated carriers, including recombination of excitons, charge trapping in interfacial states with SiO_2 or within sulphur and selenium vacancies in WS_2 and $PdSe_2$, respectively. Notably, the α exponent extracted at V_{gs} = -50 V is lower than that observed at zero gate bias (0.22 ± 0.03 at V_{gs} = -50 V compared to 0.49 ± 0.08 at V_{gs} = 0 V). This reduction is attributed to the onset of more complex carrier dynamics under high negative bias, where the photogating effect plays a more dominant role in modulating the channel conductance.

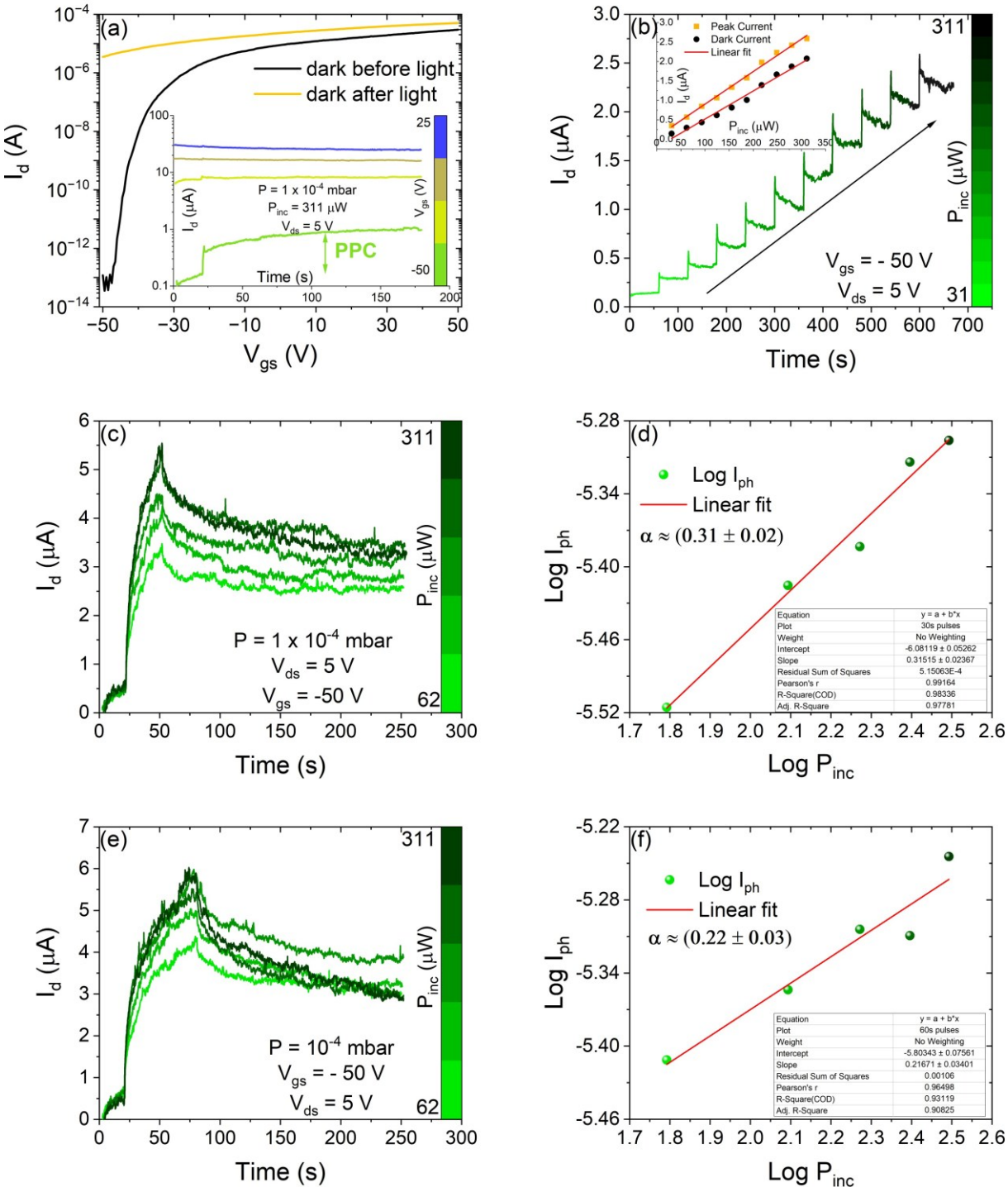


Figure 4.15: (a) Transfer curves of the $WS_2/PdSe_2$ heterostructure in dark before (black line) and after (yellow line) illumination at V_{ds} = 5 V in high vacuum at room temperature (in the inset: gate voltage-dependent one-second light pulses at V_{ds} = 5 V at different V_{gs} from -50 V to 25 V in steps of 25 V, showing the PPC). (b) Single one-second light pulses at V_{ds} = 5 V and V_{gs} = -50 V with increasing incident laser power (in the inset: peak (yellow squares) and dark (black circles) current of one-second light pulses as a function of the incident laser power with the linear fit (red line)). (c) 30-seconds and (e) 60-seconds light pulses at V_{ds} = 5 V and V_{gs} = -50 V with increasing incident laser power. (d) Photocurrent from the 30-seconds light pulses as a function of the incident laser power (log scale) with $\alpha = 0.31 \pm 0.02$. (f) Photocurrent from the 60-seconds light pulses as a function of the incident laser power (log scale) with $\alpha = 0.22 \pm 0.03$.

4.3.6 Optoelectronic synaptic devices for neuromorphic computing

Recently, the scientific community has started investigating and exploiting PPC for several applications, such as optoelectronic synapses, optical memories, and more complex device architectures.[102] The $WS_2/PdSe_2$ heterostructure was tested as an optoelectronic synaptic device, mimicking synaptic functions in the brain. This behaviour arises from the photogeneration of carriers and their subsequent trapping at defect sites or at the $WS_2/PdSe_2$ interface, resulting in a photogating effect that leads to PPC. This gradual decay and retention of photocurrent after light exposure emulate the dynamics of short- and long-term synaptic plasticity. Specifically, by exploiting the gate-tunable PPC, we demonstrate the short-term and long-term plasticity through paired-pulse facilitation (PPF) and post-tetanic potentiation (PTP).

To evaluate the $WS_2/PdSe_2$ heterostructure as a synaptic platform, we first examined the response to a single one-second light pulse. Figure 4.16a shows single one-second light pulses at t = 20 s with V_{ds} = 5 V and V_{gs} = -50 V at different incident laser powers, showcasing a stable $I_{dark,2}$ level longer than 150 s. In Figure 4.16b, the transient and memory current are plotted as a function of the incident laser power. The transient current accounts for the difference between the peak current and the dark state before illumination. Meanwhile, the memory current represents the difference in current between the two dark states before and after illumination ($I_{dark,2} – I_{dark,1}$), highlighting the device photonic nonvolatile characteristic. Both the current signals increase with increasing incident laser power, indicating that the conductance states of the device can be continuously tuned. The increase in memory current as the incident laser power increases suggests the transition from STP to LTP. [190,191]

The transition from individual events to more complex short-term plasticity was investigated by applying a series of 15 consecutive one-second light pulses with one-second intervals (Figure 4.16c). It can be observed that the first spike leads to an increase in the drain current (A_1). When the second spike is applied, the current has not yet fully returned to its original level, resulting in a higher induced current (A_2) compared to that caused by the first spike. The PPF index, given by the percentage ratio of the currents of the first two spikes, is around 137%, which is a valuable result if compared with the literature.[192,193] The repetition of light pulses results in the accumulation of additional photogenerated charge carriers, leading to an increase in the current level. The PTP index, defined as the percentage ratio between the intensity of the last light pulse and the first one, A_{15}/A_1, follows the same trend of PPF, being constant around 300% (Figure 4.16d).[190] Then, the robustness and saturation of these synaptic effects were explored by extending the stimulation to 30 consecutive one-second pulses (Figure 4.16e). Increasing the number of pulses demonstrates the cumulative nature of the carrier trapping mechanism. The corresponding extracted PTP and PPF indexes are shown in Figure 4.16f, showcasing similar results.

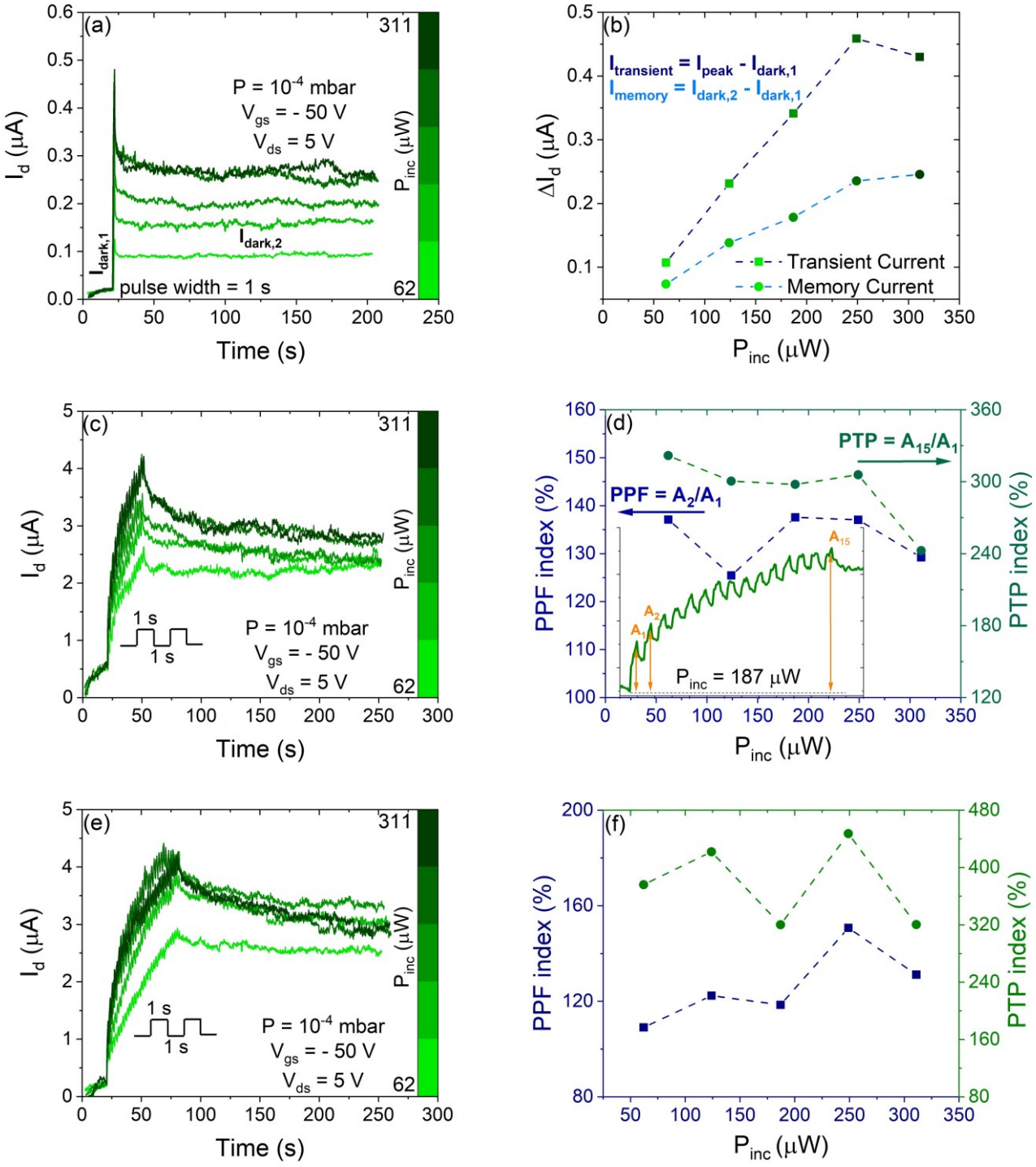


Figure 4.16: (a) One-second light pulses with long stability $I_{dark,2}$ at V_{ds} = 5 V and V_{gs} = -50 V with increasing incident laser power. (b) Transient and Memory current as a function of incident laser power. (c) Series of fifteen one-second pulses with one-second interval between them at V_{ds} = 5 V and V_{gs} = -50 V at different incident laser power. (d) PPF (left axis, blue squares) and PTP (right axis, blue circles) as a function of incident laser power (in the inset: zoom of the series of pulses at incident laser power of 187 μW, indicating A_1, A_2, A_{15}). (e) Series of thirty one-second light pulses with one-second interval between them at V_{ds} = 5 V and V_{gs} = -50 V at different incident laser power. (f) PPF (left axis, blue squares) and PTP (right axis, green circles) as a function of the incident laser power.

Beyond the quantification of synaptic indices, the cumulative response of the $WS_2/PdSe_2$ heterostructure to pulse trains enable the emulation of higher order cognitive functions. A fundamental aspect of biological intelligence is the acquisition and retention of knowledge through iterative cycles of learning, forgetting, and re-learning (Figure 4.17a). This behaviour was successfully emulated in the $WS_2/PdSe_2$ heterostructure, as illustrated in Figure 4.17b. To simulate the initial learning phase, the device was stimulated with thirty consecutive one-second light pulses. Following the cessation of stimuli, the device exhibited a forgetting phase characteristic by a natural decay in conductance as trapped carriers slowly recombined. Notably, a single subsequent light pulse was sufficient to restore the conductance to its previous maximum. Mirroring the biological efficiency where re-learning occurs more rapidly than the initial acquisition, the $WS_2/PdSe_2$ heterostructure requires significantly fewer stimuli to return to a high-conductance state compared to the initial learning process.

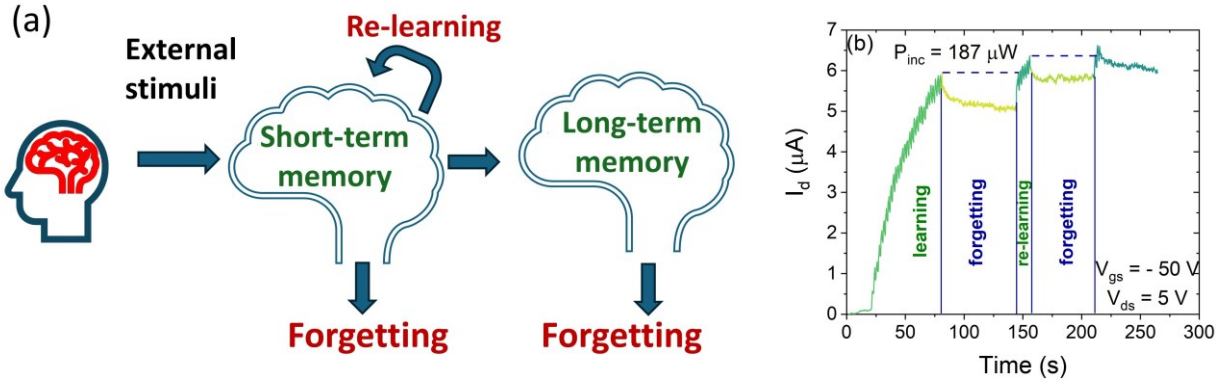


Figure 4.17: (a) Schematic of human brain operating mode. (b) Learning – forgetting – re-learning phases of the operation of the $WS_2/PdSe_2$ heterostructure as a synaptic device.

4.3.6 Optoelectronic synaptic non-volatile memory

As previously noted, the dark state after illumination undergoes a complete change: the transfer curve shifts to the left after exposure to white light at an incident power of 311 µW. This behaviour can be associated with a p-doping-like effect in the $WS_2/PdSe_2$ heterojunction. To shift the transfer curve back to the right and restore the initial configuration – or at least a more similar state – positive gate voltage pulses were applied for different time intervals. Figure Figure 4.18a shows the time evolution of the transfer curve of the $WS_2/PdSe_2$ heterostructure at V_{ds} = 5 V after consecutive gate pulses at V_{gs} = 50 V, with the duration of each gate pulse indicated in the legend. This electrical response to positive gate voltage pulses was used to reproduce one-cycle of a potential non-volatile optoelectronic memory.[194] A sequence of one-second light pulses with a one-second interval between them was applied to the device for 60 s with V_{ds} fixed at 5 V and V_{gs} fixed at -50 V. After the readout of the information at the dark level after illumination, the erasing procedure was done through a 340 s long gate pulse at V_{gs} = 50 V, thereby recovering the dark state before illumination. The optoelectronic programming and electrical erasing of the memory device was tested at different incident laser power, from 62 to 311µW. Figure 4.18b shows a complete cycle at an incident power of 62 µW as an example; the gate voltage sequence throughout the measurements is shown in the inset. The transient and memory currents were extracted and presented as a function of the incident laser power in Figure 4.18c. The values are reasonably higher than the single one-second light pulse in the same electrical and light conditions. The same measurements were performed at different

incident laser powers (Figure 4.18 d-e-f-g). Additionally, the stability of the reading state of the memory was demonstrated in Figure 4.18h. These results pave the way for the realization of efficient devices that could be implemented in the field of neuromorphic computing.

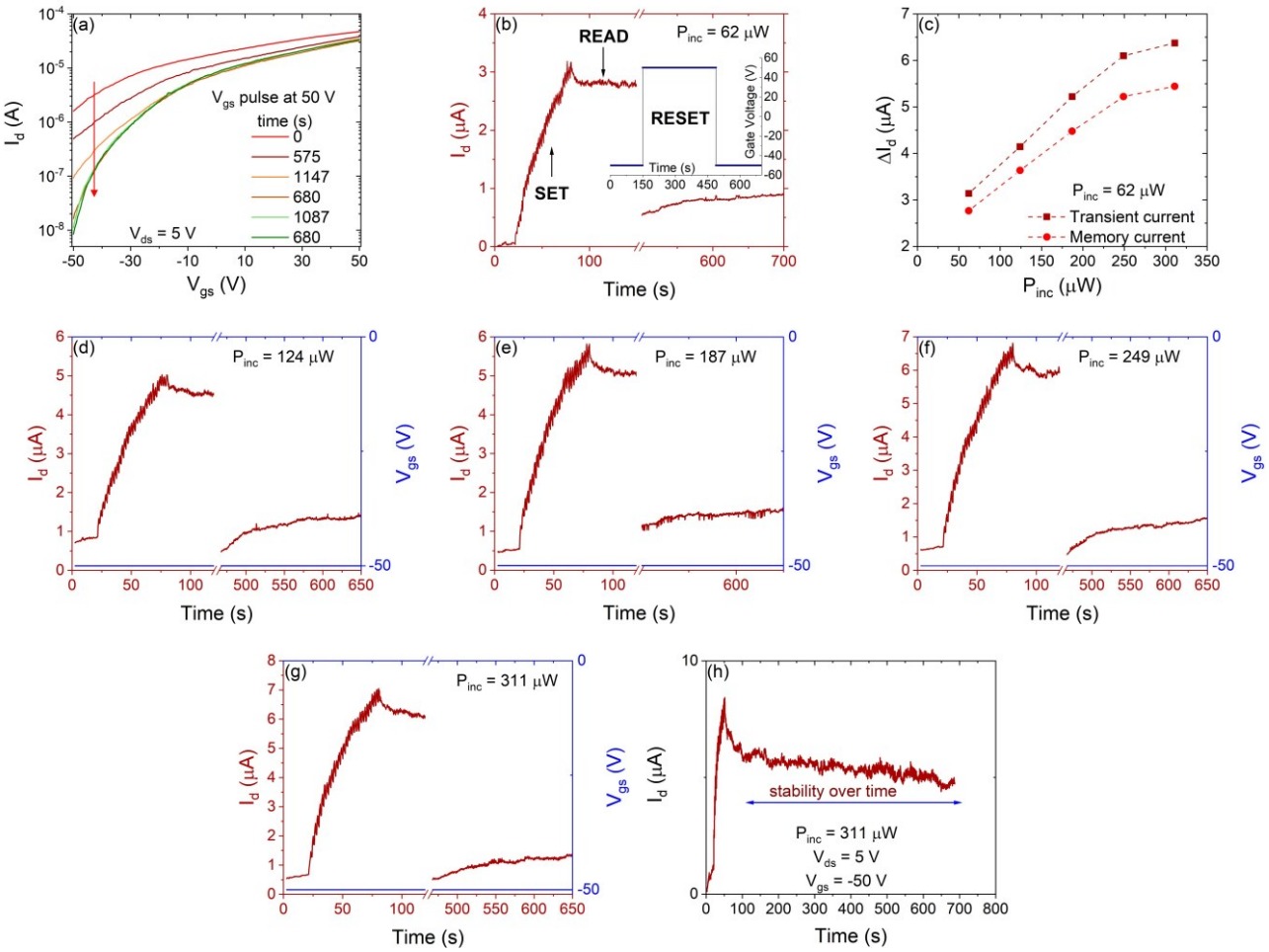


Figure 4.18: (a) Time evolution of the transfer curve of the $WS_2/PdSe_2$ heterostructure after repeated gate voltage pulses of 50 V. The time of each gate pulse before the transfer measurement is indicated in the legend. (b) One cycle programming – readout – erasing cycle of a non-volatile memory device based on the $WS_2/PdSe_2$ heterojunction (in the inset: gate voltage pulse across all the cycle). (c) Transient and memory current as a function of the incident laser power. One cycle programming – readout – erasing cycle of a non-volatile memory device based on the $WS_2/PdSe_2$ heterojunction at different light powers from (d) 124 μW to (g) 311 μW. (h) stability of the state after the application of a series of consecutive light pulses over a period of 300 s.

5. MOLYBDENUM DISELENIDE HOMOJUNCTIONS

The objective of next-generation information technologies is increasingly focused on the seamless integration of digital logic, non-volatile memory, and neuromorphic computing within a single hardware platform. While 2D materials are ideal candidates for this evolution due to their atomic thickness and gate-tunable electronic properties, the development of all 2D-cFETs remains hindered by the scarcity of stable p-type semiconductors and the complexities of controllable doping. Y. Jin et al.[195] reported p-type $MoSe_2$ obtained through Nb substitutional doping, where Mo atoms were partially replaced by Nb, which has one fewer valence electron than Mo. Fan et al.[196] demonstrated efficient carrier-type modulation in a single $MoSe_2$ flake by combining rapid thermal annealing in air for p-type doping and triphenylphosphine (PPh_3) coating for n-type doping, enabling the fabrication of a lateral $MoSe_2$ p-n homojunction with a rectification ratio of 10^4, an ideality factor of 1.2, and enhanced photoresponse. Most p-doping strategies rely on approaches such as chemical dopants[197–200], contact engineering[201,202], or oxide coatings[203]. However, these methods often suffer from inhomogeneity or degradation of carrier mobility, and they are not compatible with vdW stacking, which is essential for achieving local doping in more complex multilayer structures. This chapter explores an interface-engineering approach to address these limitations using $MoSe_2$. We demonstrate that by coupling pristine $MoSe_2$ with chromium oxychloride (CrOCl), it is possible to achieve robust p-type conduction through vdW interfacial charge transfer, bypassing the need for traditional chemical doping. This transition from the inherent n-type transport of pristine $MoSe_2$ to induced p-type behaviour enables the fabrication of cFETs with balanced carrier mobilities. F. Zhong et al.[204] reported the synthesis of undoped (n-type) and Ta-doped (p-type) $MoSe_2$ flakes and fabricated complementary inverters entirely based on $MoSe_2$, achieving high gain around 15 and low power consumption of 20 nW at a 5 V bias. Beyond logic applications, the increasing demand for high-density and low-power data storage has driven significant interest in memory devices, which have been widely reported in the literature, by exploiting various charge trapping and detrapping mechanisms.[189,205–209] Among emerging architectures, FETs incorporating floating gate structures have attracted attention due to their non-volatile operation, scalability, and compatibility with 2D materials. By exploiting the high charge storage capacity of multilayer graphene, an ultrafast non-volatile flash memory has been demonstrated, featuring write/erase times down to 20 ns, a channel current window of 10^6 A, and robust non-volatile retention performance.[210] L. Wu et al.[211] also utilized a hBN layer to enable charge accumulation in floating gate memory devices constructed from vdW heterostructures featuring atomically sharp interfaces between distinct functional elements. The devices achieved programming/erasing times in the nanosecond range and exhibited a current window of approximately 10^{10} A. Furthermore, such type of devices can emulate synaptic behaviour, enabling neuromorphic computing and artificial intelligence applications, where memory and processing are closely integrated.

Building upon this material platform, the following sections detail the realization of diverse device functionalities. We first characterize the individual pristine $MoSe_2$ and $MoSe_2$/CrOCl FETs, as well as the anti-ambipolar transport in pristine $MoSe_2$/p-doped $MoSe_2$ homojunctions, demonstrating their implementation in both resistive-load and CMOS inverter configurations. Furthermore, we exploit the interfacial coupling to implement multi-level non-volatile floating gate memory and artificial synaptic devices capable of long-term plasticity. Finally, an optoelectronic characterization provides deeper insight into the carrier dynamics of the pristine and p-doped $MoSe_2$ devices and the resulting

homojunction. Together, these results establish a versatile architecture that bridges the gap between conventional digital logic and brain-inspired computing.

All the presented electrical measurements were conducted in high vacuum at a pressure of 6 x 10^{-5} mbar.

5.1 Materials characterization

Figure 5.1a shows an optical image of a device fabricated according to the procedures detailed in section 2.1.3. As indicated by the labels, multiple electrodes are integrated onto a single $MoSe_2$ flake, enabling the realization of various device configurations. Specifically, the ED device is the investigated one with pristine n-type $MoSe_2$ channel, the HJ device is the one with p-doped $MoSe_2$/CrOCl channel and the JE device is the heterostructure formed by the lateral combination of pristine $MoSe_2$ and $MoSe_2$/CrOCl bilayer. The corresponding schematic of the device architecture is shown in Figure 5.1b, where the highly doped Si substrate acts as the control gate of the transistor, and the Au electrode serves as the floating gate. The Ti/Au contacts are used as drain and source electrodes of the transistors.

Multiple profiles were extracted from the AFM image in the inset of Figure 5.1c, and the thickness of pristine $MoSe_2$ was estimated to be approximately 30 nm, as reported in the profile in Figure 5.1d. This analysis allowed also for the estimation of the thickness of the hBN and CrOCl layers, whose values are 22 nm and 11 nm, respectively, as shown in Figure 1e.

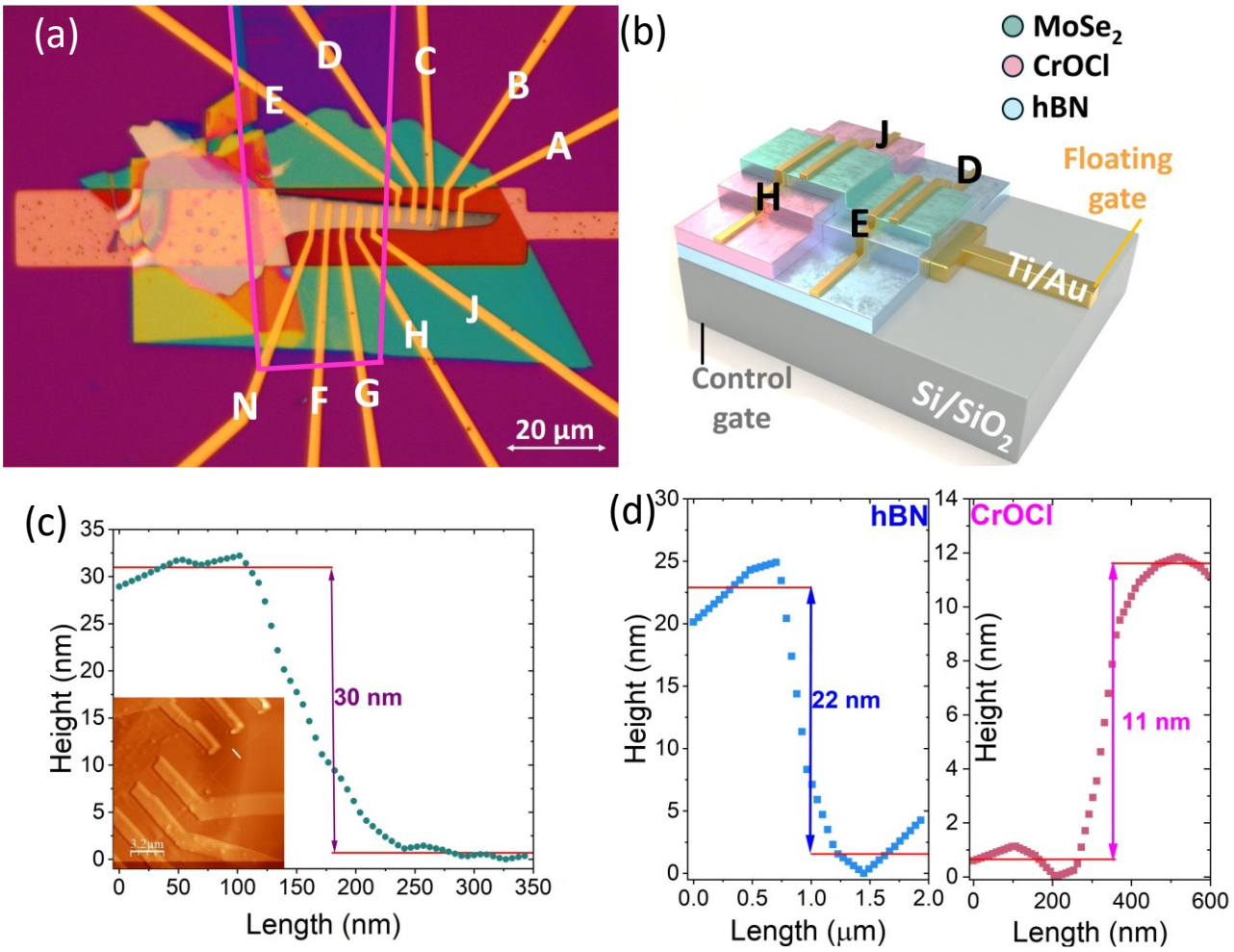


Figure 5.1: (a) Optical image of the $MoSe_2$ cFET showing the pristine $MoSe_2$, the $MoSe_2$/CrOCl and the homojunction devices with labelled electrodes. The pink line delimits the CrOCl flake. (b) Schematic of the fabricated cFET. (c) AFM profile of the $MoSe_2$ flake (in the inset: AFM image of the $MoSe_2$ cFET. The white line indicates the region from which the height profiles were extracted) (d) AFM profiles of the hBN and CrOCl layers.

5.2 Pristine and p-doped $MoSe_2$

To establish a baseline for the transport properties of our material system, we first conducted an individual electrical characterization of the pristine $MoSe_2$ and $MoSe_2$/CrOCl transistor. This step is fundamental to confirm the successful transition from the inherent n-type conduction of $MoSe_2$ to the interface-induced p-type behaviour in the CrOCl-coupled region.

Figure 5.2a displays the transfer characteristics of the pristine $MoSe_2$ transistor measured at different source-drain biases, from 100 to 300 mV. The pristine $MoSe_2$ shows n-type conductive behaviour, with higher current at positive gate voltage. The on/off current ratio remains on the order of 10^4. The clean hBN/$MoSe_2$ interface results in non-hysteretic transfer curves, and sharp switching between the off and on states of the transistor. For electrons, the field-effect mobility, $\mu_{eff,e}$, is around 18 $cm^2\ V^{-1}\ s^{-1}$. Figure 5.2b shows the output curves of the pristine $MoSe_2$ device, with V_{gs} stepped from -5 to 5 V in 1 V increments. The n-type behaviour is further confirmed. Moreover, the I_d vs V_{ds} curves exhibit a slight Schottky-like behaviour, which can be attributed to the Cr/$MoSe_2$ interface.[212] The n-type behaviour of $MoSe_2$ is expected due to the presence of selenium vacancies, which act as

donor-like states. Such chalcogen vacancies are common in TMDs and typically pin the Fermi level close to the conduction band minimum, as demonstrated by density functional theory (DFT) calculations.[213–215]

Figure 5.2c shows the transfer curves of the $MoSe_2$/CrOCl transistor at different V_{ds}. The device transitions to p-type conduction because of the direct contact with the CrOCl layer. The transfer characteristics have on/off current ratios one order of magnitude lower with respect to pristine $MoSe_2$. The field-effect mobility of the majority carriers can be calculated as stated previously. In this case, the gate oxide capacitance is given by the series capacitance of hBN and CrOCl, $\frac{1}{C_{ox}} = \frac{1}{C_{hBN}} + \frac{1}{C_{CrOCl}}$. When considering holes, the mobility, $\mu_{eff,h}$, is 1.1 $cm^2\ V^{-1}\ s^{-1}$. The output curves of the $MoSe_2$/CrOCl device are reported in Figure 5.2d with V_{gs} stepped from -5 to 5 V in 1 V increments. The presence of the CrOCl layer, which is a vdW antiferromagnetic insulator, allows for the tuning of the polarity of major carriers in the $MoSe_2$ flake. According to DFT calculations, the polarity inversion induced by interfacial coupling with CrOCl originates mainly from charge transfer from the TMD layer to the polymer and subsequent electron-electron (e-e) interactions in the surface states of CrOCl.[213] In detail, electrons are transferred from the $MoSe_2$ flake to the CrOCl layer, where they accumulate on the CrOCl side of the interface, leaving holes in the $MoSe_2$. However, the transferred charges on the CrOCl side tend to localise and form an electronic crystal state driven by strong e–e interactions. As a result, CrOCl preserves its insulating nature despite the charge transfer, while the Fermi level of $MoSe_2$ shifts towards the valence band maximum, leading to p-type behaviour.

Figure 5.2e displays the transfer curves of the pristine (red dashed lines) and p-doped (blue dashed lines) $MoSe_2$ FETs on linear scales. The linear fits used for extracting the transconductance are represented by the red and blue solid lines. As shown in Figure 5.2f, the field-effect mobility results independent on the V_{ds}, maintaining values around 18 $cm^2\ V^{-1}\ s^{-1}$ for electrons and 1.1 $cm^2\ V^{-1}\ s^{-1}$ for holes.

All the presented measurements were acquired using the Au gate, denoted as floating gate. Since the entire device was fabricated on top of the Au gate, the same results were obtained using the back Si gate.

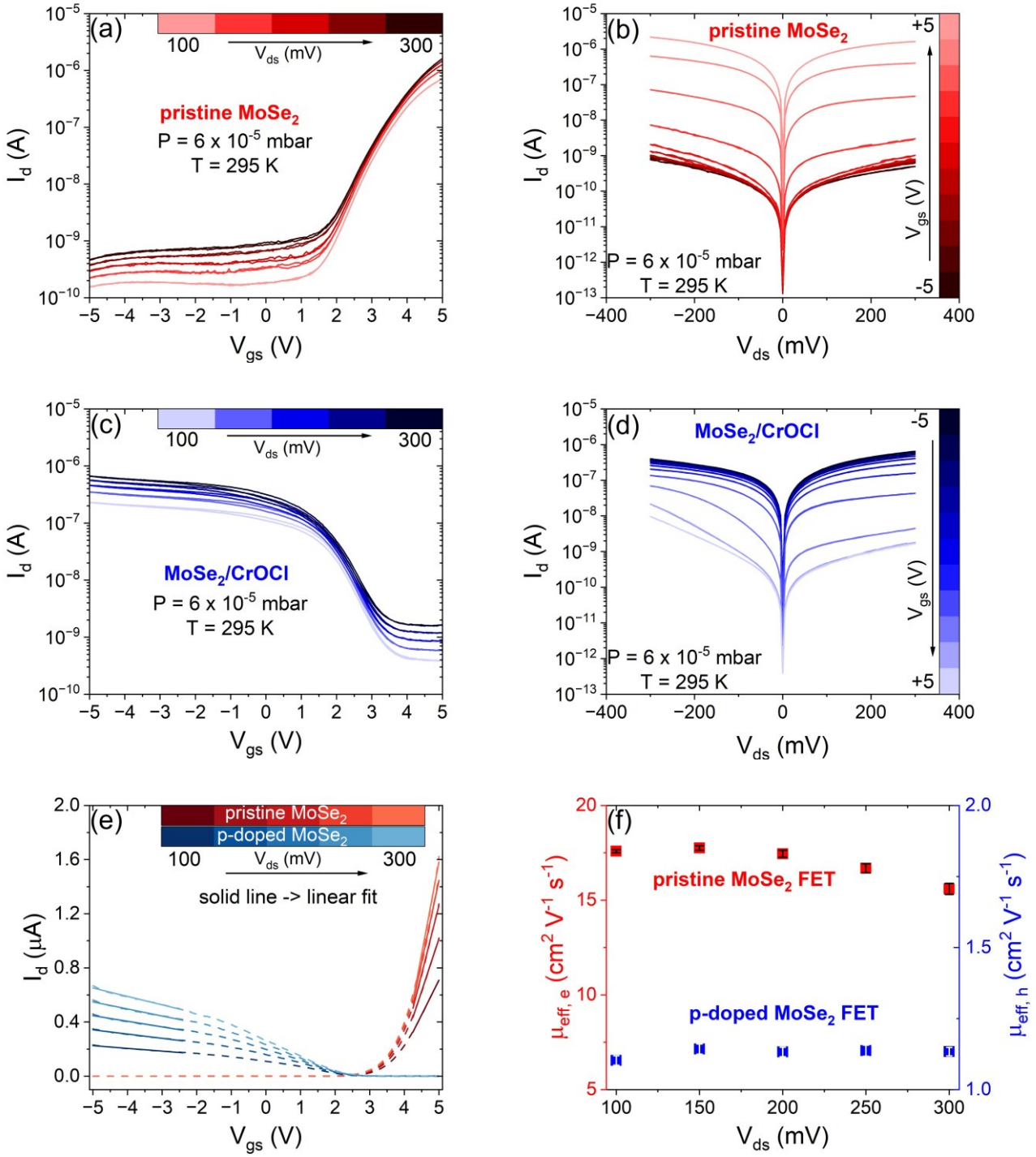


Figure 5.2: Electrical characterization of the pristine and p-doped $MoSe_2$ devices at room temperature in high vacuum at a pressure of 6 x 10^{-5} mbar. Transfer characteristics at different V_{ds} of the (a) pristine $MoSe_2$ and (c) $MoSe_2$/CrOCl devices. Output curves of the (b) pristine $MoSe_2$ and (d) $MoSe_2$/CrOCl devices. (e) Transfer curves of the pristine (red) and p-doped $MoSe_2$ devices on linear scale. The linear fit of the linear region of the transfer curves is reported with solid lines. (f) Electron (left-axis, red squares) and holes (right-axis, blues sqaures) mobility at different V_{ds}, from 100 to 300 mV.

5.3 Anti-ambipolarity in pristine $MoSe_2$/p-doped $MoSe_2$ homojunctions

Figure 5.3a shows the I-V characteristic at zero bias on the gate electrode of the homojunction formed by the lateral combination of pristine $MoSe_2$ and p-doped $MoSe_2$, as evidenced by its inset.

The device exhibits an ohmic contact, facilitating the analysis of the observed electrical behaviour of the homojunction. Figure 5.3b shows the transfer curve of the heterostructure (green line) with a V_{ds} of 100 mV. An anti-ambipolar behaviour is observed, characterised by a pronounced current peak in the gate-voltage range between 1.5 and 3.5 V. This region corresponds to the transition from the off (on) to the on (off) state of the pristine (p-doped) $MoSe_2$ channel. The anti-ambipolarity arises from the series connection of the n-type and the p-type transistor in which the threshold voltage of the n-$MoSe_2$ is lower than the threshold voltage of the p-doped $MoSe_2$ transistor. The peak current, also referred to as the on-state current of the homojunction, is hundreds of times lower than the on-state current of the individual pristine or p-doped $MoSe_2$ device.[216–221] The reason is that, as shown in Figure 5.3b, the transfer curve of the heterostructure can be interpreted as the superposition of the transfer curves of pristine $MoSe_2$ and $MoSe_2$/CrOCl in their most resistive branches.[222] The channel current is mainly limited by the off-state of the pristine $MoSe_2$ device for $V_{gs} < 1.5$ V and by the off-state of the p-doped $MoSe_2$ channel for $V_{gs} > 3.5$ V.

The absence of significant modulation outside this range suggests that the homojunction can be exploited as a resistive element in more complex logic circuits. Additional contact configurations across the homojunction were investigated by pairing electrodes from the pristine $MoSe_2$ region with those from the p-doped $MoSe_2$ region of the device, and vice versa. Figure 5.3c-d show the I-V characteristics at $V_{gs} = 0$ V and the transfer curves at $V_{ds} = 100$ mV of the homojunctions formed using the central contact of the pristine $MoSe_2$ device as the source electrode. Conversely, Figure 5.3e-f show the corresponding measurements for homojunctions formed with the central contact of the p-doped $MoSe_2$ flake as the drain electrode. The transfer curves still present an anti-ambipolar behaviour, attributed to the series connection of a n-type and a p-type transistor. These results highlight the versatility of the device architecture and are promising for its integration into logic gates structures, such as inverters.

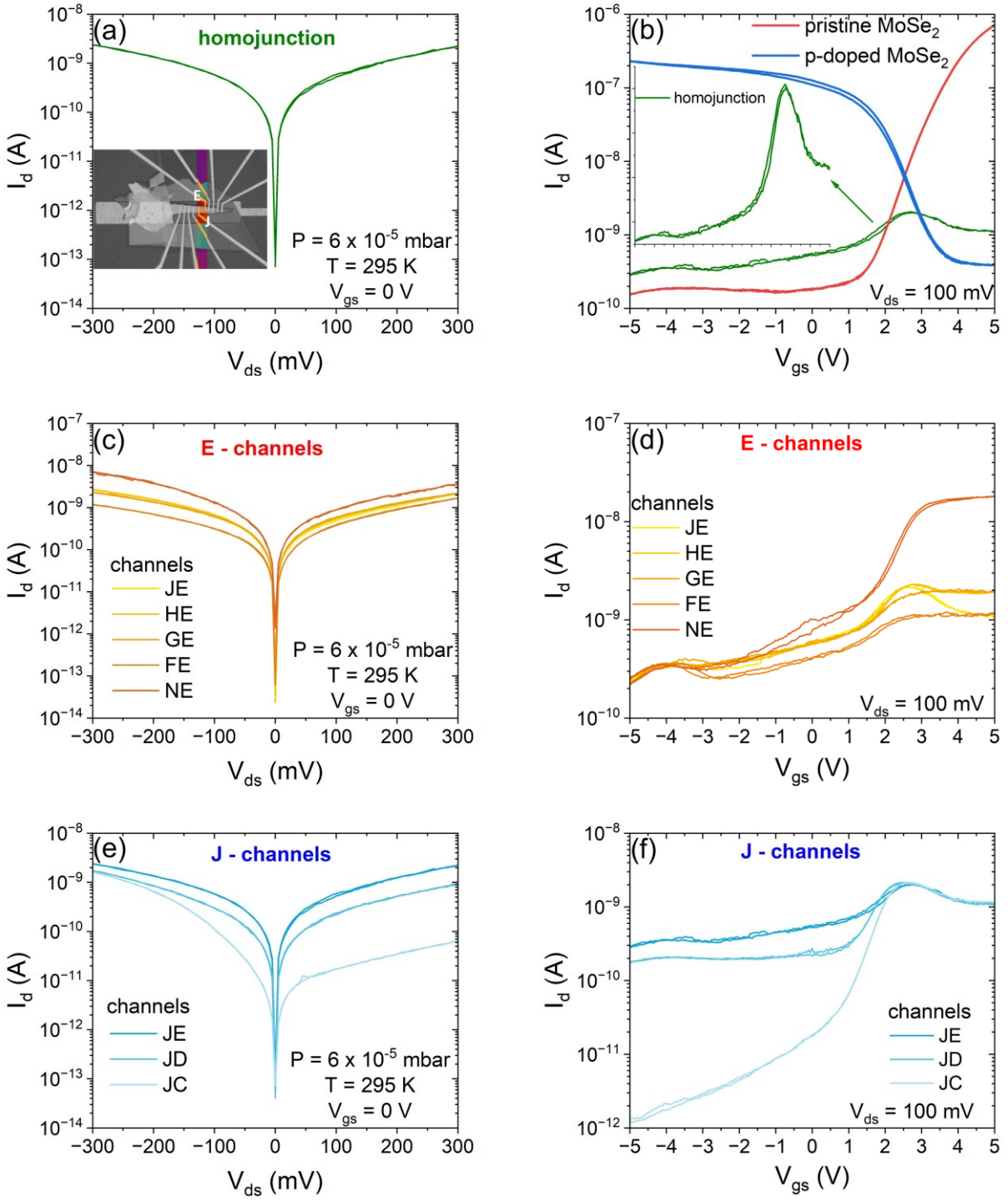


Figure 5.3: Electrical characterization of the homojunction formed by the lateral combination of pristine $MoSe_2$ and p-doped $MoSe_2$ at room temperature in high vacuum at a pressure of 6 x 10^{-5} mbar. (a) I-V characteristic at V_{gs} = 0 V and (b) transfer curve at V_{ds} = 100 mV of the central heterostructure (green line). Transfer curves of the pristine $MoSe_2$ (red line) and p-doped $MoSe_2$ (blue line) at V_{ds} = 100 mV (in the inset: transfer of the homojunction on a zoomed linear scale to highlight its anti-ambipolarity). (c) I-V characteristics at V_{gs} = 0 V and (d) transfer curves at V_{ds} = 100 mV of multiple contact configurations across the homojunction using the central contact of the pristine $MoSe_2$ as the source electrode. (e) I-V characteristics at V_{gs} = 0 V and (f) transfer curves at V_{ds} = 100 mV of multiple contact configurations across the homojunction using the central contact of the p-doped $MoSe_2$ as the drain electrode.

5.4 Inverters: resistive-load and CMOS configuration

Building upon the individual transport properties established in the previous section, we integrated the n-type and p-type regions of the $MoSe_2$ flake into logic inverter circuits. To evaluate their performance as digital building blocks, we first investigated resistive-load configurations. In these circuits, the pristine n-type $MoSe_2$ FET serves as the driver transistor, while the load is implemented using various contact configurations across the $MoSe_2$/CrOCl homojunction to act as a resistive element. The static performance of these inverters is characterized by their VTC. Figure 5.4a presents a representative VTC, using the ED transistor, illustrating the methodology used to determine the characteristic points of the VTC for the calculation of the noise margins. The schematic of this inverter configuration is depicted in the inset of Figure 5.4a. Figure 5.4b compares the VTCs for different inverter configurations. The threshold voltage, V_T, is obtained from the intersection of VTC with the line $V_{out} = 0.02 \times V_{in}$, where 0.02 is the ratio between the output and input range (100 mV/5 V). The graphical representation of such equation is depicted in Figure 5.4b with a pink line. As expected, V_T approaches 2.5 V for all the depicted curves.[20,80] It can be noted that the output signal is high for $0 V < V_{in} < 1.5 V$, which corresponds to the region in which the pristine $MoSe_2$ FET is in its off-state, whereas the output signal is low for $3 V < V_{in} < 5 V$, which corresponds to the region in which the pristine $MoSe_2$ FET is in its on-state. The narrow (around 1.5 V) and symmetric window between the low and high logic states highlights the good performance of the inverter circuit. The differential curves of the tested inverters with the n-type FET are reported in Figure 5.4e, showing a gain around 0.10. This value, which is higher than the ratio between the output and input range, guarantees the regeneration of the logical states.[81,82] However, the logic states 1 and 0 are not associated with single voltage values, but rather with voltage ranges that can be defined through the noise margins. After rescaling the input voltages according to the equation $V_{in}^* = 0.02 \times V_{in}$ to make the input and output ranges equal, the noise margins for both high (NM_H) and low (NM_L) signals were determined (with reference to V_{dd} = 100 mV) as approximately 24-30% for NM_H and 22-27% for NM_L, thus satisfying the minimum requirement of exceeding 10% of V_{dd}.[20,83]

As a complementary architecture of the traditional resistive load inverter circuit, it can also be realised by employing a p-type transistor as the pull-up device and a resistor connected to the ground as the load, as schematized in the inset of Figure 5.4c. In this case, the driver transistor is the p-doped $MoSe_2$ FET electrically characterized previously, while different contact configurations across the homojunctions have been tested as the resistive load. Figure 5.4c presents a representative VTC, using the HJ transistor, illustrating the methodology used to determine the characteristic points of the VTC for the calculation of the noise margins. The VTCs of such inverter configurations are depicted in Figure 5.4d. In this case, V_T, calculated as previously explained, approaches 3 V for all the depicted curves. Figure 5.4f shows the gain of the inverter for the different configurations that remains around 0.08 (still higher than 0.02). With reference to V_{dd} = 100 mV, the noise margins are found to be approximately 13-23% for NM_H and 22-32% for NM_L, thus satisfying the minimum requirement of exceeding 10% of V_{dd}.

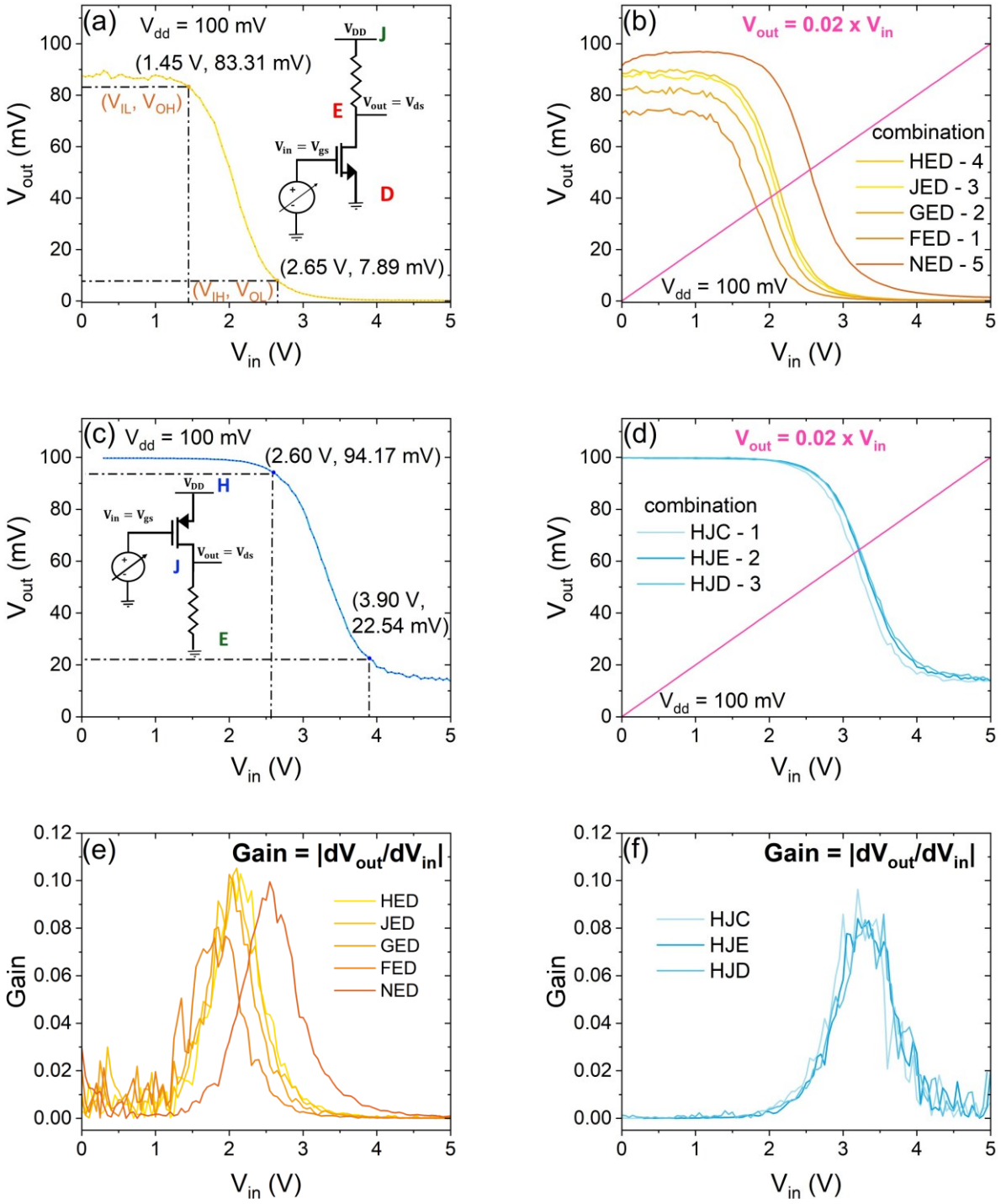


Figure 5.4: VTC curve of the resistive-load inverter with their characteristic points for the estimation of the noise margins for the circuit with (a) the homojunction and the ED n-type transistor and (c) with the HJ p-type transistor and the homojunction (in the inset: schematic of the corresponding resistive-load inverter circuits). VTC curves of the inverter circuits made with (b) the pristine $MoSe_2$ device and the heterostructure and (d) the p-doped $MoSe_2$ device and the heterostructure. (e-f) Gain of the different inverters implemented with the different combinations.

While resistive-load inverters demonstrate the basic logic functionality of our platform, they are limited by constant power dissipation in the on state and a restricted output voltage swing. To overcome these limitations, we implemented a CMOS architecture by pairing the pristine n-type

$MoSe_2$ FET with the interface-engineered p-type $MoSe_2$/CrOCl FET. This configuration exploits the balanced transport properties of both channels to achieve a more efficient logic transition. Figure 5.5a shows the schematic of the realized inverter circuit. Figure 5.5b shows the dynamical pulse measurements at V_{dd} = 100 mV, showing the simultaneous time evolution of V_{out} and V_{in}. In Figure 5.5c, the VTCs curves of the inverter at different V_{dd}, from 100 to 500 mV, are shown. The corresponding differential curves are depicted in Figure 5.5d, highlighting the gain of the inverters that are one order of magnitude higher than the ratio between the output and input ranges. The threshold voltage of the inverters, which are between 2.6 and 2.8 V, were determined as previously and are displayed in the inset of Figure 5.5d. The noise margins for the high and low signals are around 30% and 40% of V_{dd}, respectively. Figure 5.5e shows the VTC curve (V_{out} vs V_{in}^*) of the inverter with V_{dd} = 100 mV along with the butterfly graph for the visualization of the tolerance levels for both the high and low signals.[223,224] In addition, the total noise margin, defined as $NM_{TOT} = (NM_H + NM_L)/V_{dd}$ is plotted as a function of V_{dd} in Figure 5.5f.[225–227] Its value remains around 70%. It is important to highlight that, in CMOS inverters, the p- and n-type transistors are never strongly conducting at the same time, which minimises static power dissipation (on the order of 10^{-5} W) and guarantees both high noise margins and full logic-level swings.

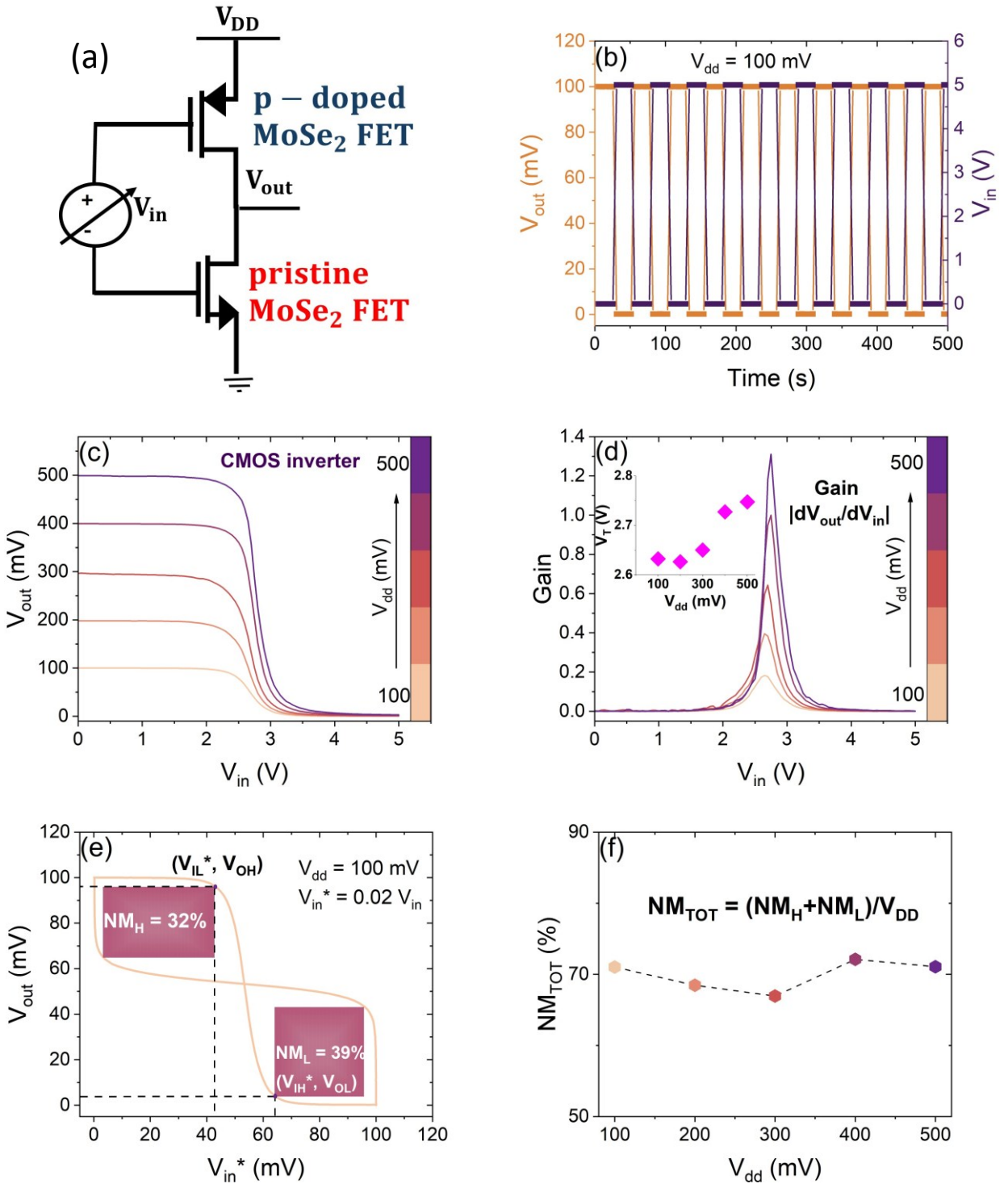


Figure 5.5: (a) Schematic of the CMOS inverter circuit using the $MoSe_2$ cFET. (b) Inverter pulses of the inverter obtained with the $MoSe_2$ cFET with V_{dd} = 100 mV. (c) VTC characteristics of the inverter based on the $MoSe_2$ cFET at different V_{dd} from 100 to 500 mV. (d) Gain of the inverter at different V_{dd} (in the inset: threshold voltage of the inverter as a function of V_{dd}). (e) V_{out} versus V_{in}^* plot of the inverter with V_{dd} = 100 mV along with the butterfly graph for the visualization of the tolerance levels for both the high and low signals. (f) Total noise margin of the inverter as a function of V_{dd}.

5.5 Floating-gate multilevel memory

Beyond its transistor operation, the $MoSe_2$/CrOCl device was further investigated in a floating-gate memory configuration, where non-volatile data storage is enabled through reversible charge

trapping and detrapping in the floating gate. The Au gate forms a high barrier with the hBN and SiO_2 layers, which facilitates charge retention in the floating gate after the voltage pulse is removed, as illustrated in the band diagram in Figure 5.6a.[228–230] In our initial characterizations, we restricted the V_{gs} sweeps to a narrow range, between -5 V and +5 V, to prevent potential gate dielectric damage and ensure device longevity. However, by extending the sweep to higher bias (±20 V), we demonstrate a substantial hysteresis loop (Figure 5.6b), confirming a high accumulation of charge and a wide memory window. Figure 5.6c illustrates the effect of charge trapping mechanism in the floating gate, showing the transfer curves of the p-doped $MoSe_2$ device before (dashed sky-blue line) and after the application of consecutive negative voltage pulses to the control gate electrode (solid lines in different shades of green). Negative pulses (≤ -15 V) induce hole tunnelling through the CrOCl/hBN stack into the floating gate, shifting the $MoSe_2$ transfer curve leftward. The stored charge can be released by grounding the Au electrode, resulting in the discharge of the floating gate (solid blue curve). Figure 5.6d shows the evolution of the transfer curve of the $MoSe_2$/CrOCl device after the application of a negative voltage pulse (- 18 V, green line) followed by a positive pulse (+ 18 V, dark yellow line). Positive pulses (≥ +15 V) let electrons accumulated in the CrOCl layer tunnel into the floating gate through the hBN flake, shifting the curve rightward; the effect is reproducible over multiple set/reset cycles. The shift of the transfer curve, and consequently of the threshold voltage, allows for the estimation of the stored charge density in the floating gate according to $n = (\Delta V_{th} C_{SiO2})/e$, where ΔV_{th} is the threshold voltage shift, C_{SiO2} is the capacitance of the SiO_2 blocking layer, and e is the elementary charge.[231,232] The density of stored holes after the -18 V pulse is estimated to be 2.9×10^{11} cm^{-2}.

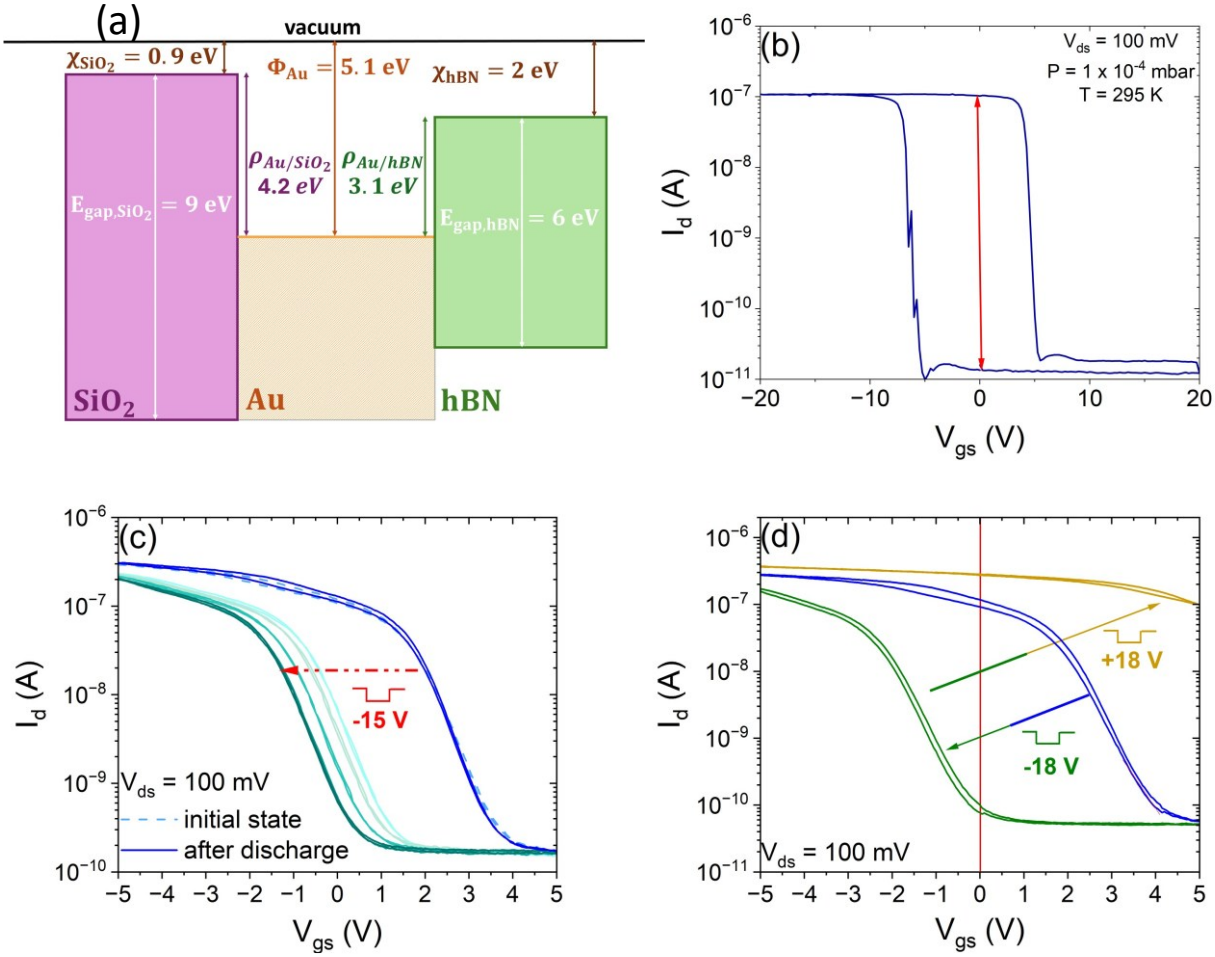


Figure 5.6: (a) Band diagram of SiO_2/Au/hBN stack. (b) Transfer characteristic of the $MoSe_2$/CrOCl FET sweeping V_{gs} between -20 V and +20 V. The current separation between the two levels at V_{gs} = 0 V suggests charge accumulation in the floating gate. This mechanism is used for the demonstration of the device as a floating gate non-volatile memory. (c) Transfer curves before (dashed blue-sky line) and after (solid green lines) the application of consecutive -15 V pulses to the control gate, showing charge trapping and detrapping in the floating gate. (d) Transfer curves showing charge trapping and detrapping in the floating gate after the application of negative and positive voltage pulses to the control gate electrode.

The memory operation of the analysed device is shown in Figure 5.7a. The channel current is monitored while applying gate voltage pulses. When a positive or negative voltage pulse is applied to the control gate electrode, electrons or holes tunnel through the tunnelling hBN layer, corresponding to the reset and set states of a memory device. At zero gate voltage, two well-separated stable states can be defined as the read states with a current memory window of 0.24 µA. The endurance of the $MoSe_2$/CrOCl floating gate memory device was evaluated by repeating set/reset cycles, with the memory window remaining stable for 1074 cycles, as shown in Figure 5.7b. The current margin between the states remains well-defined, with no significant degradation or closing of the memory window, confirming the robustness of the $MoSe_2$/CrOCl interface. The same device was also demonstrated as a three-level non-volatile memory by monitoring charge trapping in the floating gate through different successive control gate voltage pulses: first a -18 V gate pulse was applied, then a -20 V pulse, and then a +20 V pulse to release all the accumulated holes from the floating gate. All the pulses were alternated with 0 V pulses for the readout. Figure 5.7c shows the operation of the three-level floating gate memory device, with distinct current levels from 40 pA

to 0.3 µA at $V_{gs,\ Si\ gate}$ = 0 V; the endurance of the three-level memory over 50 cycles is shown in Figure 5.7d. Moreover, the same $MoSe_2$/CrOCl device was operated as a four-level non-volatile memory by alternating +20 V, -20 V, +16 V, and -16 V pulses with 0 V pulses for the readout. Figure 5.7e presents this operation, showing four distinct current levels within the same interval; the endurance of the four-level memory over 70 cycles is shown in Figure 5.7f.

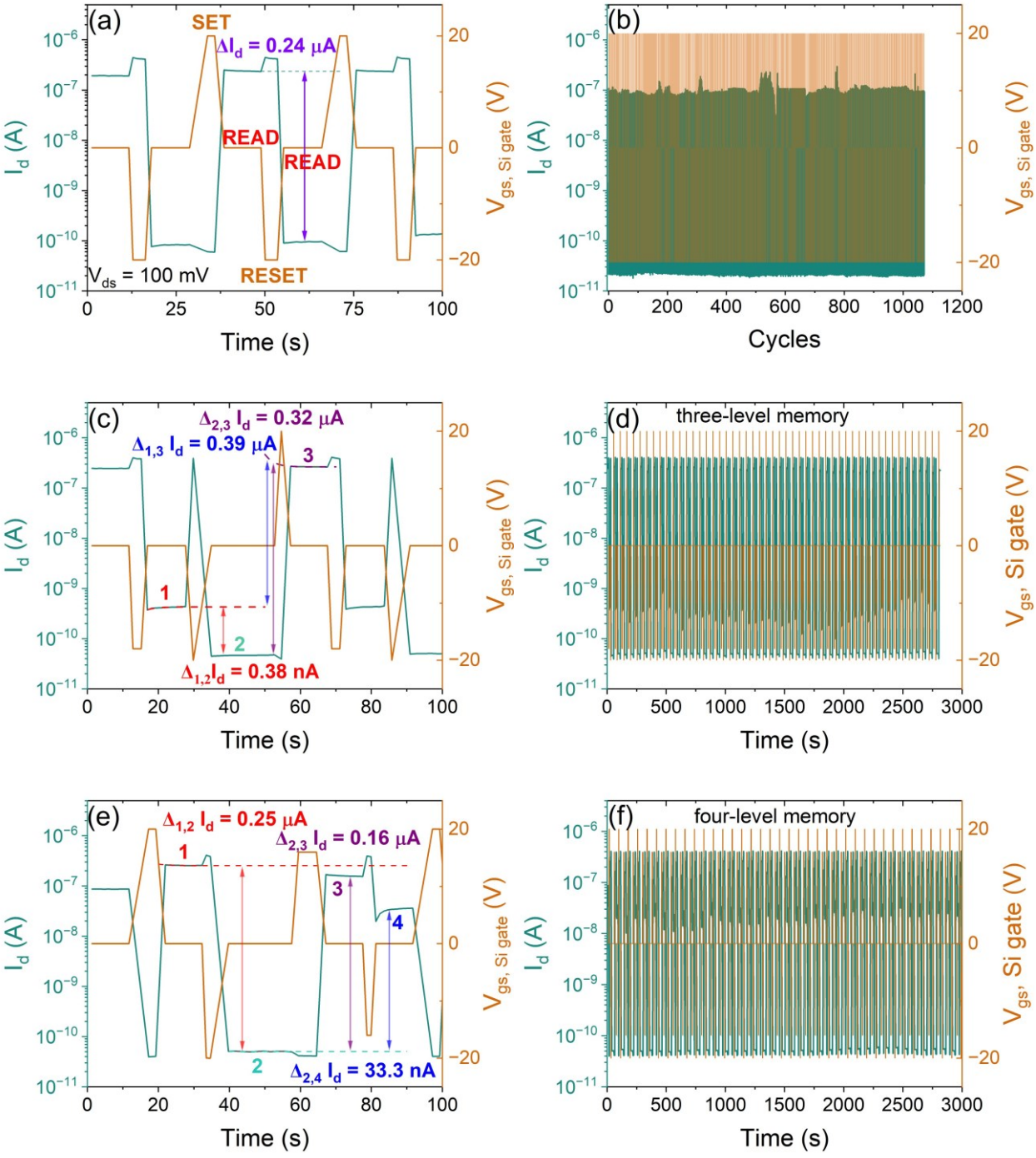


Figure 5.7: (a) Two-level operation (single cycle) and (b) endurance over more than 1000 set/reset cycles. (c) Three-level and (e) four-level operation obtained by applying programming pulses of different amplitudes. Endurance of the (d) three- and (f) four-level memory based on the p-doped $MoSe_2$ device.

The practical viability of multi-level memory architectures depends on the ability to define discrete conductance states that are not only clearly distinguishable but also exhibit long-term non-volatility and statistical consistency. To evaluate these critical performance metrics in our $MoSe_2$/CrOCl device, we performed a details analysis of the signal integrity, retention characteristics, and state distribution. As shown in Figure 5.8a-b, the various levels of the three- and four-level memory remain distinguishable with a high signal-to-noise-ratio. Additionally, to rigorously evaluate the non-volatile performance of the $MoSe_2$/CrOCl heterostructure, we conducted long-term retention measurements for all four programmed levels. As illustrated in Figure 5.8c-d-e-f, the four levels demonstrate exceptional stability over 45000 s with negligible current drift, confirming the reliability of the multi-bit storage.

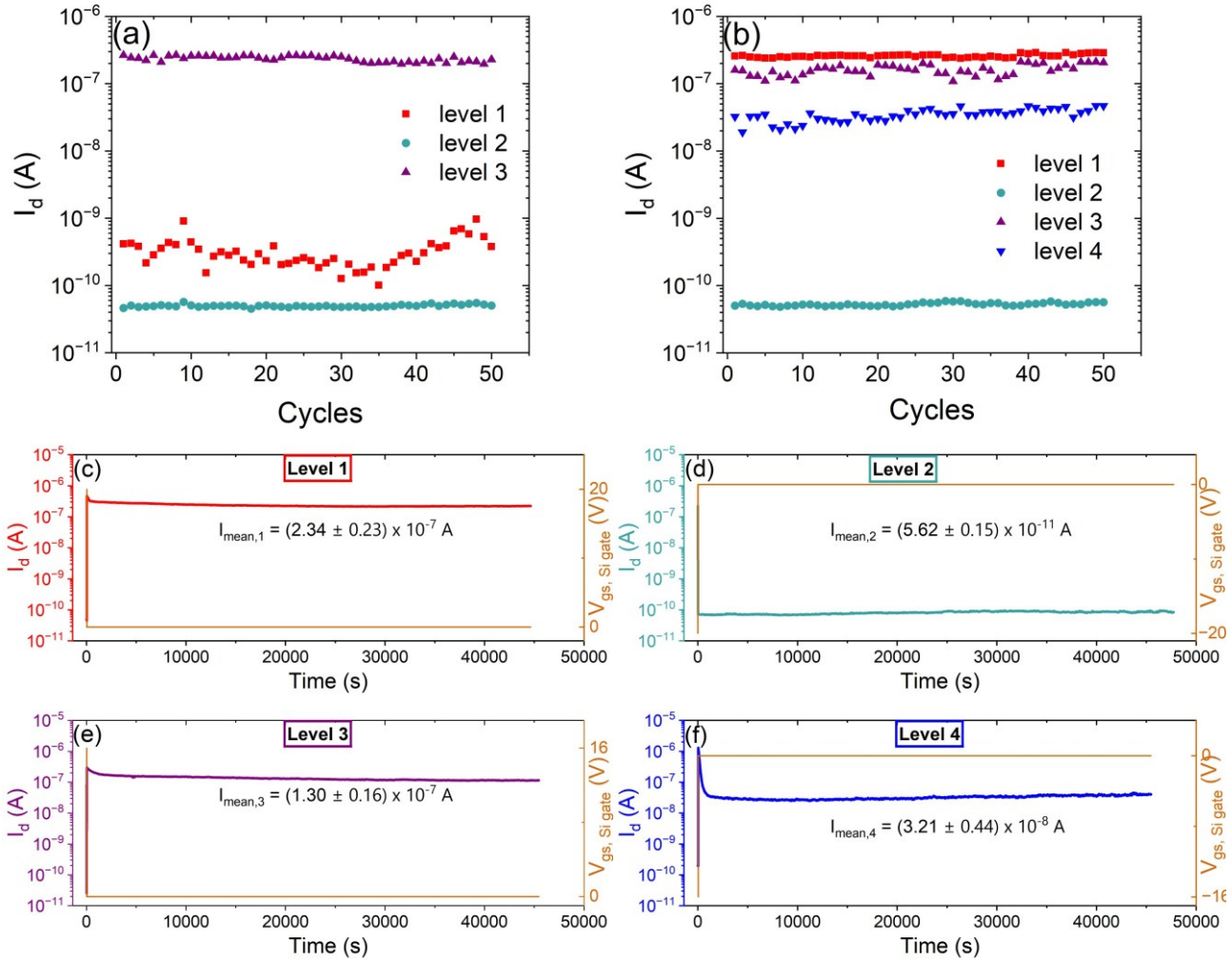


Figure 5.8: Distinguishability of current levels of the (a) three- and (b) four-level memory devices. (c-f) Stability and charge retention of the four levels of the non-volatile memory.

Reproducibility is confirmed by the state distribution histograms in Figure 5.9 with the normal distribution fits. The Gaussian fits, whose function is $f(x|\mu) = \frac{1}{\sigma\sqrt{2\pi}} e^{\frac{(-(x-\mu)^2)}{2\sigma^2}}$, allows us to quantify the separation between states and their distribution, calculating the mean (μ) and standard deviation (σ) for each level.

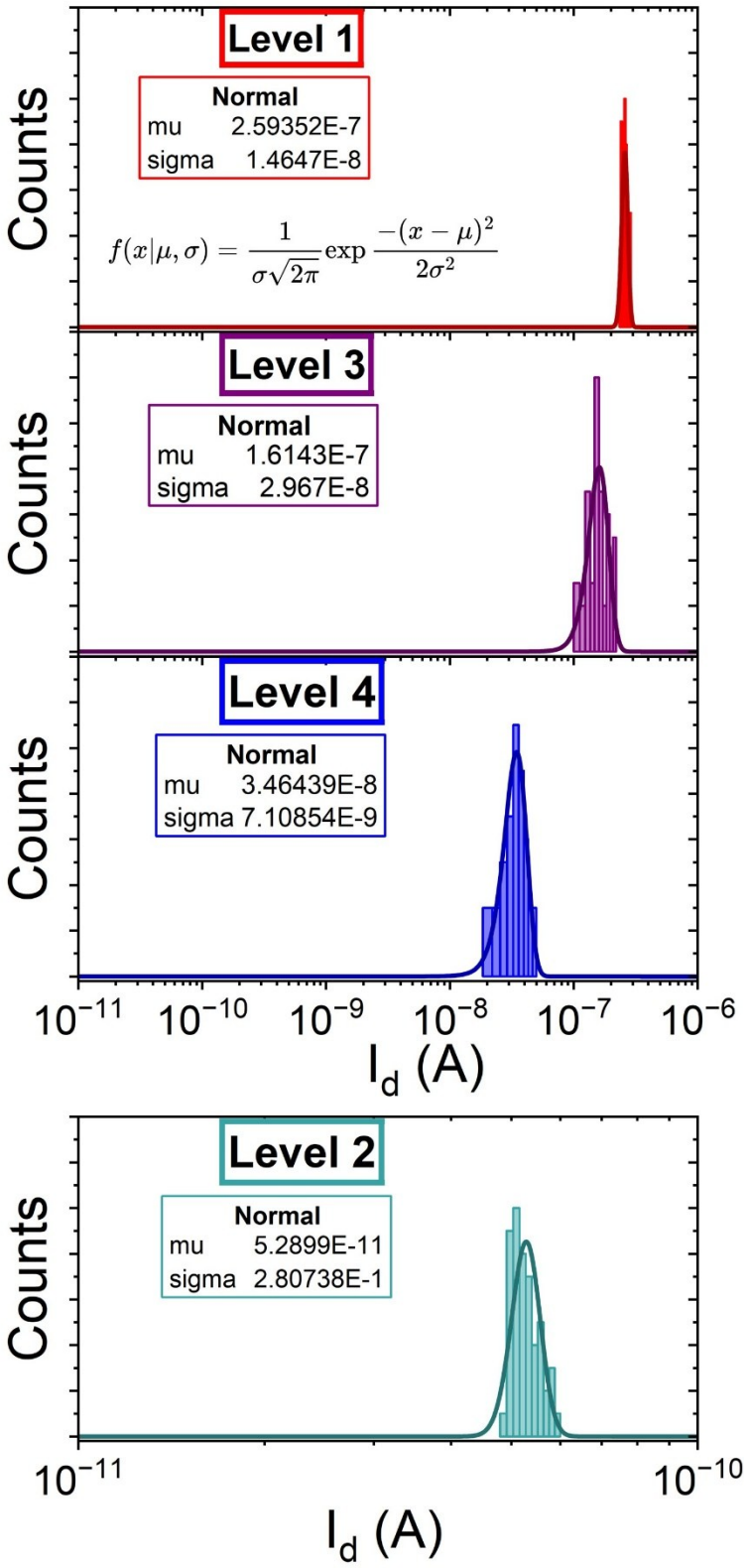


Figure 5.9: State distribution histogram of the four levels in the floating gate non-volatile memory. Solid lines represent Gaussian fits, with calculated mean (mu, μ) and standard deviation (sigma, σ) values indicating the stability and distinguishability of each state.

The $MoSe_2$/CrOCl device was also studied at low (77 K) and high (360 K) temperatures, both as a transistor and as a memory device. Figure 5.10a shows the transfer curves of the $MoSe_2$/CrOCl

device measured at a drain bias of 100 mV and temperatures of 77, 294, and 360 K. Current and gate modulation is dramatically suppressed at low temperature, while the switching behaviour is enhanced at elevated temperatures. Figure 5.10b-c illustrate the operation of the $MoSe_2$/CrOCl floating gate non-volatile memory device at 77 K and 360 K, respectively, under consecutive -20 V and +20 V set/reset pulses, with 0 V pulses applied in between at the control gate electrode for readout. At 77 K, the memory measurements exhibit narrower current windows (on the order of 10^{-11} A) and larger current fluctuations with respect to the ambient temperature performance. At 360 K, the memory operation is more stable, consistent with the behaviour observed in the transfer characteristics.

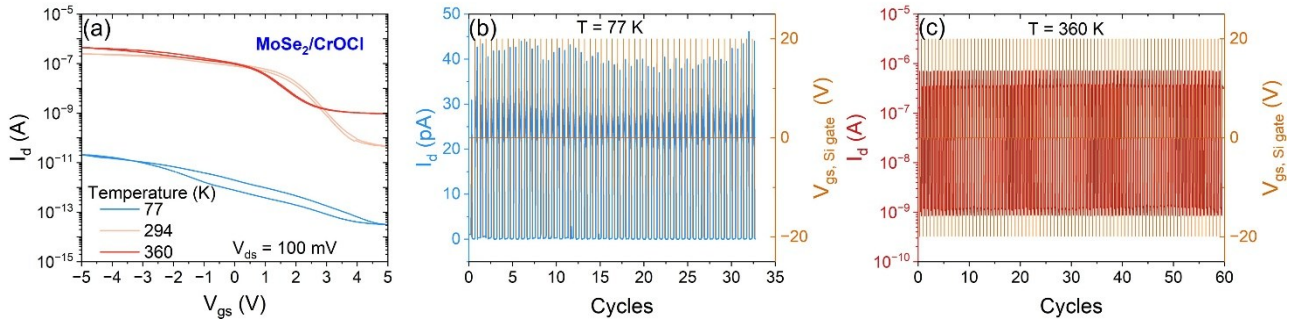


Figure 5.10: (a) Transfer curves of the p-doped $MoSe_2$ device at V_{ds} = 100 mV at 77 K (blue line), ambient temperature (pink line), and 360 K (red line). Multiple cycles of the two-level floating gate non-volatile memory device at (b) 77 K and (c) 360 K.

5.6 Artificial synaptic devices for neuromorphic computing

The rapid expansion of the Internet of Things and Artificial Intelligence has led to an unprecedented growth in dataset sizes, demanding a paradigm shift in data processing architectures to overcome the von Neumann bottleneck.[98] Recent advances illustrate that floating gate architectures based on 2D materials are uniquely positioned to meet this challenge. For instance, Zeng et al.[233] reported a vdW floating gate heterostructure based on black phosphorus/phosphorus oxides/tungsten diselenide ($BP/PO_x/WSe_2$) stack, exploiting naturally formed BP oxide as the dielectric and BP as the charge-trapping layer. This device showcased robust non-volatile memory metrics alongside essential synaptic features, such as bidirectional weight updates in both electrical and optoelectronic modes. Similarly, $MoSe_2$ has emerged as a promising candidate for neuromorphic hardware, exhibiting stable resistive switching and intriguing neuromorphic functions such as multilevel conductance, spike-timing-dependent plasticity, and image-edge extraction, highlighting their potential for energy-efficient neuromorphic computing.[234] This section investigated the application of our pristine $MoSe_2$ floating-gate structure as an artificial synaptic device.

The control gate modulation capacity and floating gate charge retention observed in $MoSe_2$ devices are potential for neuromorphic applications. A correspondence can be established between the elements of a biological synapse and those of the floating gate FET-based synaptic device. The pristine $MoSe_2$ FET operates as an artificial synapse. The presynaptic neuron is represented by the control and floating gate stack ($Si/SiO_2/Au/hBN$). In this stack, the presynaptic pulses are applied to the control Si gate, while the data retention is guaranteed by charge tunnelling through the hBN layer and its trapping at the hBN/Au interface. The hBN layer serves as the synaptic cleft, the gap across which signals are transmitted. Charge carriers trapped at the interface between the hBN layer

and the floating gate act as neurotransmitters, modulating the $MoSe_2$ channel conductance and thereby generating the postsynaptic signal. Thus, the 2D $MoSe_2$ flake mimics the postsynaptic membrane. A voltage pulse applied to the control gate electrode induces an electrical response, generating a spike in the drain current analogous to an excitatory post synaptic current (EPSC); similarly, an inhibitory postsynaptic current (IPSC) can be emulated by applying a voltage of opposite polarity, resulting in a decrease in the drain current. Since charge remains stored after the gate voltage pulse, the channel does not immediately return to its initial value. This charge retention and release emulate synaptic plasticity, with the degree of conductance modulation corresponding to the learning and memory functions of biological synapses.

To emulate synaptic behaviour and demonstrate long-term plasticity, consecutive -15 V pulses (200 in total) were applied to the control gate electrode, inducing LTP of the EPSC. This was followed by 100 consecutive +12 V pulses, which gradually restored the device to its baseline, simulating LTD.[100] The corresponding potentiation and depression curves of the pristine $MoSe_2$ FET as a synaptic device are shown in Figure 5.11a. Figure 5.11b-c show the dynamic measurement from which the current values for the potentiation and depression curves were extracted. The synaptic relative weight change is reported in Figure 5.11d for LTP (blue triangles) and LTD (red triangles). In contrast to potentiation, where consecutive pulses gradually accumulate charges leading to a progressive increase in synaptic weight, depression exhibits a sharp initial decrease followed by a weaker response to subsequent pulses. This behaviour suggests that the first positive pulse efficiently releases most of the stored charges, while the following pulses act mainly on residual states, thus restoring the current close to its baseline. The synaptic pristine $MoSe_2$ device reaches synaptic weight changes on the order of 100, which is very promising compared to other devices of the same category.[101,235] Furthermore, the tunability of the synaptic behaviour of the pristine $MoSe_2$ device was evaluated by applying different voltage pulses to the control-gate electrode, as reported in Figure 5.11e. In addition to the long-term plasticity discussed above, the endurance of the floating gate and the long-term stability of the current level after charge trapping/detrapping were further confirmed by overnight measurements (Figure 5.11f), which also reveal the expected exponential decay of the current.

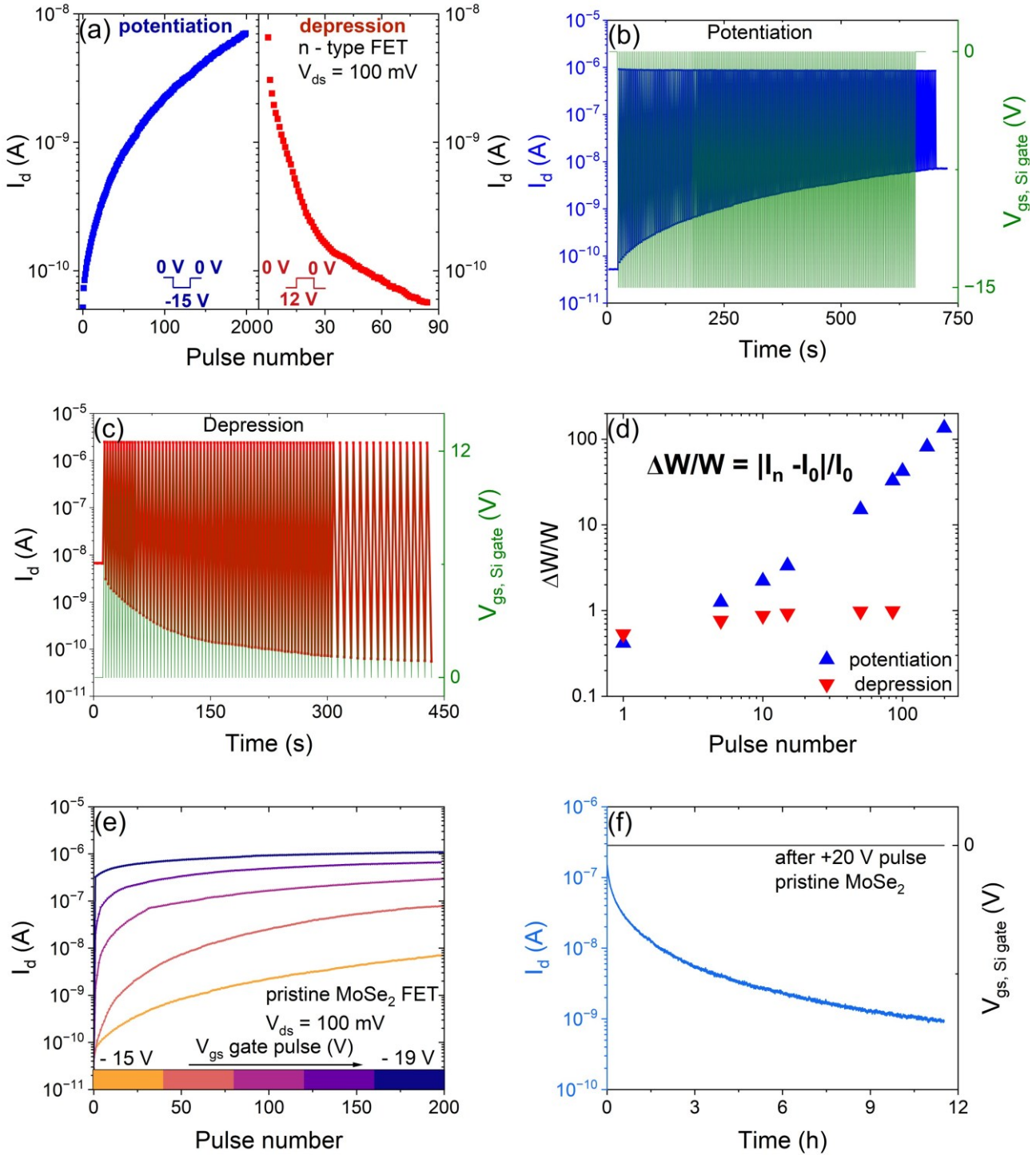


Figure 5.11: (a) Potentiation (blue dots) and depression (red dots) curves after the application of consecutive -15 V and 12 V pulses to the control gate electrode. Dynamic measurement of the synaptic functions of the $MoSe_2$ based device from which the current values for the (b) potentiation and (c) depression curves were extracted. (d) Synaptic weight as a function of pulse number. (e) Potentiation curves of the synaptic pristine $MoSe_2$ device at different voltage pulses applied on the control-gate electrode. (f) Overnight stability of charge retention and exponential decay of the store charge after a positive (+20 V) voltage pulse.

5.7 Optoelectronic characterization $MoSe_2$, p-doped $MoSe_2$, homojunction

To further evaluate the functionality of the $MoSe_2$ platform, its optoelectronic response was investigated under white light and monochromatic illumination. It should be noted that while the

logic and neuromorphic operations discussed in the previous sections focus on devices ED and HJ, the fundamental optoelectronic characterization was performed on devices AB (pristine $MoSe_2$) and FN ($MoSe_2$/CrOCl).

The optoelectronic performance of both the pristine $MoSe_2$ and the p-doped $MoSe_2$ devices is summarized in Figure 5.12.

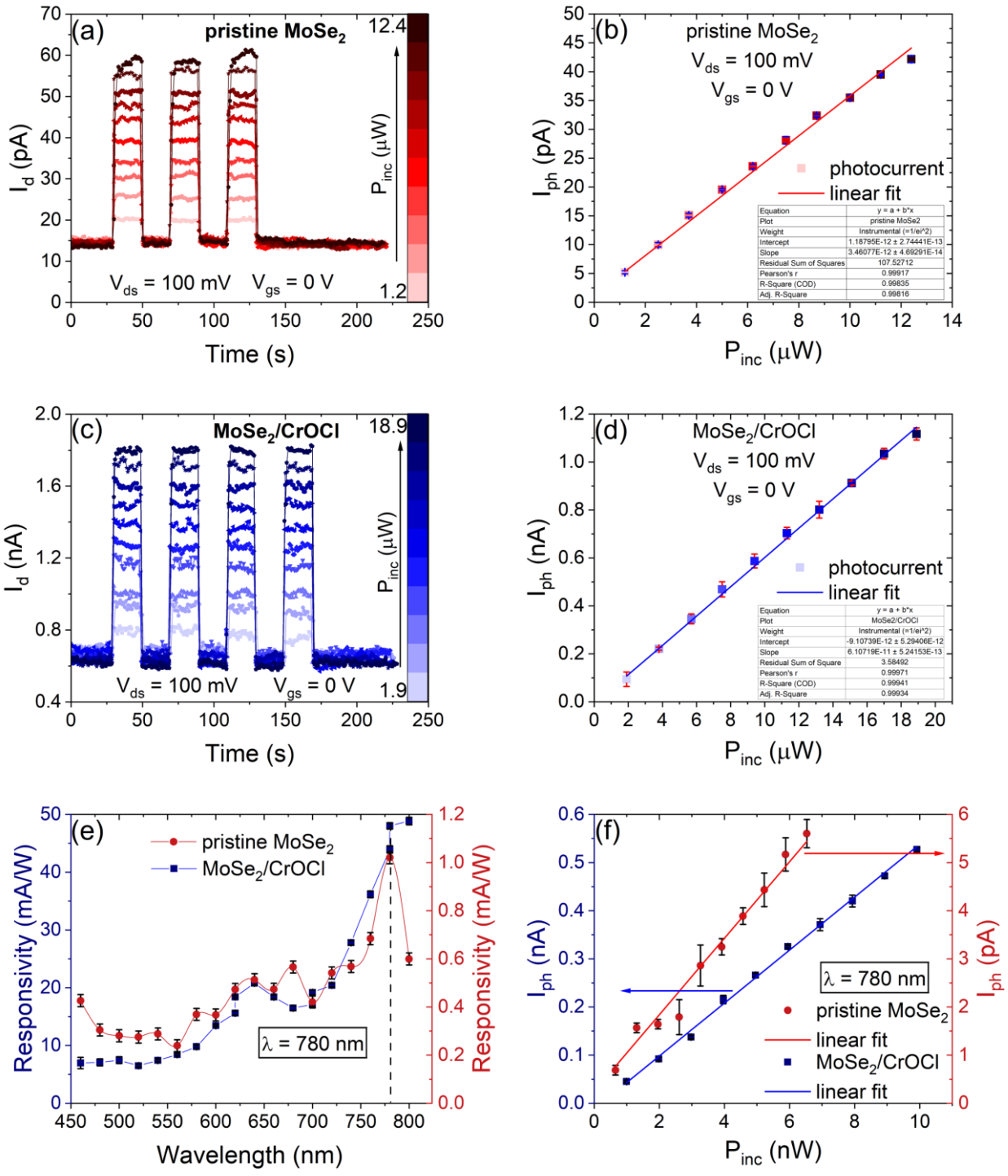


Figure 5.12: Optoelectronic characterization of the $MoSe_2$ platform. 20-second white light pulses at different incident optical power at V_{ds} = 100 mV and V_{gs} = 0 V of the (a) pristine and (c) p-doped $MoSe_2$ device. Photocurrent as a function of the incident optical power with linear fit for the (b) pristine and (d) p-doped

$MoSe_2$ device. (e) Wavelength-dependent responsivity of the pristine (red circles, right axis) and p-doped (blue squares, left axis) $MoSe_2$ devices. The responsivity peak value is around 780 nm. (f) Photocurrent as a function of the incident optical power at λ = 780 nm with linear fits for the pristine (red circles, right axis) and p-doped (blue squares, left axis) $MoSe_2$ photodetector.

Figure 5.12a-c display the time-resolved measurements for the pristine and p-doped $MoSe_2$, respectively, under white light illumination at different incident optical powers. Both configurations demonstrate fast, stable and reproducible switching behaviour, without persistence of the photoconductivity. The dependence of the photocurrent on the incident laser power is shown in Figure 5.12b-d for the pristine and p-doped $MoSe_2$, respectively. Both devices exhibit a clear linear scaling of I_{ph} with power, I_{ph} α P_{inc}. this linear characteristic is highly desirable for practical photodetectors as it ensures a constant responsivity, facilitating predictable signal processing across varying light intensities. Furthermore, the calculated photosensitivity, defined as the ratio between the photocurrent and the dark current, I_{ph}/I_{dark}, is on the order of 10^1. This consistent ratio across the different material regions confirms that the interfacial coupling with CrOCl preserves the fundamental photodetection capabilities of the $MoSe_2$ while enabling the p-type conduction necessary for the advanced logic and memory applications discussed in the previous sections.

To conclude the optoelectronic characterization of the $MoSe_2$ devices, the spectral photoresponse was investigated in the 460-800 nm range. Figure 5.12e presents the wavelength-dependent responsivity of the pristine (right axis, red circles) and p-doped (left axis, blue squares) $MoSe_2$ devices. Both spectra exhibit a characteristic peak centred at approximately 780 nm, consistent with the excitonic absorbance peaks reported in literature.[236,237] The peak responsivity values reach up to 50 mA/W, demonstrating that the interfacial coupling with CrOCl does not significantly degrade the intrinsic light-harvesting efficiency of the $MoSe_2$ flake. To evaluate the device performance under resonant excitation, the power-dependent photocurrent was measured specifically at the peak wavelength of λ = 780 nm, as shown in Figure 5.12f. Even at this optimized wavelength, both the pristine and p-doped regions maintain a robust linear dependence of the photocurrent on the incident optical power. This consistent linearity at the peak responsivity wavelength further confirms the suitability of these devices for high-fidelity photodetection.

The optoelectronic characterization of the homojunction formed between pristine and p-doped $MoSe_2$ is presented in Figure 5.13. Figure 5.13a displays the time-resolved measurements of the homojunction under white light illumination at different incident optical powers. The device exhibits highly reproducible and stable switching characteristics, with the photocurrent magnitude scaling directly with the illumination intensity. The lack of significant signal drift or persistent photoconductivity at these powers indicates a clean interface with low trap density. The photocurrent as a function of the incident optical power is plotted in Figure 5.13b. A robust linear dependence is observed. This linearity is a key metric for photodetectors, as it translates to a constant responsivity and simplifies signal processing for integrated circuits.

The spectral photoresponse of the homojunction is examined in Figure 5.13c. The responsivity spectrum covers the visible to near-infrared range, with a discernible peak remaining at approximately 780 nm. While this excitonic feature is less pronounced than in the single region devices, likely due to spectral broadening induced by the interfacial coupling with CrOCl and the multilayer nature of the $MoSe_2$ flake, it confirms that the $MoSe_2$ maintains its intrinsic excitonic transitions even after the doping process. Finally, to assess the performance under resonant

excitation, Figure 5.13d shows the power-dependent photocurrent measured specifically at the peak wavelength of λ = 780 nm. The data confirms that even at the wavelength of maximum absorption, the pristine/p-doped $MoSe_2$ homojunction maintains its linear behaviour. This consistent scaling at the peak responsivity wavelength highlights the reliability of the CrOCl-induced homojunction for high-performance photodetection applications.

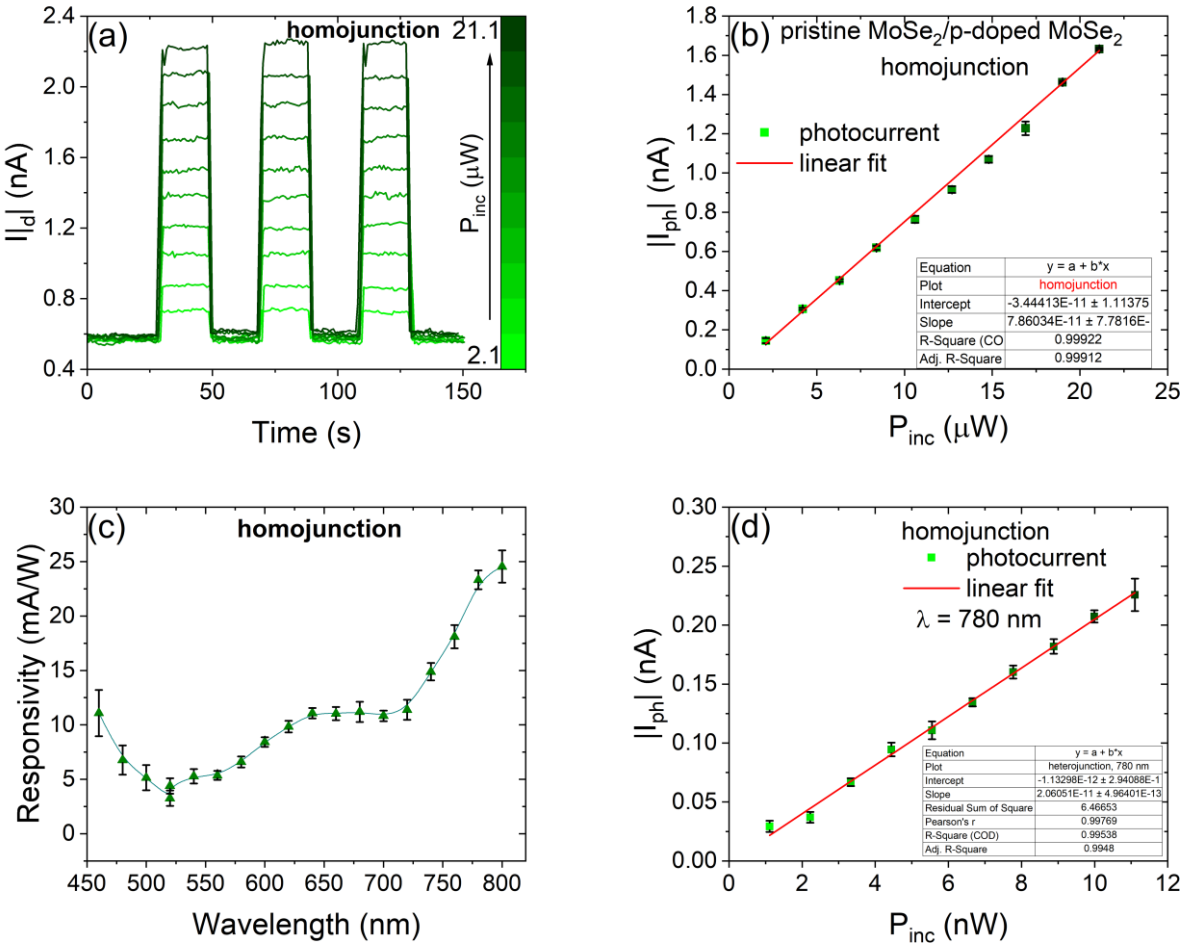


Figure 5.13: Optoelectronic characterization of the $MoSe_2$ homojunction. (a) 20-second white light pulses at different incident optical power of the $MoSe_2$ homojunction. (b) Photocurrent as a function of the incident optical power with linear fit. (c) Wavelength-dependent responsivity of the $MoSe_2$ homojunction. The peak responsivity is still present at λ = 780 nm. (d) Photocurrent as a function of the incident optical power at λ = 780 nm with linear fit.

The existence of a robust built-in electric field at the $MoSe_2$/CrOCl homojunction interface allows for device operation in self-powered mode. In this regime, photogenerated electron-hole pairs are spatially separated by the internal field, generating a photovoltaic current without the need for an external bias. As shown in Figure 5.14a, the I-V characteristics under white light illumination exhibit a clear rightward shift as the incident optical power increases. To confirm the reliability of this self-powered detection, time-resolved measurements were performed at V_{ds} = 0 V and V_{gs} = 0 V (Figure 5.14b). The device demonstrates sharp, reproducible switching between the dark and light states, proving that the homojunction can function as an autonomous light sensor. Finally, the extraction of short-circuit current I_{sc} is plotted against the incident optical power in Figure 5.14c. The data follows

a strict linear fit, confirming that the carrier collection efficiency remains constant across the investigated power range, which is ideal for quantitative photodetection applications.

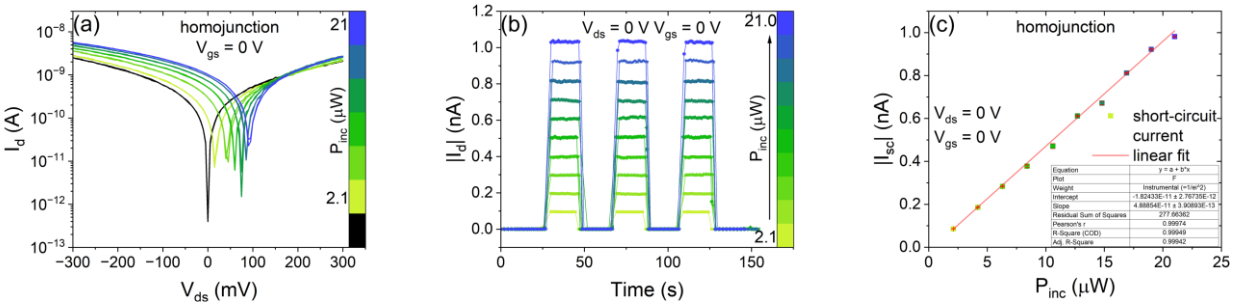


Figure 5.14: $MoSe_2$ homojunction operation in self-powered mode. (a) I-V characteristics at V_{gs} = 0 V under white light at different incident optical powers. The curves exhibit a rightward shift with increasing power. (b) 20-second white light pulses at V_{ds} = 0 V and V_{gs} = 0V. (c) Short-circuit current as a function of the incident optical power for the $MoSe_2$ homojunction with linear fit.

6. ONE-DIMENSIONAL DEVICES

While 2D materials offer an ideal platform for flexible and transparent electronics, the reduction of dimensionality to the one-dimensional (1D) limit introduces a new set of physical phenomena governed by quantum mechanical principles. These include size-dependent excitation and emission, quantized conductance, and ballistic charge carrier transport. Specifically, 1D structures offer superior electrostatic control compared to their bulk counterparts, making them ideal candidates for FETs where the gate-all-around geometry can minimize short-channel effects. In this chapter, we extend the investigation of low-dimensional systems by exploring WS_2 nanotubes and InAs nanowires. The move from planar WS_2 sheets to cylindrical nanotubes allows for the study of curvature-induced strain and its impact on the electronic bandgap. Furthermore, InAs nanowires, characterized by a high charge carrier mobility, provide an interesting platform for logic applications, such as resistive-load inverters investigated in this chapter.

6.1 WS_2 nanotubes in field-effect transistors

While 2D TMDs like WS_2 have gained significant attention for their electrical and optoelectronic properties, the transition to 1D tubular geometries introduces a new paradigm of physical phenomena. WS_2 nanotubes (NTs) combine the unique properties of this semiconductor material with the advantages of tubular geometries, making them highly suitable for several applications, such as FETs, photodetectors, and sensors.[238] As demonstrated for carbon nanotubes, the hollow geometry and curvature-induced strain of nanotubes, accompanied with the loss of the crystalline symmetries, can significantly influence charge transport, enabling novel device functionalities.[239–241] As demonstrated in Section 4.2, devices based on 2D flakes of WS_2 typically exhibit n-type conduction at ambient pressure. To achieve ambipolar conduction, Y. Li et al.[242] implanted phosphorus ions into WS_2, enabling balanced electron and hole transport. More generally, various strategies such as contact engineering, doping, and electrostatic gating have been employed to enhance hole conduction and achieve ambipolarity in n-type WS_2 flakes.[243] On the other hand, ambipolar conduction has been reported in WS_2 NTs[244,245], which is advantageous for CMOS applications, as it enables the integration of both n- and p-type operations within a single material system. G. Lee et al.[246] leveraged the ambipolar behaviour of WS_2-based devices to demonstrate a CMOS-like inverter with a gain of 78. In this section, we report on the fabrication and electrical and optoelectronic characterization of a single WS_2 NT-FET at ambient pressure and temperature, highlighting its potential for practical applications due to its long-term air stability. Furthermore, the device's response to white light has been explored both at a fixed drain voltage (2 V) and in self-powered mode.

6.1.1 Device fabrication and material characterization

WS_2 NTs were synthesized through a two-step reaction process under an atmosphere of H_2 and H_2S gases using N_2 as a carrier gas.[247] They were dispersed onto Si/SiO_2 substrates for the realization of FETs. In Figure 6.1a, a transmission electron microscopy (TEM) image of a single WS_2 NT is reported, showing its inner structure with an outer radius of 19 nm. The high quality of the WS_2 NT is evidenced by the Raman spectrum, displayed in Figure 6.1b, with the WS_2 characteristic $E_{2g}{}^1$ and A_{1g} modes at 350 cm^{-1} and 420 cm^{-1}, respectively, accordingly with the 2D WS_2 flake.[174] Thermally evaporated Ti/Au (20/120 nm) metal contacts were patterned through e-beam lithography and used to contact a single WS_2 NT. Figure 6.1c shows an optical image of the fabricated device. The schematic of the

WS_2 NT-device is depicted in Figure 6.1d, showing the electrical measurement setup. The bottom of the highly doped Si substrate was covered by conductive silver paste and used as a gate electrode. The 500 nm-thick oxide layer enables the investigation of channel current modulation at high gate voltages, up to 100 V.

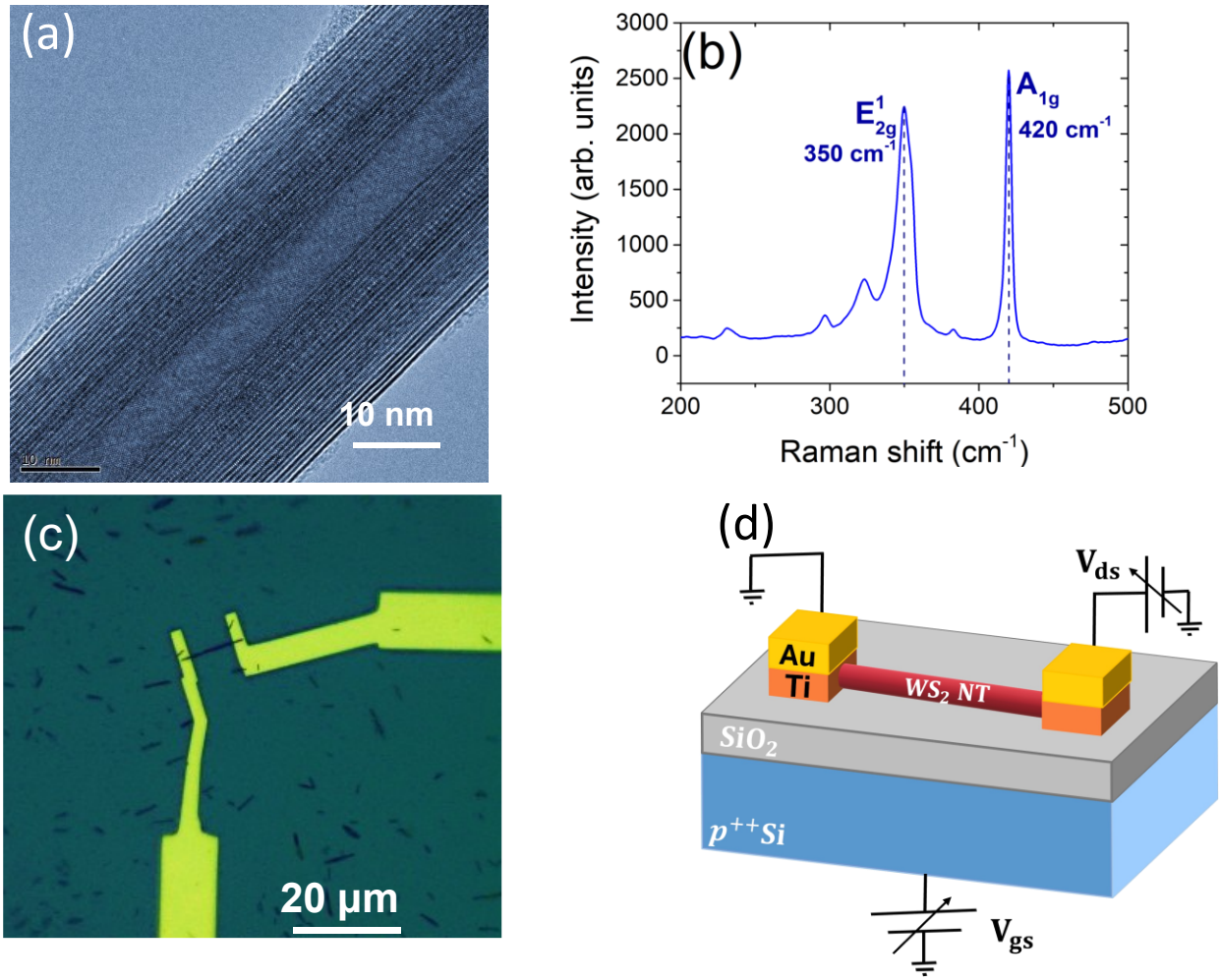


Figure 6.1: (a) Blue-contrast TEM image of a WS_2 NT. (b) Raman spectrum of the WS_2 NT. (c) Optical image of a single WS_2 NT-device. (d) Schematic of the structure of the device with the electrical measurement setup.

6.1.2 Electrical characterization

Figure 6.2a shows the I-V characteristic of the single WS_2 NT-FET measured under ambient pressure and with a grounded gate with V_{ds} ranging from -2 to 2 V. The slightly non-linear behaviour suggests non-Ohmic contact between Ti and the NT, with a low Schottky barrier of approximately 0.2 eV.[205] Figure 6.2b shows the transfer curve with V_{ds} = 500 mV. The gate voltage is swept from 100 to -100 V (reverse branch), and back to 100 V (forward branch). The transfer curve indicates a p-type conductive behaviour, characterized by higher currents at negative V_{gs} with the off-state of the transistor at positive V_{gs}. The hysteretic behaviour of the transfer curves can be attributed to trapped charges at the NT/SiO_2 interface, as well as intrinsic defects in the material, mainly due to sulphur vacancies.[119,248] Furthermore, since the measurement was performed at ambient pressure, water and oxygen molecules tend to adsorb onto the NT surface, contributing to an increase in the hysteresis width. The maximum charge carrier mobility, equal to 0.17 $cm^2\ V^{-1}\ s^{-1}$, was calculated

using the usual formula with C_{ox} equal to the gate oxide capacitance of the structure. C_{ox} was estimated using the "metallic cylinder on an infinite metal plate" approximation[20,249–251] and was found to be C_{ox} = 2.71 x 10^{-11} F/m. The red line of Figure 6.2b indicates the linear fit of the linear region of the transfer characteristic for the extraction of the transconductance.

The transfer curves at different V_{ds}, ranging from 0.25 to 2 V in steps of 0.25 V, are shown in Figure 6.2c. The WS_2 NT-device transitions from p-type to ambipolar conduction as V_{ds} increases to 0.75 V. The charge carrier mobility, calculated as previously described, for electron and hole conduction as a function of drain voltage is reported in Figure 6.2d: the hole mobility remains approximately constant at approximately 0.2 $cm^2 V^{-1} s^{-1}$, while the electron mobility increases from 0.02 $cm^2 V^{-1} s^{-1}$ at V_{ds} = 0.75 V to 0.13 $cm^2 V^{-1} s^{-1}$ at V_{ds} = 2 V.

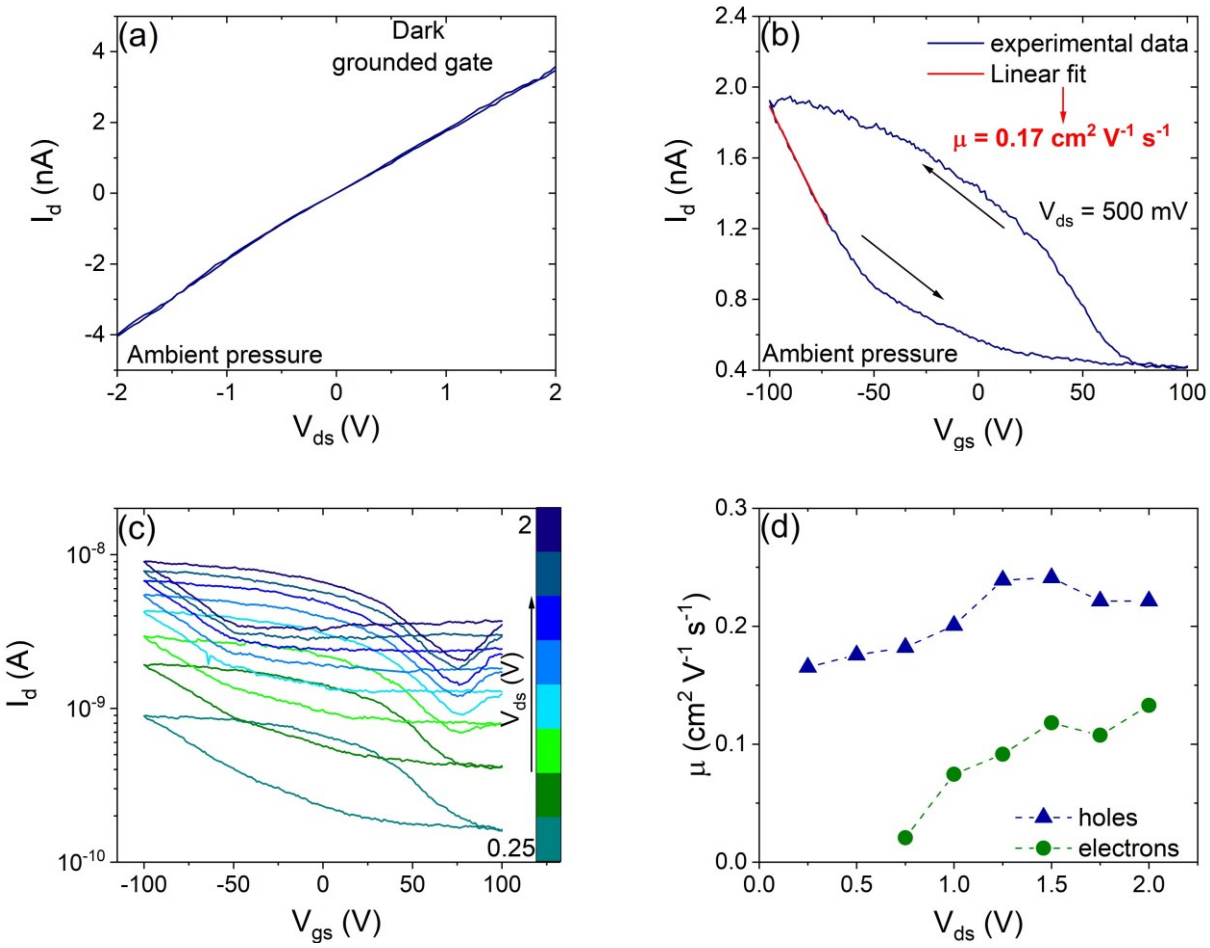


Figure 6.2: Electrical measurements of the WS_2 NT-FET under dark conditions and ambient pressure. (a) I-V characteristic with the gate grounded. (b) Transfer curve at V_{ds} = 500 mV with linear fit (red line) of the linear region for the extraction of the charge carrier mobility. (c) Transfer curves at different V_{ds}, ranging from 0.25 to 2 V in steps of 0.25 V. (d) Mobility of the holes (blue triangles) and electrons (green circles).

The gate modulation of the WS_2 NT-device was extensively investigated. Figure 6.3a shows the output curves at different fixed V_{gs} from -100 to 100 V in steps of 20 V, on a semilogarithmic scale. At V_{ds} < 1 V, the drain current increases as the gate voltage becomes more negative, as expected for p-type conduction. At V_{ds} > 1 V, the drain current starts increasing as the gate voltage exceeds 40 V. The analysed data clearly confirm the ambipolar conduction in the WS_2 NT-FET when a high V_{ds} is

applied. Figure 6.3b displays the drain current at V_{ds} = ±2 V as a function of gate voltage, showing the increase in drain current at positive drain voltage as the gate voltage rises from 40 to 100 V. Figure 6.3c shows a series of transfer curves at V_{ds} = 2 V at different gate voltage ranges, from 20 to 100 V in steps of 20 V. As the gate voltage range increases, both the electron and hole currents increase. In Figure 6.3d (right axis, coloured circles connected by a dotted red line), it can be observed that the ratio between the current values at the minimum and maximum V_{gs} for each ΔV_{gs} range increases as the gate voltage range expands up to 100 V. The hysteresis width of the transfer curves is defined as the voltage difference between the V_{gs} values corresponding to the minimum drain current in the forward and reverse branches of the transfer characteristics. Its dependence on the gate voltage range is depicted in Figure 6.3d on the left axis (coloured triangles connected by a dotted blue line). The hysteresis width of the transfer curves increases from 1 V when V_{gs} is swept between ±20 V to 115 V when V_{gs} is swept between ±100 V. Indeed, as the gate voltage range increases, the sweep time becomes longer, leading to greater carrier trapping at the WS_2 NT/SiO_2 interface and resulting in a larger hysteresis width in the transfer curves.[10]

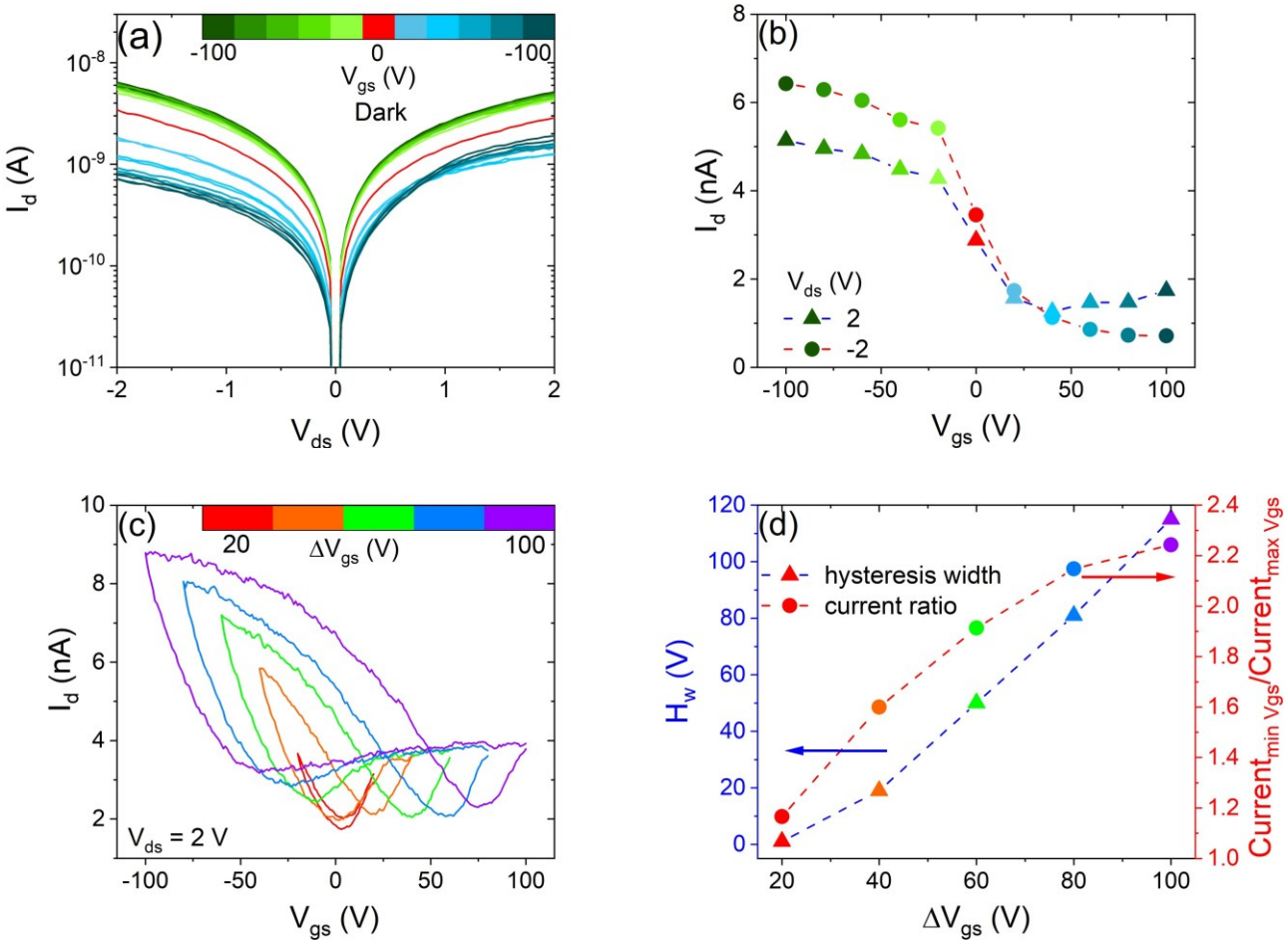


Figure 6.3: Gate modulation of the WS_2 NT-FET under dark conditions. (a) Output curves at different V_{gs}, ranging from -100 to 100 V in steps of 20 V. (b) Drain current at V_{ds} = ± 2 V as a function of gate voltage. (c) Transfer curves at V_{ds} = 2 V with V_{gs} sweeping across different ranges from 20 to 100 V. (d) Hysteresis width (left axis, coloured triangles connected by a dotted blue line) of the transfer curve and current ratio of the extreme points (right axis, coloured circles connected by a dotted red line) of the transfer curves as a function of gate voltage range.

6.1.2 Optoelectronic characterization

Figure 6.4a shows the output curves of the WS_2 NT-FET at fixed V_{gs}, ranging from -100 to 100 V in steps of 20 V, under white light illumination with an incident laser power of 80 nW. At $V_{ds} < 1$ V , the device still exhibits p-type conduction, while at $V_{ds} \geq 1$ V, ambipolar conduction emerges. This behaviour is more evident in the transfer curves at different V_{ds} values, ranging from 0.5 to 2 V in steps of 0.5 V, as shown in Figure 6.4b. A series of 10 seconds long light pulses at different incident laser powers, from 16 to 80 nW, is reported in Figure 6.4c. The linear dependence of the photocurrent as a function of the incident laser power is shown in Figure 6.4d. This is a highly desirable feature for practical photodetectors. The WS_2 NT-device was tested in self-powered mode, showing its response to light pulses in short- and open-circuit conditions. Figure 6.4e-f present a series of light pulses under white illumination at an incident laser power of 80 nW at $V_{ds} = 0$ V and $I_d = 0$ A, respectively. This photovoltaic effect is characterized by a short-circuit current equal to 2.6 pA and an open-circuit voltage of approximately 3 mV. The variation in Schottky barrier heights at the Ti contacts could be the cause of this photovoltaic effect.[205,252]

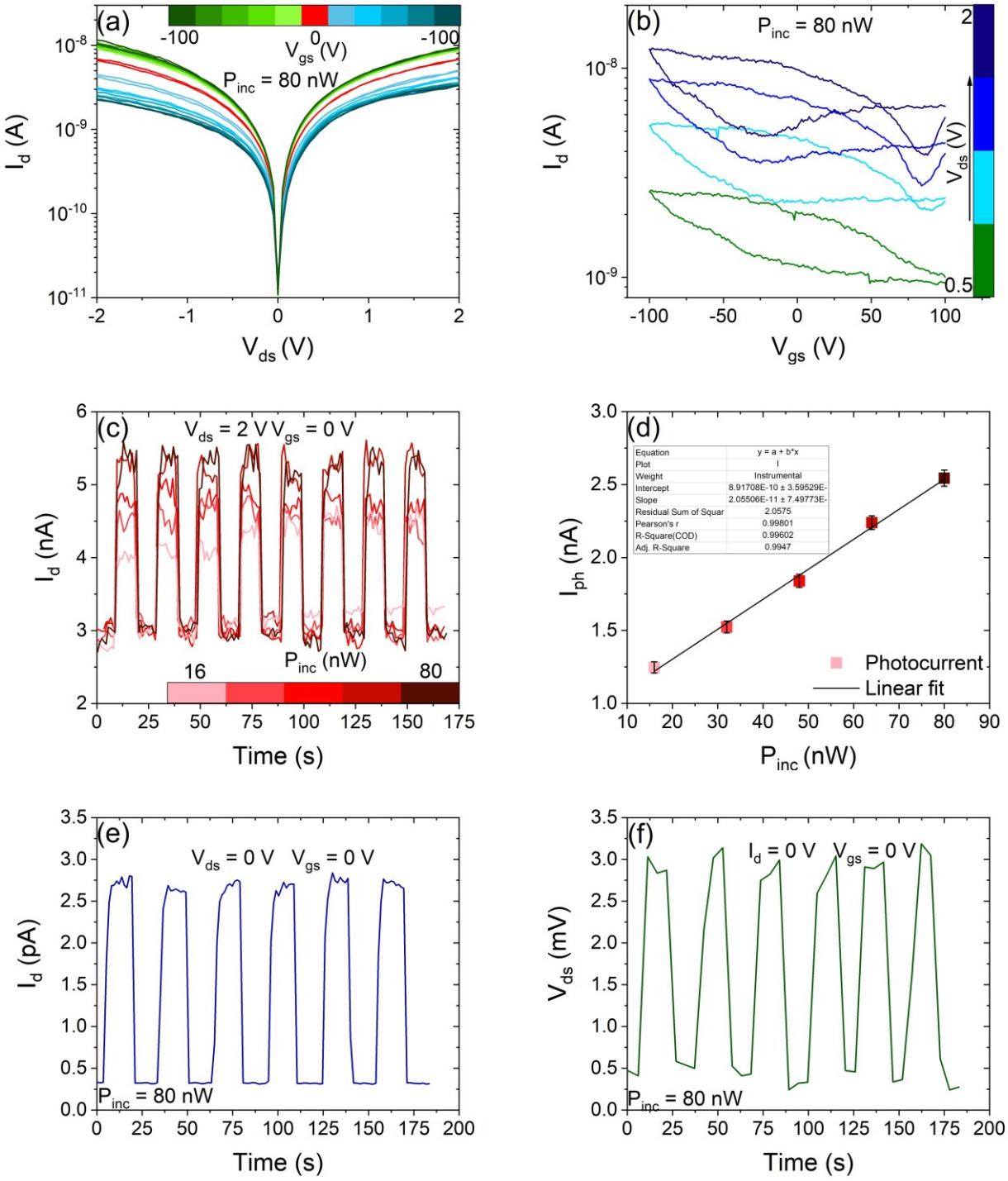


Figure 6.4: Optoelectronic characterization of the WS_2 NT-FET under white light illumination. (a) Output curves at different V_{gs}, ranging from -100 to 100 V in steps of 20 V, under illumination at an incident laser power of 80 nW. (b) Transfer curves at different V_{ds}, from 0.5 to 2 V in steps of 0.5 V, under illumination at an incident laser power of 80 nW. (c) Light pulses of 10 s at V_{ds} = 2 V and V_{gs} = 0 V at different incident laser powers from 16 to 80 nW. (d) Photocurrent as a function of incident laser power. (e) Photogenerated current at V_{ds} = 0 V under illumination at 80 nW. (f) Photogenerated voltage at I_d = 0 A under illumination at 80 nW.

6.2 InAs nanowires in field-effect transistors

Nanowires (NWs) have been obtained from several materials, including III-V semiconductor compounds, most of which are characterized by a direct bandgap, low electron effective mass and high carrier mobility.[253,254] Indium Arsenide (InAs) presents a narrow bandgap that ranges from 0.354 eV in the zincblende (ZB) to 0.477 eV in the wurtzite (WZ) structure at room temperature.[255] Such a bandgap makes InAs NWs good candidates for mid-wave infrared photodetection.[256,257] InAs NWs are ideal channels in FETs with high switching speeds and low power consumption due to the low contact resistance and high electron mobility.[258,259] They are good candidates to push forward Si-based electronics because they can easily grow directly on Si substrates without damaging the devices.[260] C. Thelander et al.[261] fabricated multiple tunnel junction (MTJ) memories made of junction arrays of InAs quantum dots and InP barriers incorporated at the end of InAs NWs, where the metal seed particles acted as storage nodes. The storage of few-electrons in these epitaxially grown semiconductor NWs was demonstrated, exploiting the hysteresis in the charging/discharging of the storage node as a function of the writing voltage. InAs NWs-based devices have been mostly used in the CMOS technology [262,263] as n-type transistors due to InAs NWs electron mobility higher than 4000 $cm^2\ V^{-1}\ s^{-1}$ at room temperature.[258,264] Single n-InAs/p-GaSb heterostructure NWs were used to realize CMOS-inverters, achieving a gain up to 10 applying 1 V as power supply.[265] In literature, a few works deal with temperature dependent electrical properties of FETs with single InAs NWs, mainly focusing on the temperature interval below 200 K. N. Gupta et al. [266] investigated the electrical transport in the temperature range from 10 to 200 K, revealing a more evident change in parameters above 50 K. In particular, the electron mobility changes its temperature dependence at 50 K. Because of the transport across severely confined 1D subbands in NWs, InAs NW-FET transfer characteristics exhibit step-like patterns below 50 K. It is also observed that the low field magnetoconductance depends on temperature. At 8 K, a spin-orbit interaction causes a modest antilocalization effect, which is shown by a negative magnetoconductance. As the temperature rises, the antilocalization effect gradually disappears, reaching a positive magnetoconductance at 25 K.[267]

In this section, we present the fabrication and electrical characterization of back-gated FETs based on single InAs NWs, exploring their performance across a broad thermal range and demonstrating their potential in next-generation digital circuitry.

6.2.1 Device fabrication and material characterization

Nominally undoped InAs NWs were grown on InAs (111)B substrates by Au-assisted chemical beam epitaxy (CBE), in a Riber Compact-21 reactor.[268] Gold nanoparticle catalysts were obtained by thermal dewetting, in the growth chamber, of a 0.5 nm thick Au film that had previously been thermally evaporated on the substrate (Figure 6.5a). The growth process took place at a temperature of (390 ± 10)°C (Figure 6.5b), using tri-methylindium (TMIn) and tertiarybutylarsine (TBAs) metalorganic precursors (Figure 6.5c). After the growth, the InAs NWs were mechanically detached from the growth substrate by sonication in isopropyl alcohol (Figure 6.5d-f) and randomly deposited on a $p_{++}Si/SiO_2$ substrate (0.3 mm/ 280 nm) by drop casting (Figure 6.5g-h). The NWs were contacted by a single step electron beam lithography (EBL) followed by an evaporation of a metallic bilayer (Cr/Au 10/100 nm) and lift-off. A passivation step in a highly diluted ammonium polysulfide $(NH_s)_2S_x$ – H_2O solution was performed prior to metal evaporation, to remove the native oxide from the NW surface in the contact areas and promote the formation of low resistance Ohmic contacts. The

fabricated InAs NW-based devices were backgated with silver paste onto the degenerate Si substrate.

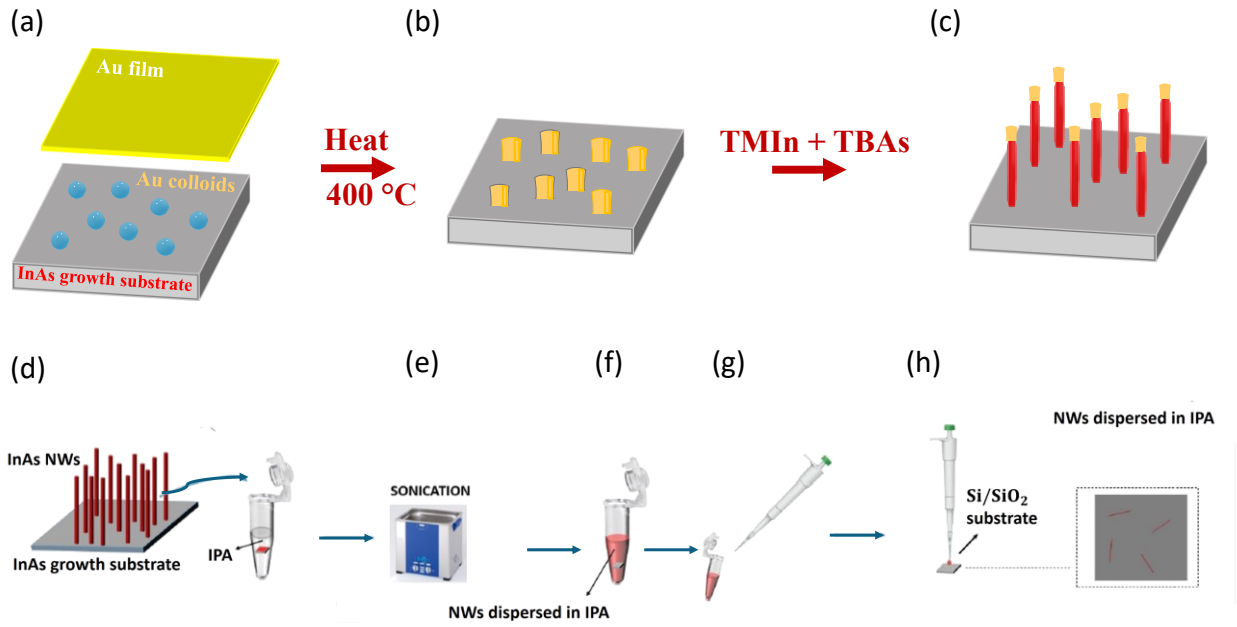


Figure 6.5: Au-assisted chemical beam epitaxy for the growth of InAs NWs. (a) InAs (111)B substrates with 0.5 nm thick Au film. (b) Thermalization process at around 400 °C. (c) Use of TMIn and TBAs metalorganic precursors. (d) Dispersion of InAs NWs in IPA and (e) sonication. (f-g) InAs NWs dispersed in IPA and (h) transferred onto Si/SiO_2 substrates.

The grown NWs exhibit a wurtzite crystal structure (see Figure 6.6a) with a hexagonal cross section, have diameters of about 100 nm and are around 4.5 µm long. The scanning electron microscopy (SEM) top view image of the fabricated device is shown in Figure 6.6b. The InAs NW is contacted by metal leads of Cr and Au, where chromium is used as adhesion layer. Cr, along with Ti and Ni, is commonly used as an adhesion layer for realizing metal electrodes on wurtzite InAs NWs.[259,269–271] In fact, due the favorable Fermi level pinning in the conduction band at the semiconductor surface, it allows to easily obtain good ohmic contacts with this nanostructures, provided a preliminary removal of the native oxide and passivation is performed.[272] The channel of the measured transistor is the part of the NW between the inner leads, indicated as source (S) and drain (D) in Figure 6.6b. The channel length is L = 1 µm and the radius of the NW is about r ≈ 50 nm. The radius of the NW was estimated from the SEM image. The schematic of the back-gated device, together with the measurement setup, is reported in Figure 6.6c, where only the leads used as electrodes are depicted. The source is grounded, whereas the voltage bias is applied to the drain electrode. The gate voltage is applied to the Si substrate covered by silver paste.

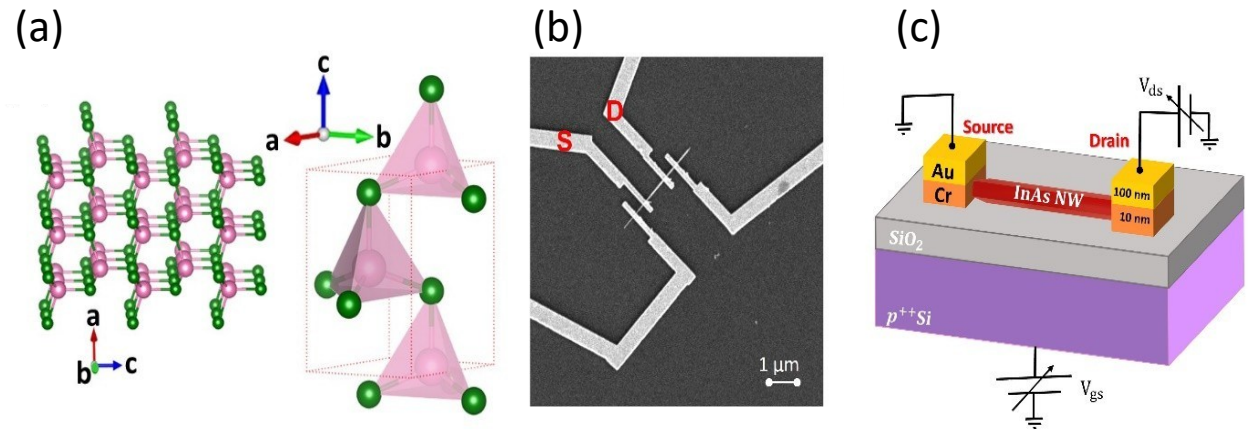


Figure 6.6: (a) Schematic of InAs WZ atomic structure (the green and pink spheres represent the arsenic and indium atoms, respectively; the single unit cell is depicted with a red dotted line). (b) SEM image of the device with the NW as conductive channel and Cr/Au leads as source and drain electrodes. The channel length is 1µm. (c) Schematic of the InAs NW-based back-gated FET with the measurement setup (only the leads used as electrodes are depicted).

6.2.2 Electrical characterization

Figure 6.7 reports the electrical characterization of one of the fabricated transistors with an InAs NW as a conductive path. Figure 6.7a shows the output characteristics, while Figure 6.7b shows the transfer characteristic at fixed V_{ds} = 10 mV, both in forward and reverse direction (V_{gs} from -10 V to 10 V, and back from 10 V to -10 V). The drain current is modulated by both the drain and the gate voltage, as demonstrated by the output curves collected stepping V_{gs} from -10 to 10 V. The linear behaviour of the output curves indicates the presence of Ohmic contacts (InAs/Cr) over the explored V_{ds} interval, ranging from -15 to 15 mV. Since the current I_d decreases for negative V_{gs}, the device presents n-type conduction. It is worth mentioning that this behaviour, despite the material being nominally undoped, is typical of Arsenic-based III-V semiconductor materials. The n-type conduction is confirmed by the transfer characteristic featuring higher current levels towards more positive gate voltage values. The estimated threshold voltage V_{th} is around -3 V, whose sign is typical of normally-on n-type FETs. The transistor under investigation operates efficiently: the device shows a high on/off current ratio of 5 x 10^3 and a subthreshold swing SS ≈ 2.7 V/decade, whose extraction is displayed in the inset of Figure 6.7b. The off current of the order of 10^{-10} A contributes to lower the static power consumption, while the high channel current of the order of µA can be widely exploited for high-speed electronic devices. By sweeping the gate voltage backward and forward in the range from -10 to 10 V, a hysteretic behaviour can be observed. The maximum hysteresis width, H_w, of the transfer characteristic, which is defined as the difference in voltage at the fixed current level of I_d = 6 nA, is less than 2 V. The origin of hysteresis can be found in a charge redistribution under the gate electric stress, which can result in charge transfer, charge trapping or charge polarization. Indeed, a high value of H_w is typically undesirable because it makes the transistor operation affected by the gate voltage sweep range, direction, and time. The maximum field-effect mobility is calculated using the usual equation. The transconductance curve in the backward direction is reported with a black line in the inset of Figure 6.7b.

The fabricated device presents thermally generated SiO_2 that serves as the gate dielectric and a highly doped Si substrate that operates as the back-gate. To estimate C_{ox}, the "metallic cylinder on

an infinite metal plate" approximation is used.[273] The charge density in the NW is assumed to be so high that the semiconducting NW can be treated as metallic. D. Vashaee et al.[274] showed the reliability of this approximation for GaN NWs with doping concentrations above 10^{17} cm^{-3}.

The fringing capacitance at the source and drain electrodes can be ignored because the NW length is one order of magnitude higher than the dielectric layer thickness (1 µm vs 0.3 µm). However, this model assumes that NW is completely embedded in the dielectric and possesses a circular cross

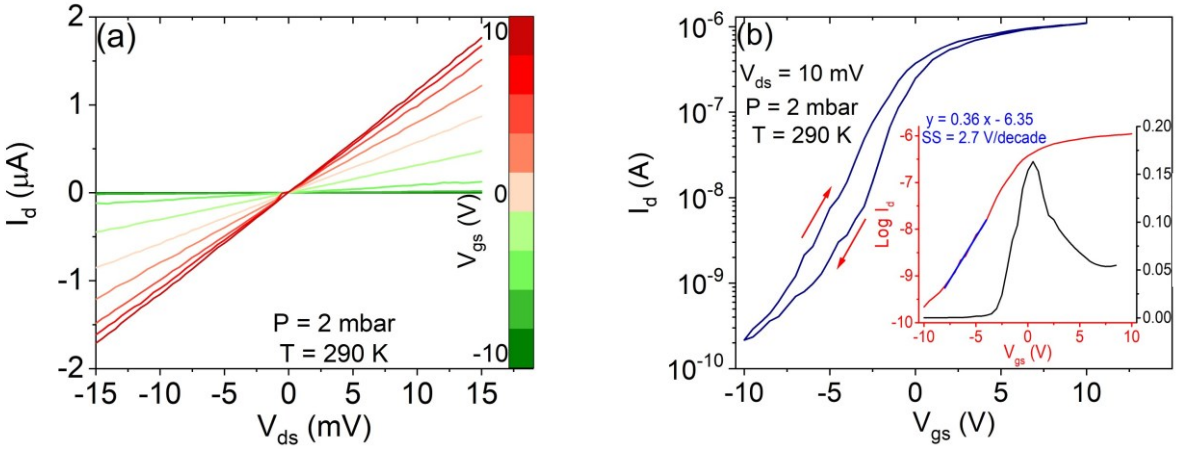


Figure 6.7: Electrical measurements at room temperature of an InAs NW-based FET: (a) Output curves for V_{ds} sweep at given V_{gs}. (b) Transfer characteristic on semilog scale at V_{ds} = 10 mV. (In the inset: log transfer curve (red) with linear fit (blue) for the extraction of SS and transconductance curve (black).

section. It yields an analytical equation for the gate oxide capacitance per unit length $C_{ox} = \frac{C'_{ox}}{L} = \frac{2\pi\epsilon}{\cosh^{-1}\frac{(t_{ox}+r)}{r}}$, where ε is the absolute dielectric constant and is given by the product of the constant of the embedding dielectric and the vacuum permittivity, $\varepsilon = \varepsilon_0 \varepsilon_{SiO2}$, r is the radius of the NW, r = 50 nm, and t_{ox} is the oxide thickness equal to 280 nm. The estimated capacitance is C_{ox} = 8.4 x 10^{-11} F/m. The maximum mobility reached at room temperature is μ_{FE} = 1591 cm^2 V^{-1} s^{-1}. By using this approximated model, the carrier mobility can be underestimated by a factor of almost 2 because the capacitance of non-embedded NWs is nearly two times lower than the value calculated as reported above. The overestimation of C_{ox} is confirmed by studies based on finite element method, implemented by O. Wunnicke.[275] The carrier concentration, which is defined as $n = \frac{C_{ox}(V_{gs}-V_{th})}{e\pi r^2}$, is equal to n = 8.2 x 10^{17} cm^{-3}, at room temperature[276]; this demonstrates the self-consistence of our method.[274]

6.2.3 Temperature-dependent electrical properties

The temperature dependence of the transistor transfer characteristics is investigated in the range (200 – 290) K, performing I-V measurements every 10 K. Figure 6.8a reports some of the transfer characteristics at V_{ds} = 10 mV, with V_{gs} from -10 to 10 V, showing the n-type behaviour. This behaviour is preserved when the temperature is lowered but the current decreases and the effect is particularly evident in the subthreshold region. The inset of Figure 6.8a shows the output characteristics at V_{gs} = 0 V and V_{gs} = 10 V. The linear behaviour of the output curves at different temperatures emphasizes the Ohmic character of the contacts between Cr/Au electrodes and the NW, and this is confirmed by

the negligible Schottky barrier height (SBH), extracted from the Arrhenius plot, which is depicted in the inset of Figure 6.8b. SBH largely affects the transport mechanism, especially when the transistor conductive path is made of a semiconductive NW. The current in the thermionic region can be fitted by the following equation:

$$I_d = I_{thermo} = SA^* T^2 \exp\left(-\frac{e\Phi_B}{k_B T}\right)\left[1 - \exp\left(-\frac{eV_{ds}}{k_B T}\right)\right]$$

where S is the cross-section area of the NW channel, A^* is the Richardson constant, k_B is the Boltzmann constant, and e is the elementary electron charge.[277]

The slopes of the linear fit of the Arrhenius curves correspond to the barrier height, ϕ_B, at different gate voltages. By plotting ϕ_B as a function of V_{gs}, in absence of Schottky barrier, the voltage bias at which ϕ_B-V_{gs} plot shows a kink is the value that distinguishes between the on and the off region, V_{th}.[277–280] In Figure 6.8b the dependence of ϕ_B on V_{gs} is shown. At V_{th} = -3 V, the transition from the off to the on region can be observed. Indeed, for $V_{gs} > V_{th}$, the device is in on-state operation. For $V_{gs} < V_{th}$, thermionic emission over the channel barrier is the only allowed transport mechanism.[277,281] The thermionic emission over the barrier can be investigated from the slope of the transfer characteristics in the subthreshold region. The subthreshold swing, SS, is defined as the change in gate voltage per decade of current and it is extracted for -7 V < V_{gs} < -4 V. It becomes lower than 1 V/decade at 200 K. The device operation can be described through the lowering of the barrier between source and drain; the charge flow in the channel results to be proportional to the concentration of electrons that can overcome the barrier. It can be demonstrated that the current in the subthreshold region has the following dependence[282]:

$$I_d \propto e^{\frac{q(V_{gs}-V_{th})}{(1+(C_d+C_{it})/C_{ox})K_B T}}$$

in which C_d, C_{it} and C_{ox} are the depletion, the interface trap, and the gate oxide capacitance per unit length, respectively. Taking the derivative of the logarithm of I_d with respect to V_{gs}, the SS is given by

$$SS = \left(\frac{d \log I_d}{dV_{gs}}\right)^{-1} = \frac{k_B T}{q}\left(1 + \frac{C_d + C_{it}}{C_{ox}}\right)\ln 10$$

Because of the structure of the device presented previously, the source and drain capacitances can be negligible. In the subthreshold region, the NW is fully depleted, and C_d is negligible. The linear fit of SS as a function of temperature, which is presented in Figure 6.8c, provides the estimation of the density of trap states at the Fermi energy E_F, D_{trap} = 4 x 10^8 cm^{-1} eV^{-1}.[283,284] As a transistor metric, the SS indicates how sharply the transistor switches on and off. A related figure of merit is the on/off current ratio: the higher the ratio, the more the device is suitable for digital applications. Moreover, an important goal of electronics is the lowering of static power dissipation, which corresponds to low currents when the device is switched off. A strong reduction in the off current can be observed from the transfer characteristics. Figure 6.8c also reports the on/off current ratio as a function of temperature. It increases by three orders of magnitude, reaching 5 x 10^6, lowering the temperature from 290 to 200 K.

Figure 6.8d reports the field-effect electron mobility dependence on temperature. Two competing phenomena, which are the ionized impurity scattering and phonon scattering, generally limit the semiconductor mobility.[285–287] The first mechanism is dominant at very low temperatures and yields

an increasing mobility with increasing temperature, while at higher temperatures phonon scattering becomes the main mechanism and causes a decrease in mobility with increasing temperature.[288–290] The influence of scattering mechanism from charged impurities can be observed below 50 K for InAs NWs based transistors.[266] In our InAs FETs the field-effect mobility goes from 1591 to 1943 $cm^2 V^{-1} s^{-1}$, lowering the temperature from 290 to 200 K. The obtained mobilities are consistent with literature. The change in mobility can be described by a power law, $\mu_{FE} \sim T^{-\alpha}$. Fitting the experimental data with the power function, as reported in the inset of Figure 6.8d, the α parameter results to be (0.6 ± 0.1). Indeed, the mobility dependence on temperature due to optical phonon scattering only is expected to be proportional to $T^{-0.5}$.[291] Therefore, in the explored temperature range, the most dominant scattering mechanism should be due to optical phonons. This result is consistent with the InAs WZ phase, which is characterized by three low-lying optical and six highly placed optical branches, in addition to three acoustic branches.[292]

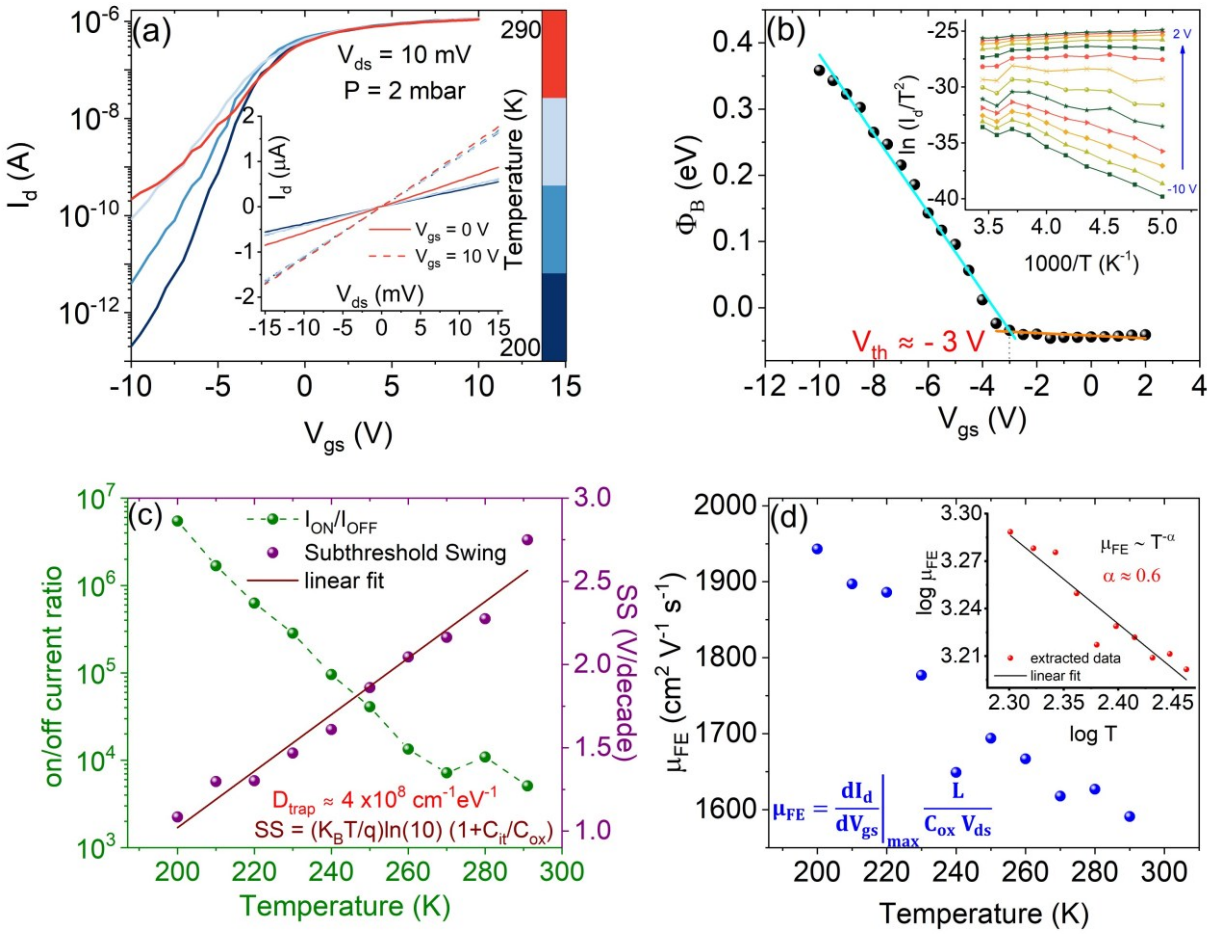


Figure 6.8: (a) Electrical measurements in (200, 290) K range. Transfer characteristics on semilog scale at V_{ds} =10 mV and T = 200, 230, 260, 290 K (in the inset: Output curves at V_{gs} = 0 V and V_{gs} = 10 V at the same temperatures of the transfer curves). (b) Effective barrier height ϕ_B extracted from the Arrhenius plot as a function of V_{gs}. ϕ_{SBH} results to be negligible (in the inset: Arrhenius plot at V_{gs} between -10 V and 2 V). (c) I_{ON}/I_{OFF} on semilog scale (green dots) and SS (purple dots) as a function of temperature. The density of trap states extracted from the linear fit of SS is D_{trap} = 4 x 10^8 cm^{-1} eV^{-1}. (c) Temperature dependence of field-effect mobility in the temperature range from 200 to 290 K (in the inset: Mobility as a function of temperature on log scale. The fit with the power law $T^{-\alpha}$ gives the estimation of the parameter, α≈ 0.6).

6.2.4 Resistive-load inverter

InAs has remarkable applications in the wide field of digital electronics that is based on logic operations implemented through different circuits. The InAs NW-based transistor was employed in a resistive load inverter circuit, whose schematic is shown in the inset of Figure 6.9a. The driver transistor is the n-type NW-based FET investigated in the previous sections. The load consists of a resistor R, whose optimal resistance results to be about 400 kΩ. The power supply of the circuit is V_{DD} = 10 mV. While applying a gate voltage sweep from -10 to 10 V, the drain voltage was monitored as the outcome of the circuit. Although the coupling between a transistor and a resistor is not the most advantageous approach for power consumption and processing speed, it results to be low cost and easy to implement. Firstly, the analysis was conducted at room temperature. Figure 6.9a shows the VTC of the inverter. To evaluate NM_H and NM_L, V_{IH} and V_{IL} are rescaled considering that V_{in} ranges from -10 to 10 V, while V_{out} from 0 to 10 mV. They are defined as $NM_H = V_{OH} - V_{IH,mod}$ and $NM_L = V_{IL,mod} - V_{OL}$, where $V_{IH,mod} = 0.5 \times 10^{-3} \times (V_{IH} + 10)$ V and $V_{IL,mod} = 0.5 \times 10^{-3} \times (V_{IL} + 10)$ V. The percentage of variation with reference to V_{DD}, 10 mV, is 30% for NM_H and 24% for NM_L. The noise margins represent the tolerance to signal fluctuations. The obtained values are well above the minimum requirement that the noise margin should be at least 10% of V_{DD}.[265] The extracted noise margins evidence the robustness of the inverter toward noise for multistage operations. Several digital applications use multiple inverters connected in series; in these cases, the output signal from one stage serves as the input signal for the subsequent step.[293,294] Hence, NM_L and NM_H indicate the noise margins that the inverter can tolerate for multistage operations, which is crucial for the demonstration of ring oscillator and SRAM, as example.[295] The threshold voltage of the inverter, V_T, was estimated by the intersection of the VTC and the linear equation $V_{out} = 0.5 \times 10^{-3} (V_{in} + 10)$, as depicted in Figure 6.9b. The equation parameters were rescaled to make $V_{out} = V_{in}$, because V_{in} and V_{out} ranges are different in size and order of magnitude. The inverter with the 400 kΩ resistor has V_T around 0 V. Figure 6.9b reports the VTC of different inverter circuits with resistors of 80 kΩ, 400 kΩ and 2 MΩ. The ideal characteristic curve is dashed to compare the three VTCs to it. It is evident that the curve of the inverter with 400 kΩ resistor has a more similar behaviour to the ideal characteristic with respect to the other VTCs.[296–298] Moreover, the red VTC is symmetric in the V_{in} range. The curve with the lowest resistance presents the worse performance, as demonstrated by its slope, the right shift of V_T and the higher zero logical state that can reach. The performance of the inverter was also tested at T = 200 K, both with the 0.4 and 2 MΩ resistors. The measured VTCs are reported in Figure 6.9c. The threshold voltage V_T shifts to higher voltage values, making the curve lose the symmetric behaviour highlighted at room temperature with 0.4 MΩ. However, the inverter is still working at low temperature, showing comparable small transient regions.[299]

An important challenge in the realization of this type of inverter consists of the reduction of the transient region whose width is related to the gain of the inverter. It must be higher than the ratio between the output and input ranges to guarantee the regeneration of the logical states, i.e. greater than 5×10^{-4} (10 mV/20 V = 5×10^{-4}).[300–302] In Figure 6.9d the gain curves for all the investigated InAs NW-based inverters are reported. It is quite constant around 3×10^{-3}, which is one order of magnitude higher than the minimum expected value. The lowest gain is exhibited by the inverter with the resistor of 80 kΩ, and this is consistent with the previous comments.

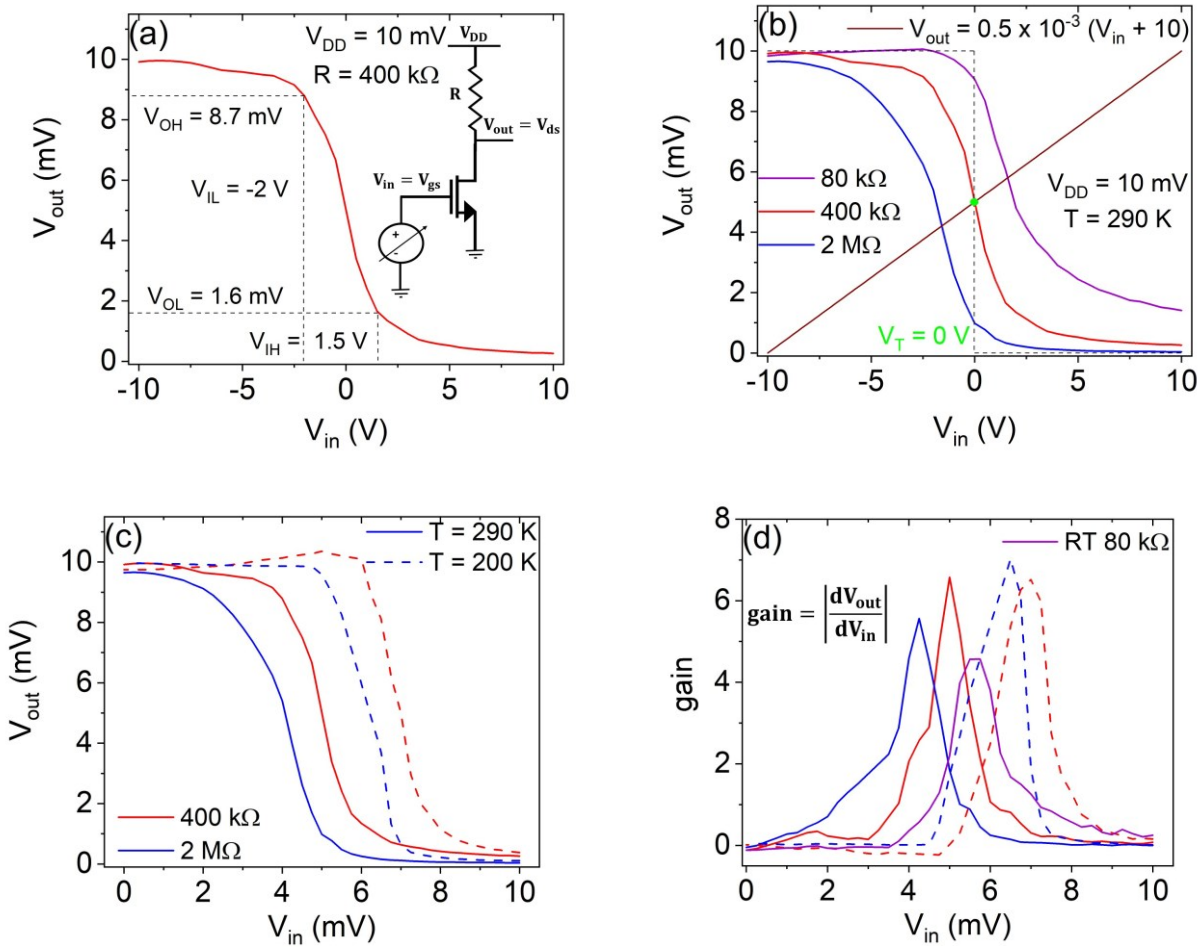


Figure 6.9: Inverters measurements: (a) Voltage-transfer-characteristic (VTC) of the resistive load inverter based on the InAs NW-based transistor with a 400 kΩ resistor, obtained at V_{DD} = 10 mV. The evidenced points of the VTC are characterized by a slope equal to 1 x 10^{-3}. The extracted noise margins correspond to 30% and 24% of V_{DD} for the high and the low level, respectively. The schematic of the analyzed inverter is reported as inset. (b) VTCs of the resistive load InAs NW-based inverters with different resistors. The dashed curve is the ideal inverter characteristic. The reported green dot shows the threshold voltage of the inverter with a 400 kΩ resistor. (c) VTCs at room temperature (RT, solid lines) and 200 K (dashed lines) with different resistors. (d) Gain of the different inverters implemented at room temperature and 200 K with different resistors.

DATA AVAILBILITY STATEMENT

The data that support the findings of this study are available from the author of this thesis. To ensure the reproducibility of the reported results, all experimental protocols, including material synthesis, device fabrication parameters, and characterization settings, were strictly standardized. Each key experiment was performed in multiple independent batches. Data processing followed a consistent pipeline, and raw datasets have been documented to allow for external verification of the findings.

CONCLUSIONS AND FUTURE PERSPECTIVES

The research presented in this thesis has explored the vast potential of low-dimensional materials, ranging from 2D vdW heterostructures to 1D nanotubes and nanowires, as the building blocks for post-Moore's law electronics. By navigating the challenges of material stability, contact resistance, and device architecture, this work demonstrates a clear pathway from fundamental material characterization to the realization of high-performance optoelectronic, logic, memory, and neuromorphic systems. A central aspect of this work is the demonstration of vdW heterostructures as a transformative platform for functional integration. The inherent lack of dangling bonds at 2D interfaces allows for the vertical stacking of disparate materials without the crystalline constraints of lattice matching. This architectural flexibility enables the integration of multiple functionalities into a single device platform. Beyond this, these heterostructures serve as a catalyst for enhanced optoelectronic properties that surpass the capabilities of individual isolated layers.

The investigation began with bP, where optimization strategies were successfully implemented for contact resistance and an efficient capping method to mitigate its inherent environmental instability. The combination of bP with MoS_2 into staggered vdW heterostructures proved to be a versatile platform for photodetectors and self-powered photovoltaic applications, showcasing the power of band-alignment engineering. A quantitative analysis reveals that the relaxation time constants for the bP/MoS_2 heterojunction are substantially reduced relative to those of single MoS_2 flakes. This reduction confirms that the high mobility bP (around 269 $cm^2 V^{-1} s^{-1}$) layer facilitates more efficient charge carrier extraction and faster signal recovery, thereby overcoming the intrinsic speed limitations of MoS_2. The shown linear dependence of the photocurrent on the incident laser power is a highly desirable characteristic for a photodetector, as it ensures a constant responsivity across the operational range. This linearity facilitates predictable signal processing and high-fidelity detection of varying light intensities. Importantly, the internal electric field created by the type-II staggered band alignment at the bP/MoS_2 interface enables the separation of photogenerated carriers without the need for an external bias. This produces a short circuit current of 0.12 nA and an open circuit voltage of 75 mV, enabling the self-powered mode operation of the bP/MoS_2 heterostructure.

Addressing the need for air-stable alternatives, the study of WS_2/$PdSe_2$ heterostructures revealed an exceptional multifunctionality. This versatility is rooted in the distinct electronic properties of the constituent materials; specifically, $PdSe_2$ exhibits ambipolar behaviour in ambient conditions that transitions to n-type conduction under vacuum conditions, while WS_2 maintains consistent n-type polarity regardless of the environment. The resulting WS_2/$PdSe_2$ heterostructure demonstrates n-type behaviour with on/off current ratios on the order of 10^8, successfully exploiting these environmental sensitivities. Consequently, these devices not only provided stable optoelectronic responses for visible-light photodetectors but also served as optoelectronic pressure sensors and artificial synaptic elements. A key finding in this research was the significant enhancement in carrier dynamics: the combination of $PdSe_2$ and WS_2 in the heterojunction results in response times that are one order of magnitude shorter than those of individual WS_2 FETs. The superior carrier mobility of $PdSe_2$, which is around two orders of magnitude higher than WS_2, continue playing a fundamental role in achieving these accelerated relaxation constants, facilitating more efficient charge transfer and extraction across the vdW interface. The enhanced photoresponsivity and environmental sensitivity, typical of $PdSe_2$, has led to the demonstration of the WS_2/$PdSe_2$ heterostructure as an

optoelectronic pressure sensor. Furthermore, the controllable persistent photoconductivity within these structures was successfully exploited to emulate biological synaptic plasticity with PPF and PTP with indexes of approximately 140% and 300%, respectively. This transition from high-speed switching to long-term memory states underscores the unique ability of vdW heterostructures to support multi-modal operations within a single, air-stable device architecture.

While the 2D heterostructures resulted as multifunctional platforms for advanced applications in different fields, a major hurdle remains for 2D-based logic: the inherent n-type dominance of most TMDs and the relative scarcity of stable, high-performance p-type 2D semiconductors. Thus, this challenge was addressed in this thesis by investigating the electrical properties of $MoSe_2$ and an innovative doping strategy based on interfacial coupling with the anti-ferromagnetic insulator CrOCl. By exploiting the charge transfer mechanism at the $MoSe_2$/CrOCl interface, high-performance devices with p-type conduction were realized, providing a robust platform for cFET architectures essential for CMOS applications. The pristine $MoSe_2$ FET was characterized by n-type conductive behaviour with electron mobility of 18 $cm^2 V^{-1} s^{-1}$, while $MoSe_2$/CrOCl FET showed p-type conduction with hole mobility of 1.1 $cm^2 V^{-1} s^{-1}$. This development allows for the fabrication of lateral homojunctions between pristine and p-doped regions, which exhibit a unique anti-ambipolar transport behaviour with the peak current hundreds of times lower than the on-state current of the individual pristine or p-doped $MoSe_2$ devices. This characteristic is utilized to implement high-gain logic gates, such as resistive-load inverter with the pristine $MoSe_2$/p-doped $MoSe_2$ homojunction as a resistive load and CMOS inverter with gain of 1.2 and total noise margins around 70%, within a single material system. Beyond electronic logic, the optoelectronic properties of the individual pristine and p-doped $MoSe_2$ devices, as well as of their combination, were thoroughly explored, demonstrating a stable photoresponse with a strictly linear dependence of the photocurrent on incident optical power across all device configurations. Wavelength-dependent characterization identified a peak responsivity at 780 nm, consistent with the excitonic transitions of $MoSe_2$. Notably, the strong built-in potential at the p-n interface enabled self-powered photovoltaic operation, allowing for efficient photodetection without external bias, with I_{sc} that reach up to 1 nA. Furthermore, the integration of a floating gate into this heterojunction platform enables the realization of non-volatile multilevel memory and artificial synapses. By mimicking biological action potentials through pulsed voltages sequences, these devices demonstrate the potential for integrating logic, storage, and neuromorphic computing into a simplified, air-stable 2D architecture.

Finally, the transition to 1D nanostructures provided a critical perspective on dimensionality. The study of WS_2 nanotubes highlighted how cylindrical geometry and curvature-induced strain introduce intrinsic ambipolarity and enhance self-powered photodetection phenomena with a short circuit current of 2.6 A and an open circuit voltage of 3 mV, which are distinct from their planar counterparts. Furthermore, the high-performance InAs nanowires inverters served as a high-mobility benchmark, demonstrating that while 2D materials offer unmatched scaling potential, 1D architectures provide superior electrostatic control and maturity for integrated digital technology.

While this thesis demonstrates significant progress, several avenues remain open for future exploration. The next step for 2D/1D electronics is the transition from flake-level fabrication to wafer-scale integration. Investigating large-area CVD growth and automated transfer processes will be essential for compatibility with existing CMOS foundries. The artificial synapses demonstrated here are individual components. Future work should focus on integrating these devices into crossbar

arrays to implement hardware-level neural networks capable of complex pattern recognition and energy-efficient edge computing. In conclusion, by exploring a broad spectrum of low-dimensional systems and their combinations, this thesis highlights how vdW engineering and dimensionality control can bypass traditional scaling limits, offering a robust and versatile framework for the next generation of high-performance, integrated electronics.

APPENDIX A: Gradual channel approximation for current derivation

To describe the fundamental operation of a FET in the on state analytically, the gradual channel approximation (GCA) serves as the standard physical framework. The GCA model is based on two main assumptions: uniformity across the channel width and field separation. The channel width is assumed to be sufficiently large such that the potential distribution is independent of the y-coordinate; the variation of the electric field along the channel (ε_x) is assumed to be much smaller than the variation of the field perpendicular to it (ε_z) induced by the gate. Under this approximation, the drain current I_d at any x point along the channel can be calculated. The current density j in such a transistor is $j = -en(x,z)v(x)$ with the carrier density $n(x,z)$ and the carrier velocity $v(x)$ both being independent of y due to the assumption on the transistor width. Specifically, the gate-induced electric field modulates the charge distribution vertically from the oxide interface into the substrate (z-direction dependence), while the drain-source bias creates a potential gradient that varies the charge concentration longitudinally from source to drain (x-direction dependence). Conversely, according to the GCA, the density is assumed to be uniform across the width of the device (y-direction). By assuming that the carrier velocity is strictly longitudinal ($v_z = 0\ \mathrm{cm/s}$) and that the device properties are uniform across the width, the volumetric transport problem is reduced to a one-dimensional model. This allows the integration of the local carrier density $n(x,z)$ into a single sheet charge density $Q_{inv}(x)$ at the semiconductor-dielectric interface.

The total current can be calculated as an integral of the current density j over the cross-section of the channel:

$$I = \int\int j(x,y,z)\,dydz$$
$$I = -\int_0^W dy \int_0^\infty dz\, en(x,z)v(x) = WQ_{inv}(x)v(x) \qquad (A.1)$$

$Q_{inv}(x)$ is the charge per unit area. In the regime of strong-inversion, the gate-dielectric-semiconductor stack behaves as a parallel-plate capacitor. In this framework, the inversion charge density Q_{inv} is defined as a negative quantity for n-channel devices, consistent with the electron charge. The resulting negative sign is compensated by the direction of the electron velocity relative to the longitudinal electric field, ensuring a positive conventional drain current in the forward bias regime. The amount of mobile charge induced at any point x along the channel is modulated by the local potential $V(x)$:

$$Q_{inv}(x) = -C_{ox}\left[V_{gs} - V_{th} - V(x)\right] \qquad (A.2)$$

where C_{ox} is the oxide capacitance per unit area. The gate overdrive $V_{gs} - V_{th}$ applies only at the source end of the channel. On the other hand, at the drain end the drain-source bias (V_{ds}) leads to an effective reduction of the overdrive $\left(V_{gs} - V_{th} - V_{ds}\right)$, and in general along the channel one obtains $\left(V_{gs} - V_{th} - V(x)\right)$. The carrier velocity is proportional to the longitudinal electric field, $\vec{v} = \mu\,\vec{\epsilon}$, where μ is the charge carrier mobility. For electrons, the velocity is $v = -\mu\epsilon_x = -\mu\frac{dV}{dx}$ because they move in the opposite direction of the field. Thus, the velocity becomes:

$$v = -\mu\frac{dV}{dx} \qquad (A.3)$$

By plugging equations $A.2$ and $A.3$ in equation $A.1$, one obtains:

$$I = WC_{ox}\mu\left[V_{gs} - V_{th} - V(x)\right]\frac{dV}{dx}$$
$$Idx = WC_{ox}\mu\left[V_{gs} - V_{th} - V(x)\right]dV \quad (A.4)$$

By integrating the current equation $A.4$ along the channel length L:

$$\int_0^L Idx = \int_0^{V_{ds}} WC_{ox}\mu\left[V_{gs} - V_{th} - V(x)\right]dV \quad (A.5)$$

Integrating both sides of equation $A.5$ and noting that due to the requirement of current continuity in an ideal MOSFET the current is independent of x, the standard relationship for the drain current in the linear regime is obtained:

$$I_d = \mu\frac{W}{L}\,C_{ox}\left[(V_{gs} - V_{th})V_{ds} - \frac{V_{ds}^2}{2}\right] \quad (A.6)$$

This model defines the transition between the primary operating states of the device: the liner and the saturation regions. In the linear region, at low drain voltages, $V_{ds} \ll V_{gs} - V_{th}$, the current increases linearly with V_{ds} as the channel acts as a gate-tunable resistor.

To understand the device behaviour at low drain bias voltages, which is the typical working regime for 2D materials-based FETs, it is possible to perform a Taylor expansion of $I_d(V_{ds})$ around the point $V_{ds} = 0$. The first derivative of the current $A.6$ with respect to V_{ds} defines the output conductance g_d:

$$g_d = \frac{\partial I_d}{\partial V_{ds}} = \mu\frac{W}{L}C_{ox}(V_{gs} - V_{th} - V_{ds})$$

At the limit $V_{ds} \to 0$, the linear conductance is obtained:

$$g_{d,0} = \mu\frac{W}{L}C_{ox}(V_{gs} - V_{th})$$

The second derivative of $A.6$ is constant and represents the quadratic curvature:

$$\frac{\partial^2 I_d}{\partial V_{ds}^2} = -\mu\frac{W}{L}C_{ox}$$

By combining these terms, the expansion becomes:

$$I_d(V_{ds}) \approx \left[\mu\frac{W}{L}\,C_{ox}(V_{gs} - V_{th})\right]V_{ds} - \mu\frac{W}{L}C_{ox}V_{ds}^2$$

In the linear regime, i.e. in the limit of small drain bias, specifically when $V_{ds} \ll V_{gs} - V_{th}$, the quadratic term becomes negligible compared to the linear term. In this regime, the transistor behaves as a voltage-controlled resistor, and the current-voltage characteristic simplifies to:

$$I_d = \mu\frac{W}{L}C_{ox}(V_{gs} - V_{th})V_{ds}$$

PUBLICATIONS AND INTERNATIONAL CONFERENCES

The core research findings presented in this thesis have been extensively peer-reviewed and published in leading scientific journals. The candidate served as the first author on the majority of these publications, reflecting a primary role in the conceptualization, experimental execution, and manuscript preparation of the work. Furthermore, most of these primary works have been disseminated within scientific community through oral presentations and posters at international conferences and workshops, as detailed in the subsequent section. In addition to these primary works, a secondary list of co-authored publications is included, representing collaborative research projects and international partnerships conducted throughout the doctoral program.

Publications related to this thesis

1. **Viscardi, L.** *et al.* Interface-Engineered MoSe2/CrOCl Complementary FETs Integrating Logic, Memory, and Neuromorphic Functions, *Small Structures*, vol. 7, fasc. 3, p. e202500840, 2026, doi: 10.1002/sstr.202500840.
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Other Publications

14. Giubileo F, Faella E, De Stefano S, **Viscardi L**, Intonti K, Mazzotti A, Sessa A, Durante O, Pelella A, Cheng G, Mattevi C, Passacantando M and Bartolomeo A D 2025 Hierarchical WSe2 Nanoflowers for Efficient Field Emission *Advanced Electronic Materials* **11** e00490
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Oral presentations and poster contributions

- **SELDoM (Surface and Electronic properties of Low Dimensional Materials)**, 13-15 October 2025, Napoli, Italy. Poster contribution. *Multifunctional optoelectronic and synaptic properties of $WS_2/PdSe_2$ van der Waals heterostructures*.
- **NINETEENTH 2025**, 28-30 September 2025, Salerno, Italy. Oral presentation. *Electrical and Optoelectronic properties of $WS_2/PdSe_2$ heterostructures.*
- **IEEE-NANO 2025**, 13-16 July 2025, Washington DC, USA. Oral presentation. *Single WS_2 nanotube-based field effect transistor: ambipolar conduction and self-powered photodetection.**
- **Graphene 2024**, 25-28 June 2024, Madrid, Spain. Poster contribution. *Electric transport and photoresponse in BP/MoS_2 heterostructure.*

- **NMDC 2023 (Nanotechnology Materials and Devices Conference 2023)**, 22-25 October 2023, Paestum, Italy. Oral presentation. *InAs nanowires field effect transistors: temperature dependence of electrical properties and digital applications.*
- **SIF 2023 (Società Italiana di Fisica 2023, *Physics Italian Society*)**, 11-15 September 2023, Salerno, Italy. Oral presentation. *InAs nanowires field-effect transistors: temperature dependence of electrical properties and digital applications.*
- **NN23 (Conference on Nanoscience and nanotechnologies)**, 4-7 July 2023, Thessaloniki, Greece. Poster contribution. *Ni and NiCr alloy as metal contacts in Black Phosphorus field-effect transistors.*
- **CM LTP 2023 (Condensed Matter & Low temperature Physics 2023)**, 5-11 June 2023, Kharkiv, Ukraine (online conference). Oral presentation. *Ni and NiCr contacts in Black Phosphorus based field-effect transistors.*

*****This work was published as a conference proceeding and was awarded the **Best Student Paper Award**.

International Schools

- **17th International Summer Schools on Nanosciences & Nanotechnologies (ISSON23)**, 1-8 July 2023, Thessaloniki, Greece.
- **21st European School on Nanosciences & Nanotechnologies (ESONN24)**, 25 August – 7 September 2024, Grenoble, France.

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