PECVD low stress silicon nitride analysis and optimization for the fabrication of CMUT devices

Alvise Bagolini[1], Alessandro Stuart Savoia[2] and Antonino Picciotto[1], Maurizio Boscardin[1], Pierluigi Bellutti[1], Nicola Lamberti[3] and Giosuè Caliano[2]

[1] The MTLab Facility (Microfabrication Facility), Fondazione, Bruno Kessler (FBK), Via Sommarive 18, I-38123, Trento, Italy

[2] Dipartimento di Ingegneria, Universita Roma Tre, via della Vasca Navale 84, I-00146, Roma, Italy

[3] Dipartimento di Ingegneria Industriale, Universita di Salerno, Via Giovanni Paolo II, 132, I-84084, Fisciano (SA), Italy

Abstract

Two technological options to achieve a high deposition rate, low stress plasma-enhanced chemical vapor deposition (PECVD) silicon nitride to be used in capacitive micromachined ultrasonic transducers (CMUT) fabrication are investigated and presented. Both options are developed and implemented on standard production line PECVD equipment in the framework of a CMUT technology transfer from R & D to production. A tradeoff between deposition rate, residual stress and electrical properties is showed.

The first option consists in a double layer of silicon nitride with a relatively high deposition rate of ~100 nm min^{-1} and low compressive residual stress, which is suitable for the fabrication of the thick nitride layer used as a mechanical support of the CMUTs. The second option involves the use of a mixed frequency low-stress silicon nitride with outstanding electrical insulation capability, providing improved mechanical and electrical integrity of the CMUT active layers. The behavior of the nitride is analyzed as a function of deposition parameters and subsequent annealing. The nitride layer characterization is reported in terms of interfaces density influence on residual stress, refractive index, deposition rate, and thickness variation both as deposited and after thermal treatment. A sweet spot for stress stability is identified at an interfaces density of 0.1 nm^{-1}, yielding 87 MPa residual stress after annealing. A complete CMUT device fabrication is reported using the optimized nitrides. The CMUT performance is tested, demonstrating full functionality in ultrasound imaging applications and an overall performance improvement with respect to previous devices fabricated with non-optimized silicon nitride.

Keywords: CMUT, MEMS devices, microfabrication, mixed frequency silicon nitride, PECVD

1. Introduction

Capacitive micromachined ultrasonic transducers (CMUT) are micro-electro-mechanical devices introduced in the late 1990s [1]. These devices consist of a 2D array of miniaturized electrostatic cells, electrically connected in parallel and driven in phase, and fabricated (at that time) using surface micromachining techniques. This new generation of ultrasonic transducers seems to be competitive with piezoelectric transducers either for water or air coupled applications, thanks to

the inherently low mechanical impedance associated with a thin vibrating membrane. The CMUT takes advantage of the well-established microelectronic technology, as well as the good mechanical properties of silicon nitride as the basic material to fabricate the active plates. Further advantages of this kind of devices are the ability to integrate electronics on the same silicon wafer to design complex 1D and 2D array layouts using simple photolithography techniques. Ultimately, the low cost of manufacturing, especially for those applications requiring high volumes of production, may justify the adoption of this MEMS technology in medical ultrasound imaging.

The first immersion operation was investigated in 1996 [2] but experienced rapid development only in recent years using different technology approaches, ranging from surface micromachining [3] to wafer bonding [4]. The possibility to fabricate CMUTs with a sealed-cavity at reasonably low temperatures, compatible with underlying CMOS devices, though recently explored with wafer bonding techniques [5], has mainly relied on surface micromachining involving the use of PECVD layers [6]. Thermal cycles to control the residual stress of PECVD silicon nitrides were proposed by Cianci *et al* [7], while a low stress silicon nitride was first employed by Knight *et al* [8] for the realization of the device's vibrating plates. A promising technique for the realization of controlled stress silicon nitrides layers consists in the deposition of a sequence of compressive and tensile layers whose stress compensates: known since the early 1990s [9, 10], dual frequency PECVD silicon nitride was first demonstrated as an effective plate layer for CMUT by Savoia *et al* in 2005 [11] and confirmed by Cianci *et al* [12] in 2006.

The present paper investigates PECVD silicon nitride layers deposited with various techniques for the fabrication of CMUT devices using the reverse fabrication process (RFP) [13], patented by Caliano *et al* [14, 32]. Using this process, the fabrication of the capacitive cell is performed inverting the standard sequence of the layers by growing successive silicon nitride layers onto a silicon wafer, starting from the active plate and ending with the final supporting layer of the CMUT structure. The device is built on top of a low pressure vapor deposition (LPCVD) silicon nitride film grown over a silicon wafer, using a standard surface micromachining process, using mainly PECVD silicon nitride and finally, once the CMUT is realized, the bulk silicon wafer is completely removed by a chemical etching process, allowing the silicon nitride plates to freely vibrate. The device is fabricated using a commercial silicon wafer with a low-stress LPCVD silicon nitride layer and the whole process temperature is not higher than 350°C, so that a wide range of materials can be used.

In this paper, starting from the RFP process, different modes of deposition of the dielectric films involved in the manufacturing of the device are investigated, and the characteristics of the layers are optimized according to their specific function, with the aim of improving the process and of demonstrating its efficiency.

Section 2 describes the process and the materials involved, and identifies the characteristics that each layer has to exhibit, defining two main deposition techniques, that realize the scope. In section 3 the different nitride typologies obtained are tested, showing the adopted recipes and the obtained results in terms of deposition rate and residual stress. In section 4 the nitride layer characterization is reported in terms of interfaces density influence on residual stress, refractive index, deposition rate, and thickness variation both as deposited and after thermal treatment. In section 5 the fabrication of a complete CMUT transducer is shown, using the above techniques and the realized prototype is tested emphasizing the good agreement with the modeling results obtained with finite element modeling (FEM). In section 6, there are the conclusions.

2. Materials and methods

The RFP process [13] uses as the active plate a multi-layer structure in which the LPCVD silicon nitride is the main layer. The LPCVD nitride layer has process characteristics such as to allow the deposition of calibrated-thickness layers on a large area, maintaining the stress low and with excellent mechanical characteristics. Being the temperature of the process not compatible with the other materials used, this type of nitride is at first deposited on top of the bare silicon substrate, specifically 4'' <1 0 0> *p*-type boron, 100 ohm·cm, silicon wafers (Silicon Valley Microelectronics, Inc., Santa Clara, CA, U.S.A.). We used wafers covered with a layer of Si-rich LPCVD silicon nitride, with a calibrated thickness of 1 μm and with low-stress characteristics (<100 MPa) obtained with a deposition temperature of 850 °C. The remaining layers of SiN, fabricated with PECVD process, are compatible with the materials used for the metallization (Al–Ti), and with the sacrificial layer (chromium), but have different functions. The two layers of nitride between the two metallizations are used as passivation layers during the etching of the sacrificial layer and as an electrical insulator when operating the device, while the third nitride layer deposited on top of the second metallization acts exclusively as a passivation layer. The remaining nitride layer serves to reliably seal the realized cavities and as a mechanical support of the CMUT microstructure. All nitride layers have to preserve their low residual stress state (<100 MPa) through all fabrication steps. The LPCVD layer should have low stress to guarantee the operation of the device in respect of the design parameters. Moreover, the control of the stress of the subsequent PECVD nitride layers is a critical requirement for the yield of the manufacturing process. As a matter of fact, it is worth pointing out that the total thickness of the PECVD layers turns out to be about four times that of the LPCVD layer. Hence, the low residual stress is a mandatory requirement also for the PECVD layers, in order to avoid the risk of delamination following the final release of the CMUT by silicon substrate etching. Moreover, the electrical and mechanical characteristics of the two nitride layers between the two electrodes should ensure good structural integrity and good selectivity with respect to the sacrificial material during the chemical etching, and excellent electrical insulation during operation. Therefore, the fulfillment of all of these requirements using a single type of PECVD nitride is a major challenge in the development of RFP CMUTs. To

overcome the difficulties of making a unique material that meets all these requirements, we have developed two recipes of PECVD nitride whose characteristics comply with the criteria mentioned above, and with optimized deposition rate in relation to the different thicknesses to achieve, in the perspective to make this process more suitable for industrial production.

The first type of SiN consists in a double layer of silicon nitride with low compressive residual stress, which is suitable for the fabrication of the thick nitride layer used as a mechanical support of the CMUTs, and as a sealing layer to guarantee the effective closure of the sacrificial release etching holes. In this first deposition method, a high deposition rate was addressed, given the high thickness typically required by the backplate layer (figure 1).

The second type of SiN involves the use of a mixed frequency low-stress silicon nitride with outstanding electrical insulation capability, providing improved mechanical and electrical integrity of the CMUT active layers. In this second deposition method, electrical insulation characteristics were privileged, rather than the deposition rate that is irrelevant due to the small thicknesses of the passivation layers (figure 1).

3. Experimental tests on different nitride typologies

Several parameters control the plasma enhanced deposition of silicon nitrides, namely: nitrogen flow, silane flow, ammonia flow, pressure, and power and excitation frequency of the RF generators used. Tests were carried out in order to measure the residual stress of two different low stress nitride typologies as follows:

- *double layer nitride (DLN)*: combining two nitride layers (a compressive and a tensile one) which vary in several parameters (power, frequency, gas flow). The reported deposition rates are theoretical since the commutation times have to be taken into account when switching from one nitride layer to the other: it limits the nitride stacking to a few relatively thick layers of each kind.
- *mixed frequency nitride (MfSiN)*: setting the same gas and power levels and changing only the RF generator frequency. The commutation time between tensile and compressive stress is very fast and therefore does not affect the overall deposition rate, and allows for densely stacked tensile and compressive layers, to be deposited.

All tests were performed using 4 inch, ISO standard silicon wafers, with thickness of 350 ± 25 μm. Samples were deposited using a coupled planar parallel electrode Multiplex Series PECVD (Surface Technology Systems, Ltd), with an electrode diameter of 24 cm. The system is equipped with a high frequency (HF) generator at 13.56 MHz and a low frequency (LF) generator at 308 kHz. The operating temperature of the shower head of the machine is 250 °C while the temperature of the chuck in which the wafer is placed during the deposition process is 300 °C. All depositions were performed with a chamber pressure of 900mTorr.

Annealing was performed on all samples in a standard Thermco MB71 furnace for 60 min at 400 °C in inert atmosphere with a 4.5 SLM N_2 flow, in order to simulate the thermal budget of the full device fabrication. Stress measurements, using the Stoney wafer curvature variation equation [15], were carried out before and after the annealing. Three profiles were measured for each sample along its diameter separated by an offset of 5 mm; the resulting stress data showed a standard deviation better than 3%. This standard deviation is valid for all stress data reported in tables 2 and 3.

The deposition rate of PECVD materials is known to be directly proportional to the RF power, and in the case of silicon nitride it is also directly proportional to the NH_3 flow rate [16]. Starting from a standard set of recipe parameters (HFb and LFb in table 1), previously identified [6, 7] and used to fabricate working CMUT devices [11–13] in different foundries and with different equipment, a number of modifications were made in order to explore the effect on residual stress and deposition rate. For high frequency silicon nitride it has been demonstrated that the residual stress is directly proportional to the ammonia rate, while it is inversely proportional to the RF power [17]. Low frequency nitride experimental data show that the NH_3 to SiH_4 ratio can be tuned to obtain a low stress layer [18]. Accordingly, double layer nitride was explored testing different power levels for the tensile (high frequency) nitride and implementing two compressive (low frequency) nitrides, with and without ammonia flow (*LFa* and *LFb* respectively in table 1).

In table 2, the stress measurement results of all layers are reported before (as deposited) and after annealing. As can be seen, there is a big difference in the deposition rates of the high and low frequency nitrides: low frequency is one order of magnitude faster and therefore will drive the thickness of the double layer stack. In order to compensate its compressive state, a highly tensile high-frequency nitride is required. HF samples exhibit a behavior in agreement with literature, having lower tensile stress for higher power values.

We chose the sample *HFb* as a compromise: its stress is 11% lower with respect to sample *HFa* but has a deposition rate 119% higher.

The addition of ammonia in low frequency nitride brings both a promising increase in the deposition rate (14%) and a slight stress reduction of the deposited layer, but the stress after annealing is 20% higher than the ammonia free LF nitride. We put priority on stress rather than deposition rate and so, we chose the *LFb* as a candidate for the double layer nitride stack.

Considering the requirements for CMUT residual stress, the second combination (*LFb/HFb 2*) reported in table 3 is the best candidate for double layer approach, with an after-anneal stress of -86 MPa. The slightly compressive state can be further addressed with a fine tuning of the HF/LF ratio. The obtained deposition rate is 99 nm min^{-1}.

For the second option, based on previous studies [19], a slightly tensile mixed frequency layer was deposited and tested, with the parameters showed in table 4. Stress before and after annealing as well as deposition rate is reported in table 5: the residual stress of mixed frequency nitride is

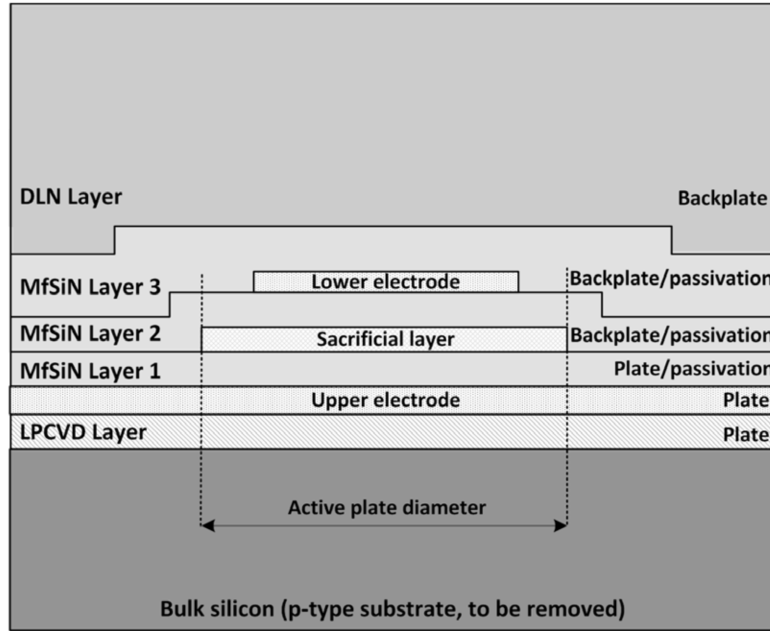

Figure 1. Schematic cross-section of the RFP CMUT device (picture not drawn to scale).

Table 1. Recipes for the double layer nitride constituents.

	Frequency	N2 flow	SiH4 flow	NH3 flow	Power
SiN sample	MHz	sccm[a]	sccm	sccm	W
HFa	13.56	1960	40	59	20
HFb	13.56	1960	40	55	60
HFc	13.56	1960	40	55	100
LFa	0.308	1500	100	60	300
LFb	0.308	1500	100	0	300

[a]Standard cubic centimeters per minute.

Table 2. Stress of the single nitride layers.

	Thickness	Dep. rate	As dep. stress	Stress after anneal
SiN sample	nm	nm/min	MPa	MPa
HFa	102	9.8	*456*	784
HFb	215	21.5	*378*	693
HFc	302	30.2	*316*	524
LFa	194	194	*−803*	−607
LFb	170	170	*−827*	−506

Table 3. Stress of double layer nitrides.

	Thickness	Dep. rate	As dep. stress	Stress after anneal
SiN sample	nm	nm/min	MPa	MPa
LFb/HFb 1	230/170	120.7	−354	−234
LFb/HFb 2	180/220	99.1	−163	−86
LFb/HFb 3	180/135	120.1	-331	−223

compliant with the CMUT application both before and after anneal, though the deposition rate is low compared to the double layer option.

To further qualify both nitride options, some test capacitors were fabricated on standard silicon 4 inches wafers with different areas from 0.25 mm^2 to 64 mm^2, having a 600 nm nitride dielectric layer deposited with both techniques. The nitride layer is stacked between two sputtered metal layers that provide the upper and lower electrode: the layers were deposited using an MCR Eclipse® PVD sputtering at 200 °C. To prevent hillock formation at the Aluminum-Si interface, Al/Ti and Al/Ti/TiN metallization multi-layers were used for the fabrication of test devices, adopting Ti and Ti/TiN as diffusion barriers [20, 21]. Simple leakage tests were performed, measuring test structures current when a 100 V_{dc} bias is applied to the electrodes. Both metal stacks had the same electrical performance, with high leakage currents in the case of double nitride layers and low leakage currents for mixed frequency nitride layers. Considering the 2.5 mm^2 structures, double layer devices had a current of more than 1 μA, while mixed frequency devices had leakage currents below 80 pA. Mixed frequency nitride electrical resistivity was measured in the range of 10^{13} Ω-cm. Electrical test results show that, despite its low deposition rate, mixed frequency nitride is the sole candidate for nitride layers one and two in figure 1. While the double layer nitride does not provide sufficient electrical

Table 4. Mixed frequency nitride deposition parameters.

	HF/LF	N2 flow	SiH4 flow	NH3 flow	Power
SiN sample	Sec	sccm	sccm	sccm	W
MF SiN	50/10	1960	40	40	50

Table 5. Mixed frequency nitride deposition rate and residual stress.

	Thickness	Dep. rate	As dep. stress	Stress after anneal
SiN sample	nm	nm/min	MPa	MPa
MF SiN	260	22.7	60	35

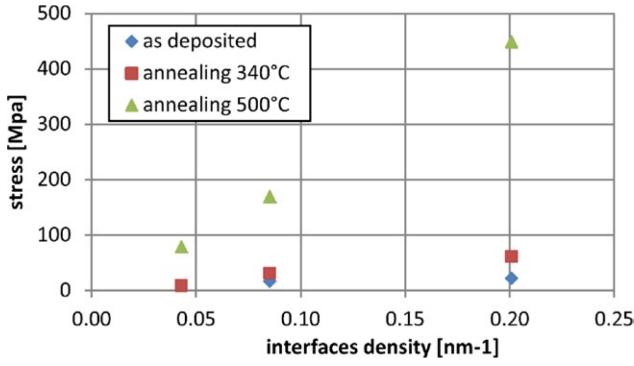

Figure 2. Mixed frequency PECVD SiN thin samples (~330 nm) residual stress.

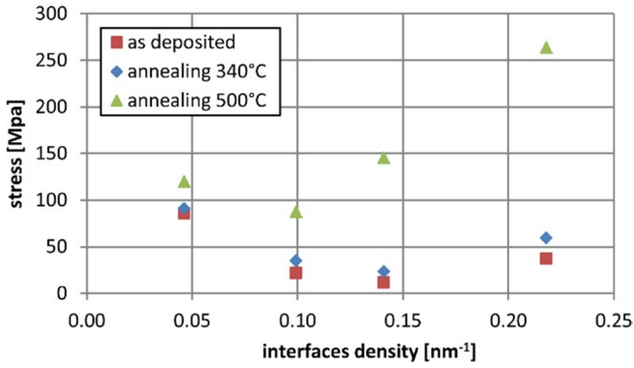

Figure 3. Mixed frequency PECVD SiN thick samples (~950 nm) residual stress.

insulation, it still holds as a back-plate nitride and for the third nitride deposition layer in the RFP CMUT (figure 1) as discussed in the introduction. In particular, given that the back-plate layer represents a large portion of the overall deposited thickness, DLN has to be preferred as a back-plate material because of its higher deposition rate (about 5 times that of MfSiN), which greatly affects the fabrication time and reliability. It has to be underlined that a tradeoff between stress and deposition rate was made for DLN in order to have a <100 MPa absolute value (which is widely accepted as low stress state) and a reasonably high deposition rate. The slightly compressive state of DLN is not considered critical as this layer is not to be part of the moving membrane.

Finally, it is worth noting that the physical and chemical changes in the layers composition and their stress characteristics due to switching from tensile to compressive stress, was further deepened in [30] by the same authors, using the XPS and SIMS analysis.

4. Study of MfSiN: effect of interfaces density and thermal treatments

Layers 1 and 2 of the RFP CMUT device are particularly critical for the performance of the device because they form the 'walls' of the internal cavity and the layer 1 becomes part of the vibrating membrane (together with the LPCVD nitride layer and the upper electrode) after bulk silicon removal. Thus a deeper analysis of the mechanical and structural properties of these layers is necessary.

A previous work by this team [19] was addressed to the study of compressive residual stress variation in MfSiN (mixed frequency silicon nitride) due to thermal cycling and how this interacts with the interfaces density of the film. As a compressive state is not suitable in any of the fabrication steps of a suspended structure, the present work addresses MfSiN with slightly tensile residual stress. Considering a deposition cycle as the sum of a single low frequency deposition plus a single high frequency deposition, the deposition process consists of the repetition of a given number of deposition cicles (DC). The interfaces density (ID), i.e. how densely the high and low frequency layers are stacked in the film, is then defined as [19]:

$$\mathrm{ID} = \frac{2 - \mathrm{DC} + 1}{t} \quad (1)$$

where DC is the number of deposition cycles performed during the deposition, and t is the total deposited thickness. The interfaces density was demonstrated to heavily affect the nitride stress variation under thermal budgets. In order to test the effect of interfaces density on tensile mixed frequency nitride for CMUT devices, we prepared a set of samples on standard 4 inches silicon wafers, fixing the HF/LF ratio at 5 and using the deposition parameters reported in table 4, and changing the interfaces density from 0.04 to 0.22. As the mixed frequency nitride deposition time is a multiple of the single cycle time, it was not possible to obtain the same thickness for all samples in each group, due to the different cycle times required for different interface densities deposition. We defined two thickness ranges: three samples named 'thin' with thickness in the range of 300–370 nm, while 4 'thick' samples with a thickness between 900 nm and 1000 nm. All samples were annealed at 340 °C and 500 °C for 30 min in inert atmosphere using the previously described equipment and parameters, in order to test the thermal stability of the layer. Stress measurements were carried out on the deposited layers, as well as after each annealing.

Thickness was also measured 'as deposited' and after annealing by means of interferometry and ellipsometry in order to monitor the well documented [22, 23] H_2 out-gassing and volume reduction of the nitride layer. The results are reported in figures 2 and 3. Thin layers (figure 2) have a steadily growing trend between residual stress and interfaces density, which is further marked after annealing. At an interfaces density above 0.8 nm^{-1} the stress after annealing is already above 100 MPa and not compliant with the device requirements (figure 2). Thick layers have a minimum stress value at 0.14 nm^{-1} of interfaces density both 'as deposited' and after the first anneal (figure 3). This minimum is shifted to 0.1 nm^{-1} of interfaces density after the second annealing: therefore this density appears to be optimal in terms of thermal stability. The same trend was already observed for slightly compressive layers of MF silicon nitride [19]: both thick (2 μm) and thin (260 nm) samples have a stress minimum at 0.04 nm^{-1} and 0.02 nm^{-1} respectively.

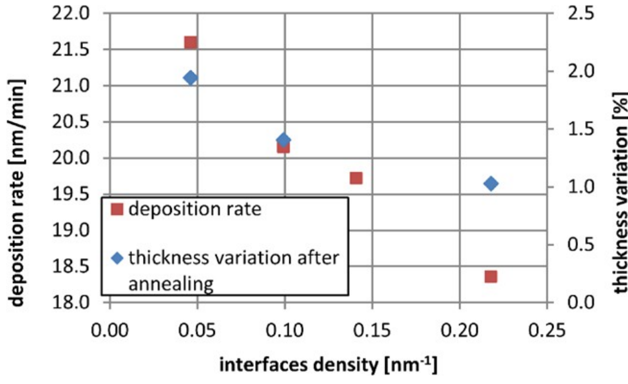

Figure 4. MF PECVD SiN thick samples (~950 nm) deposition rate and thickness variation after annealing.

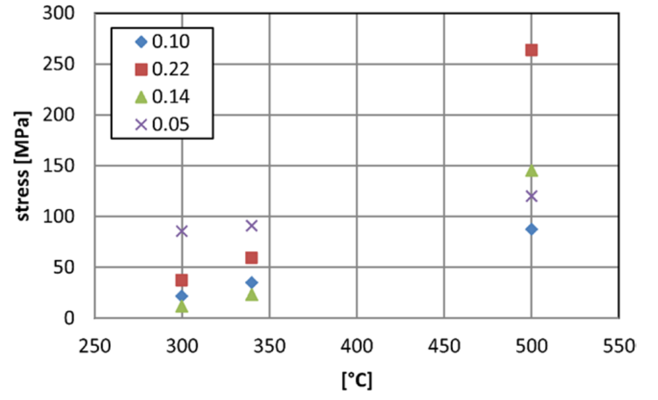

Figure 5. Thick samples (~950 nm) stress as a function of temperature for various interface densities.

Comparing the compressive and tensile nitrides (thick samples) it is evident that the initial stress state brings a major variation in the minimum point (0.04 nm^{-1} for compressive nitride, and 0.1 nm^{-1} for tensile nitride). Given this stress trend, we also suggest that thin tensile samples reported in figure 2 have a minimum which lays outside the measured range, at an ID value <0.04 nm^{-1}. It has to be noted that previously reported compressive MF silicon nitride [19], though reducing its stress upon annealing, is not compliant for the fabrication of a suspended membrane structure as the membrane layer stress has to remain tensile during all fabrication steps.

The overall effect of stress increase due to annealing and H_2 out-gassing is related to the fraction of H bonded in the film as Si–H [24]: the higher the Si-H bonds in 'as deposited' layers the more the stress increases by annealing. Data available in literature (dual frequency excitation plasma, nitride thickness 800–1000 nm, annealing at 500 °C for 10 min) match best with the thick samples, allowing an estimate of the Si–H bonded hydrogen fraction. High interfaces density (0.22 nm^{-1}) yields a stress variation of 220 MPa upon annealing, which corresponds to a fraction >70% [24]. At the other end, for low interfaces density (0.04 nm^{-1}), the stress variation is 40 MPa, and the fraction is <50%.

A correspondence between Si–H concentration and Si/N ratio exists for both low and high frequency PECVD silicon nitrides, as reported by Claassen *et al* [25]: assuming this relation valid for the mixed frequency deposition technique, the Si/N ratio ranges from 0.8 (@0.04nm^{-1}) to about 1 (@0.22 nm^{-1}). This assumption will be further discussed, analyzing refractive index data. Interfaces density affected also the deposition rate and thickness variation of the thick samples as reported in figure 4.

At low interfaces density the deposition rate is higher, following a semi-linear trend expressed by the relation:

$$D = 22.2 - (18.2 \bullet \mathrm{ID}) \quad (2)$$

where the deposition rate D is expressed in nm/min and the interfaces density ID is in nm^{-1}. This relation is not due to 'dead' time gaps during commutation between high and low frequency plasma: our setup was optimized in order to have an immediate switch between the two generators, which is confirmed by plasma luminescence being constantly visible.

Increasing the interfaces density also reduces the thickness variation after annealing: in figure 4 the variation between 'as deposited' thickness and final thickness (after both annealing cycles) is reported.

Thickness variation has been widely studied and is due to a combination of ss density increase and the release of hydrogen from Si–H and N–H bonds [25].

Assuming that the 'as deposited' stress can be related to the deposition temperature (300 °C), in figure 5 we report a plot of the various stress levels (300 °C is the 'as deposited' temperature, others refer annealing temperatures). This assumption implies the following conditions:

- All residual stresses are thermal (extrinsic).
- The annealing time is sufficient for a complete stress relaxation of the layer.

The second assumption is uphold by the fact that all annealing cycles are performed at temperatures higher than the deposition temperature and therefore a rearrangement of the layer is to be expected inducing a stress-free state during annealing. Thermal gradient stress equation [27] can fit the lowest ID (0.05 nm^{-1}) experimental data providing a rough estimate of both the thermal expansion coefficient (TCE) and the elastic modulus (E) of the 1 μm layer as follows:

TCE � $4.5 \cdot 10^{-6} K^{-1}$; E � 130 GPa

No fit is possible for this equation in the case of higher interfaces density data, which supports the idea that high ID layers suffer more from annealing induced chemical changes and out-gassing than the low ID layers.

Also, low ID layers (0.05 nm^{-1} and 0.1 nm^{-1}) exhibit a linear relation ($R^2 > 0.99$) between temperature T and residual stress S, in the form of:

$$S = a\,(\mathrm{ID}) \cdot T + b\,(\mathrm{ID}) \quad (3)$$

Assuming that a, and b functions of ID are both linear, the following empirical model is obtained, which describes the

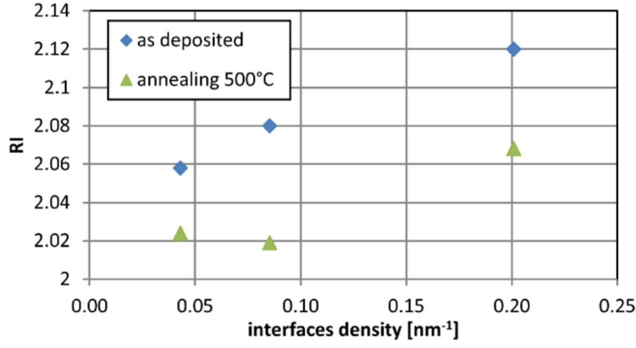

Figure 6. Refractive index (@633 nm) as a function of ID for thin samples.

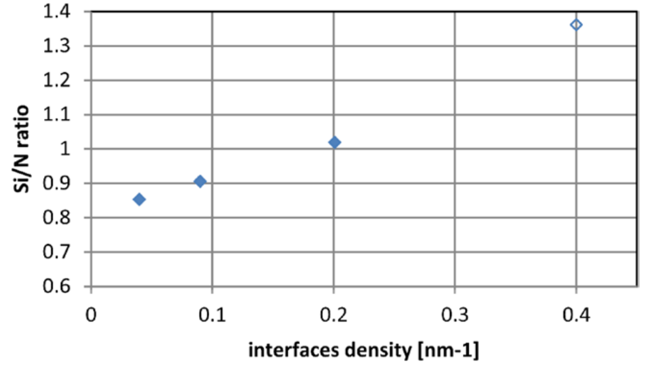

Figure 7. Calculated Si-N ratio as a function of ID for thin sample (circular point data from [30]).

relation between residual stress and annealing temperature as a function of interfaces density:

$$S = 3.064 \cdot \mathrm{ID} \cdot T + 0.0215 \cdot T - 2179.4 \cdot \mathrm{ID} + 141.43 \quad (4)$$

Given above assumptions, this relation is only valid for low interfaces density values ($\mathrm{ID} \leq 0.1\ \mathrm{nm}^{-1}$).

Refractive indexes (RI) were measured by means of ellipsometry using a variable angle spectra ellipsometer, after deposition and after each annealing.

A plot of refractive index data as a function of interfaces density for thin samples both as deposited and after annealing is reported in figure 6.

The expected RI increase upon annealing [26], due to the release of hydrogen and subsequent formation of Si–Si bonds, and is present in all samples. The as-deposited RI is almost linearly dependent on the ID, while after annealing an RI minimum appears at 0.1 nm^{-1} interfaces density. According to the model proposed by Bustarret *et al* [28] there is a direct proportion between refractive index and Si/N ratio in the form of:

$$\frac{Si}{N} = \frac{3}{4} \cdot \frac{n + n_a - 2n_s}{n_a - n} \quad (5)$$

where n is the measured refractive index, n_a is the hydrogenated amorphous silicon (a-Si:H) refractive index and n_s is the stoichiometric silicon nitride (Si_3N_4) refractive index.

Considering an average value of $n_a = 2.7$ [29] the Si/N ratio ranges from 0.85 (@0.04 nm^{-1}) to 1.02 (@0.22 nm^{-1}). This further supports the above estimate of Si/N ratio obtained from stress variation data and based on experimental data reported by Claassen [25], which suggest an identical range (from 0.8 (@0.04 nm^{-1}) to 1 (@0.22 nm^{-1})). Moreover, direct XPS analysis of mixed frequency nitride [30] deposited with an interfaces density of about 0.4 nm^{-1} reports a Si/N ratio of 1.36.

The Si/N values obtained with Bustarret model and XPS data are plotted in figure 7: all these data are referred to mixed frequency silicon nitride deposited with a SiH_4/NH_3 ratio of 1, and the Si/N variation depending on interfaces density variation only. This analysis suggests that the deposited mixed frequency silicon nitride is affected by interfaces density under several prospects. As deposited stress and refractive index (and derived Si/N ratio) increase with increasing ID, while the deposition rate decreases. Upon annealing, stress variation steadily increases with ID, while thickness variation tends to decrease. A minimum both in stress and refractive index after annealing at 500 °C is identified in the range $0.08 < \mathrm{ID} < 0.1\ \mathrm{nm}^{-1}$ (figures 3 and 6). This interfaces density is also an upper limit for thermal gradient stress equation [27] and for the above reported empirical model, describing stress as a function of annealing temperature and interfaces density. Layers with ID values higher than 0.1 nm^{-1} have a behavior which differs both from the extrinsic stress equation [27] and the empirical equations (3) and (4).

The presence of this 0.1 nm^{-1} 'sweet spot' for post-annealing stress requires further investigation but can be readily exploited in device fabrication.

5. CMUT device fabrication and preliminary testing

A complete CMUT device run was fabricated at FBK Microfabrication Laboratory in order to test the effectiveness of the optimized silicon nitrides. The process was transferred in the framework of a scientific collaboration between MTLab at Fondazione Bruno Kessler (FBK, Trento, Italy) and Aculab at University Roma Tre (Rome, Italy), in agreement with the patent [32] on the reverse fabrication process (RFP) technology [13, 31, 33–35] developed by Aculab.

A 192-element 12 MHz CMUT array, designed at Aculab for ultrasound imaging applications, was fabricated at FBK using the fabrication parameters reported in table 6 [36, 37].

Considering that the annealing tests reported in the previous paragraph simulate the thermal budget delivered on nitride layers during device fabrication, the 500 °C annealing stress results were taken into account as the best representative of the final residual stress of nitride layers in the fabricated CMUT device. Therefore all MF SiN layers reported in table 6 were deposited with an interfaces density of 0.1 nm^{-1} to obtain the highest thermal stability (figure 3). A 6-mask fabrication sequence was adopted, using standard projection microlithography, in order to fabricate the device which is schematically represented in figure 8(*a*). ISO standard 4 inch silicon wafers coated with 1 μm-thick low-stress Si-rich LPCVD silicon nitride, that forms part of the vibrating plate of the device, were used as substrates.

Table 6. CMUT array geometry parameters.

Parameter	Value
Membrane size (circular)	29 μm
Lower electrode size (circular)	22 μm
Vacuum gap (sacrificial layer thickness)	0.23 μm
SiN LPCVD membrane thickness (Si-rich)	1.00 μm
SiN layer 1 thickness (MfSiN)	0.35 μm
SiN layer 2 thickness (MfSiN)	0.35 μm
SiN layer 3 thickness (DLN)	0.50 μm
SiN backplate thickness (DLN)	4.0 μm
Upper electrode thickness (Al/Ti)	0.24 μm
Lower electrode thickness (Al/Ti)	0.26 μm
Array element width (azimuth)	112 μm
Array element length (elevation)	3 mm
No. of membranes per element	440
No. of elements per device	192

figures 8(*b*) and 9 report respectively a photo of a portion of a CMUT array element and an SEM image of the fabricated device section where cell layout and cavity are clearly visible.

Devices were diced using standard semiconductor sawing process, and then wire bonded and packaged at Aculab, following the RFP process, detailed in [34] and [35], in order to encapsulate the chip with a custom acoustic backing material, made of epoxy resin filled with tungsten and alumina powders, that also performs a glob-top for the electrical interconnections.

Finally, the bulk silicon substrate was completely removed by HNA wet etching to release the nitride membranes. The final device is pictured in figure 10.

Electrical impedance measurement of all the array elements, in air-coupled conditions, was carried out using an HP 4194A impedance analyzer (Hewlett-Packard, Palo Alto, CA). The measured data were processed in order to extract the average element capacitance and the series resistance that resulted to be respectively 13 pF and 18 Ω.

The electrical impedance of a single array element was measured biasing the element with a dc voltage. Several measurements were performed by varying the bias voltage between 50 V and 290 V in steps of 10 V. The impedance magnitude and phase plots are reported in figures 11(*a*) and (*b*), respectively.

As expected, a clear resonant behavior is observed. As usual, the element mechanical resonance frequency is evaluated as the frequency where the impedance magnitude modulation shows a minimum[4] [38]. The resonance frequency was extracted for each curve and plotted, as a function of the bias voltage, in figure 11(*c*).

Due to the well-known electrostatic spring-softening effect, the resonance frequency nonlinearly decreases, as the bias voltage increases, and asymptotically tends to zero as the collapse (pull-in) voltage is approached. A collapse voltage value between 300 V and 310V was extrapolated

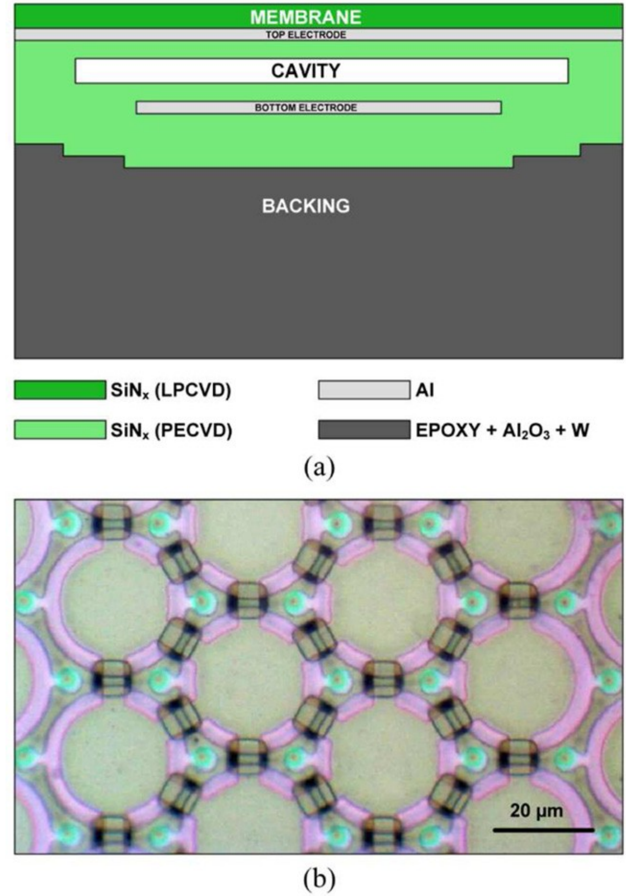

Figure 8. (*a*) Schematic representation of the CMUT fabricated by means of the reverse fabrication process (RFP), after the removal of the bulk silicon. (*b*) Optical microscopy of a portion of the fabricated device.

from the data set. This value is very close to the one predicted by finite element modeling (FEM), 310 V (see [37]), demonstrating the reliability of the overall fabrication process in terms of dimensional accuracy of the thickness of the deposited films. It can be further observed that, for high bias voltages, the impedance curves show non-ideal trend. In fact, the unevenness of the deposited films leads to a difference among the resonance frequency of the single cells that compose one array element. Such difference is amplified by the electrostatic non-linearity and becomes more significant as the biasing voltage approaches the collapse voltage. Anyway, in practical operating conditions, i.e. in water-coupled operation where the fluid mechanical load heavily damps the CMUT, such difference disappears. Moreover, in the present case, the phenomenon is negligible for bias voltages below 250 V, which represents the typical operating regime of CMUTs for ultrasound imaging applications.

To validate the described fabrication technology, we report in table 7 a comparison between the CMUT fabricated in this paper (A) and a CMUT (B) presented by some of the authors of this paper in [36, 37], and the data predicted by the FEM model.

[4] The electrical impedance of a vibrating plate exhibits a minimum at a frequency corresponding to the mechanical resonance frequency of the series mechanical RLC equivalent circuit. The same impedance exhibits a maximum at a frequency slightly above the mechanical resonance frequency. This impedance maximum (sometimes described as 'antiresonance') corresponds to the parallel resonance of the RLC equivalent circuit.

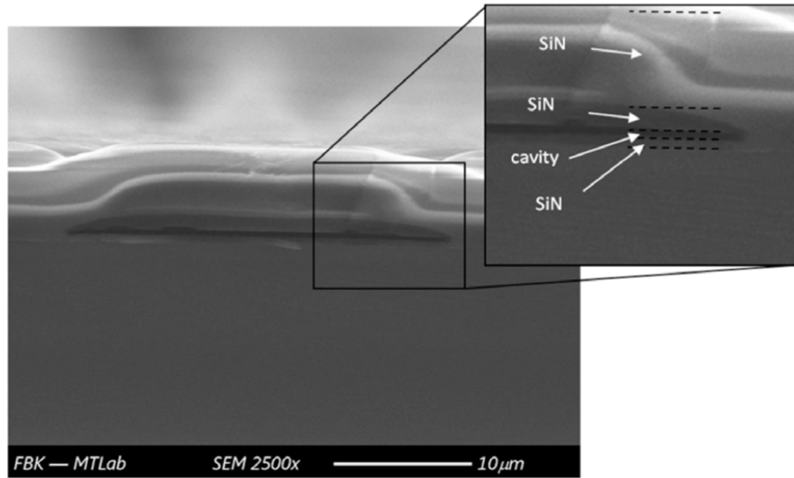

Figure 9. SEM image of the device section.

Figure 10. Image of a CMUT array bonded to a rigid-flex PCB and provided with a backing material.

The comparison is possible because we used the same mask set and same film thicknesses, but different SiN recipes. Previously reported devices were aimed at fingerprint imaging: this being an experimental field of application for CMUT, we do not consider it suitable for benchmarking, therefore we hereby report a direct comparison of the CMUT key parameters, independent of the application.

As we stated previously, and in [37], the model predicts the collapse voltage to a value of 310V, using material parameters available in literature: the actual realization is very close to this prevision. Considering that the bulk silicon removal and subsequent packaging was performed in the same lab and under the same process conditions both for CMUT (A) and (B), the only difference between the two devices is indeed the PECVD silicon nitride. One can appreciate how influent this change is in terms of performance, even though the main membrane is identical in both cases. Unlike previously suggested [37], the difference between simulated and measured collapse voltage for CMUT (B) is not in a thickness variation of the LPCVD membrane but just due to the mechanical behavior of the PECVD nitride (SiN layer 1 in figure 1). Indeed, the better quality of the MfSiN silicon nitride obtained during this work has validated the FEM results, obtained with literature material parameters.

A further confirmation of the quality of the developed silicon nitride is given by the considerable difference in the measured average resonance frequency. The SiN layer 1, which participates in the active membrane layer, is actually stiffer than that used in the past transducers, and approaches substantially to the values predicted by the FEM model in [37]. Finally, the device was tested in a dedicated water tank setup [33, 34]. Pulse-echo measurements were performed in order to characterize the transducer two-way transfer function. The CMUT array was immersed in water facing a stainless steel planar reflector placed at a distance of 14 mm. A Panametrics 5800PR pulser/receiver (Panametrics, Inc., Waltham, MA) was used to excite the CMUT array element, biased with 210 V_{dc}. The received echo waveform and its FFT spectrum are depicted in figure 12. The frequency response was found to be centered at 12.2 MHz with a −6 dB fractional bandwidth of 100%, as predicted by FEM [37].

6. Conclusions

We present an analysis of two technology options to achieve a high deposition rate, low stress PECVD silicon nitride to be used in CMUT fabrication. A tradeoff between deposition rate, residual stress, and electrical properties is presented. A double layer of silicon nitride with a deposition rate of ~100 nm min^{-1} and low compressive residual stress is obtained, which is suitable for the fabrication of the thick nitride layer used as mechanical support. A mixed frequency nitride with compliant insulating performance is analyzed: a complete characterization is reported in terms of interfaces density influence on residual stress, refractive index, deposition rate, and thickness variation. The best interfaces density, which ensures excellent thermal stability, was found to be in the range between 0.08–0.1 nm^{-1}. Simple linear equations are proposed to describe the relation between interfaces density

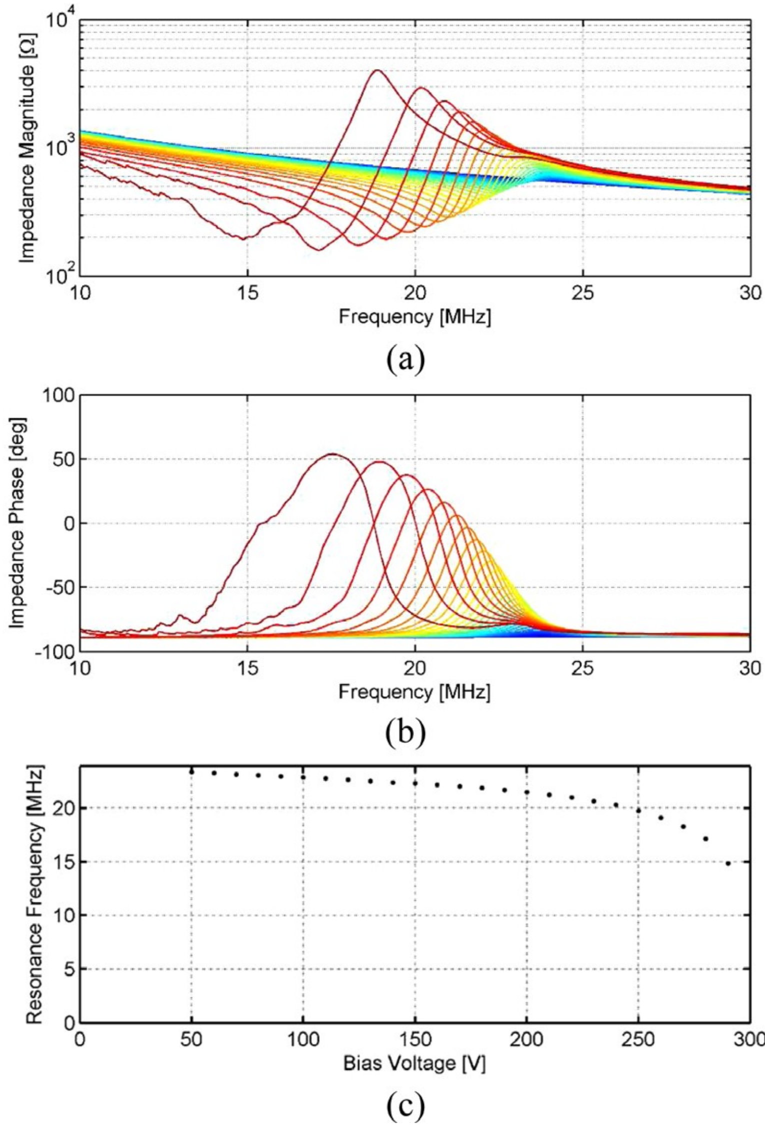

Figure 11. Electrical impedance magnitude (*a*) and phase (*b*) of a CMUT array element operating in air, measured varying the bias voltages from 50 V (blue) to 290 V (red) in steps of 10 V. (*c*) Mechanical resonance frequency as a function of the bias voltage.

Table 7. Comparison.

	CMUT A (this paper)	CMUT B [36, 37]	FEM model
Collapse Voltage	~300 V_{dc}	~250 V_{dc}	310 V_{dc}
Average Resonance Freq. (@70% of collapse voltage, in air)	21 MHz	18 MHz	20.9 MHz
% Relative Stand. Dev. of Resonance Freq.	1.54	1.28	0.0

and deposition rate, and to model the residual stress as a function of the annealing temperature for interfaces density below 0.1 nm^{-1}. A relation between interfaces density and Si/N ratio of 'as deposited' nitride is proposed, based on refractive index analysis and literature results. A 192-element 12 MHz CMUT array was fabricated, using the optimized nitrides and its performance was tested, demonstrating full functionality

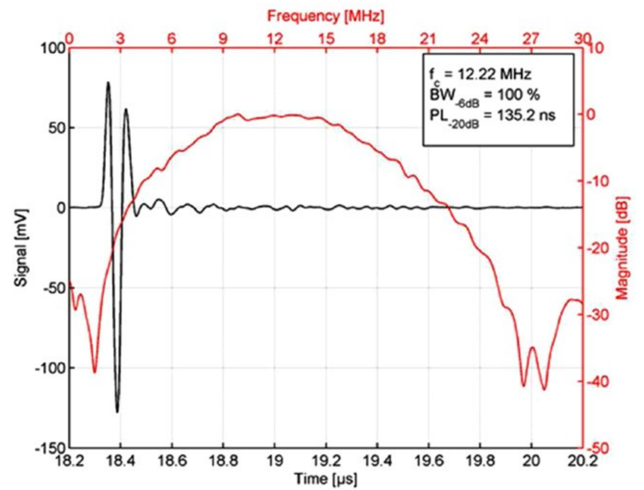

Figure 12. Pulse-echo response of a CMUT array element operating in water.

and good performance. The measured characteristics were in a good agreement with the FEM model of the device, demonstrating the reliability of the overall fabrication process in terms of dimensional accuracy of the thickness of the deposited films. The optimized materials are expected to allow for a faster and more reliable fabrication of RFP CMUT devices, enabling thick support layers to maximize the performance of the transducer.

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References

[1] Haller M I and Khuri-Yakub B T 1994 A surface micromachined electrostatic ultrasonic air transducer *IEEE Int. Ultrason. Symp. (Cannes, France)* vol 2 pp 1241–4
[2] Soh H T, Ladabaum I, Atalar A, Quate C F and Khuri-Yakub B T 1996 Silicon micromachined ultrasonic immersion transducers *Appl. Phys. Lett.* **69** 3674–3676
[3] Ergun A S, Huang Y, Zhuang X, Oralkan O, Yaralıoglu G G and Khuri-Yakub B T 2005 Capacitive micromachined ultrasonic transducers: fabrication technology *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **52** 2242–58
[4] Huang Y, Ergun A S, Hagstrom E, Badi M H and Khuri-Yakub B T 2003 Fabricating capacitive micromachined ultrasonic transducers with wafer-bonding technology *J. Microelectromech. Syst.* **12** 128–37
[5] Tsuji Y, Kupnik M and Khuri-Yakub B T 2010 Ultrasonics Low temperature process for CMUT fabrication with wafer bonding technique *Proc. IEEE Intl. Ultrason. Symp. (San Diego, CA)* pp 547–50
[6] Memmi D, Foglietti V, Cianci E, Caliano G and Pappalardo M 2002 Fabrication of capacitive micromechanical ultrasonic transducers by low-temperature process *Sensors Actuators* A **99** 85–91
[7] Cianci E, Visigalli L, Foglietti V, Caliano G and Pappalardo M 2003 Improvements towards a reliable fabrication process for cMUT *Microelectron. Eng.* **67–68** 602–8
[8] Knight J, McLean J and Degertekin F L 2004 Low temperature fabrication of immersion capacitive micromachined ultrasonic transducers on silicon and dielectric substrates *IEEE Trans. Ultrason. Ferroelectr. Freq. Control* **51** 1324–33
[9] van de Ven E P, Connick I-W and Harrus A S 1990 Advantages of dual frequency pecvd for deposition of Ild and passivation films *Proc. of IEEE VLSI Multilevel Interconnection Conf.* (*Santa Clara, CA, 12-13 Jun 1990*) pp 194–201
[10] Pearce C W, Fetcho R F, Gross M D and Koefer R F 1992 Characteristics of silicon nitride deposited by plasma-enhanced chemical vapor deposition using a dual frequency radio-frequency source *J. Appl. Phys.* **71** 1838–41
[11] Savoia A, Caliano G, Carotenuto R, Longo C, Gatta P, Caronti A, Cianci E, Foglietti V and Pappalardo M 2005 Enhanced echographic images obtained improving the membrane structural layer of the cMUT probe *IEEE Intl. Ultrason. Symp. (Rotterdam, The Netherlands)* pp 1960–3
[12] Cianci E, Schina A, Minotti A, Quaresima S and Foglietti V 2006 Dual frequency PECVD silicon nitride for fabrication of CMUTs' membranes *Sensors Actuators* A **127** 80–7
[13] Caliano G, Caronti A, Savoia A, Longo C and Pappalardo M, Cianci E and Foglietti V 2005 Capacitive micromachined ultrasonic transducer (cMUT) made by a novel reverse fabrication process *IEEE Intl. Ultrason. Symp. (Rotterdam, The Netherlands)* pp 479–82
[14] Caliano G, Pappalardo M, Caronti A, Minotti A, Foglietti V, Cianci E and Nencioni A 2010 Surface micromechanical process for manufacturing micromachined capacitive ultra-acoustic transducers and relevant micromachined capacitive ultra-acoustic transducers *Italian Patent* No. IT2005RM00093, 04/03/2005
[15] Stoney G G 1909 *Proc. R. Soc. Lond. Ser.* A **82** 172
[16] Ibok E, Santana M and Garg S 1994 Deposition, material and optical properties of UV-transimmisve PECVD silicon nitride films *Proc. of the Third Symp. on Silicon Nitride and Silicon Dioxide Thin Insulating Films* pp 385–94
[17] Mackenzie K D *et al* 2004 *Characterization & Optimization of Low Stress PECVD Silicon Nitride for Production GaAs Manufacturing* (Unaxis USA Inc)
[18] Chiou W, Lee B, Ho B, Hu G, Hua C H, Tu D W and Liu J 2005 *Dense Silicon Nitride for MMIC Protection with Low Compressive Stress, Grown in LF PECVD* (MANTECH)
[19] Picciotto A, Bagolini A, Bellutti P and Boscardin M 2009 Influence of interfaces density and thermal processes on mechanical stress of PECVD silicon nitride *Appl. Surf. Sci.* **256** 251–5
[20] Wu W, Tsai K, Chao C, Chen J and Ou K 2005 Novel Multilayered Ti/TiN diffusion barrier for Al metallization *J. Electron. Mater.* **34** 1150–6
[21] Gleason E F, Cohen S S and Wyatit P W 1993 The reactivity of thin titanium films towards aluminum and the N-O-N insulator stack, and its effects on the composition and properties of voltage programmable links *MRS Proc.* **311** 45
[22] Sopori B 2003 Silicon nitride processing for control of optical and electronic properties of silicon solar cells *J. Electron. Mater.* **32** 1034–42
[23] Bousbih R, Dimassi W, Haddadi I and Ezzaouia H 2012 The effect of thermal annealing on the properties of PECVD hydrogenated silicon nitride *Phys. Status Solidi* C **9** 2189–93
[24] Nagy F A 1997 Hydrogen redistribution in annealed silicon nitride thin films deposited by PECVD *Master's Thesis* San José State University, CA
[25] Claassen W A P, Valkenburg W G J N, Willemsen M F C and Wijgert W M v d 1985 Influence of deposition temperature, gas pressure, gas phase composition, and RF frequency on composition and mechanical stress of plasma silicon nitride layers *J. Electrochem. Soc.* **132** 893–8
[26] Wright D N, Marstein E S and Holt A 2007 Effect of annealing on Pecvd silicon nitride films *22nd European Photovoltaic Solar Energy Conf.* (*Milan, Italy, 3-7 September 2007*)
[27] Murarka S 1993 *Metallization Theory and Practice for VLSI and ULSI* (Butterworth-Heinemann) p 65
[28] Bustarret E, Bensouda M, Habrard M C, Bruyère J C, Poulin S and Gujrathi S C 1988 Configurational statistics in a-SixNyHz alloys—A quantitative bonding analysis *Phys. Rev.* B **38** 8171–84
[29] Lin S H, Chan Y C, Webb D P and Lam Y W 1999 Optical characterization of hydrogenated amorphous silicon thin films deposited at high rate *J. Electron. Mater.* **28** 1452–6

[30] Vanzetti L, Barozzi M, Giubertoni D, Kompocholis C, Bagolini A and Bellutti P 2006 Correlation between silicon-nitride film stress and composition: XPS and SIMS analyses *Surf. Interface Anal.* **38** 723–6

[31] Coppa A, Cianci E, Foglietti V, Caliano G and Pappalardo M 2007 Building CMUTs for imaging applications from top to bottom *Microelectron. Eng.* **84** 1312–5

[32] Caliano G, Caronti A, Pappalardo M, Cianci E, Foglietti V, Minotti A, Nencioni A 2008 Surface micromechanical process for manufacturing micromachined capacitive ultra-acoustic transducers and relevant micromachined capacitive ultra-acoustic transducers *U.S. Patent* US2008212407

[33] Caronti A *et al* 2008 Curvilinear capacitive micromachined ultrasonic transducer (CMUT) array fabricated using a reverse process *IEEE Intl. Ultrason. Symp.* (Beijing, China) pp 2902–5

[34] Savoia A, Caliano G and Pappalardo M 2011 Performance optimization of a high frequency cMUT probe for medical imaging *10th Int. Workshop on Micromachined Ultrasonic Transducers* (*Salerno, Italy, 16–17 June 2011*)

[35] Savoia A, Caliano G and Pappalardo M 2012 A CMUT probe for medical ultrasonograpy: from microfabrication to system integration *IEEE Trans. Ultrason. Ferroelectron Freq. Contr.* **59** 1127–38

[36] Savoia A, Caronti A, Longo C, Caliano G, Carotenuto R, Iula A and Pappalardo M 2010 Design and fabrication of a cMUT probe for ultrasound imaging of fingerprints *IEEE Intl. Ultrason. Symp. (San Diego, CA)* pp 1877–80

[37] Lamberti N, Savoia A, Caliano G and Iula A 2011 A high frequency cMUT probe for ultrasound imaging of fingerprints *Sensors Actuators* A **172** 561–9

[38] Edmonds P D (ed) 1981 *Ultrasonics (Methods of Experimental Physics*) vol **19** (New York: Academic Press) ISBN 9780124759619