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A Cost-Effective Adaptive Rectifier for Low Power Loosely Coupled Wireless Power Transfer Systems

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***Abstract*— This paper introduces an integrated receiver circuit based on a full-wave adaptive rectifier (AR). It achieves complex impedance matching and enables complexity and cost reduction in resonant wireless power transfer (WPT) systems. The conversion and system efficiency based on this AR receiver are theoretically compared with other receiver architectures by using a WPT system model including all conduction and switching losses. Fabricated in a 0.18-μm BCD process, the AR receiver chip operates at 6.78 MHz, occupies 3-mm^2 active die area and includes control and supporting circuitry for independent control of the reactive and resistive parts of the load impedance. The chip was tested in a 2.5-W WPT system, purposely built with extremely low coupling coefficient to enable spatial freedom. Experimental data show that the proposed AR chip achieves up to 96% efficiency. In addition, when used in a WPT system, it delivers 2.15 W with 50.3% system efficiency and 1.96 W with 29% system efficiency for coupling coefficients $k = 0.085$ and $k = 0.03$, respectively.**

***Index Terms*— Wireless power transfer, resonant power conversion, adaptive tuning, impedance matching.**

I. Introduction

IN THE last decade, the growing number of personal electronic devices that the average person relies on has created a large demand for Wireless Power Transfer (WPT). The development and commercialization of this technology for consumer applications have also opened opportunities in several markets, such as electric vehicles [1], household appliances [2], RF energy harvesting systems [3], [4] and biomedical implants [5], [6]. Among all WPT technologies, magnetic induction has proliferated into many electronic systems. The wide acceptance of magnetic induction as a WPT mechanism is in part due to good tolerance to object misalignment, safety for living beings [7], and to the possibility of using extremely thin coils as transmitter and receiver antennas [8]. In many WPT applications, the most pressing needs are maximizing performance and minimizing footprint and cost. In order to minimize the size of coils and other passive components it is advantageous to operate at higher frequencies. Complying with near and far field regulatory specifications is easier if the operating frequency is constant and within one of the Industrial Scientific Medical (ISM) frequency bands [9]. For these reasons, many end-equipment manufacturers are interested in WPT solutions operating at 6.78 ±0.015MHz (the lowest frequency ISM band) [10].

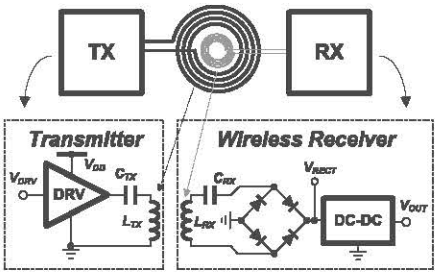

Fig. 1. Typical high-frequency wireless power transfer system, where a receiver post-regulator is used to control output voltage or current.

A typical high frequency WPT system is shown in Fig. 1. In order to maximize the performance in such systems, it is beneficial to use reactive networks, which make these systems operate in a resonant fashion and help to achieve source and load impedance matching [11]–[14]. However, tuning of such networks can be challenging, especially when transmitter and receiver coils are poorly coupled and when their relative position and orientation vary substantially [15]–[17].

Adaptive impedance matching techniques operating at a fixed frequency are employed to maintain high efficiency at a single frequency [18]. There are several adaptive impedance matching techniques aiming at maximizing system performance and efficiency, as well as increasing amount of output power [19]–[21]. Although adaptive frequency tuning approaches can be adopted for maintaining power transfer efficiency [22], they have limited applications since the resonant frequency allowing impedance tuning should be placed within allowed bandwidth. Also, additional circuitry at the transmitter and receiver is needed [13], [23]. In addition, a DC-DC converter has been shown to function as variable impedance by changing the duty-cycle of the switching devices. It has been utilized as an impedance matching circuit to decrease the power loss and increase the efficiency [24]–[26]. However, this technique only helps to adjust the resistive part of the load impedance while its reactive part is not controlled and results in less optimum efficiency. Alternatively, a phase shift control technique has been used to regulate output power when

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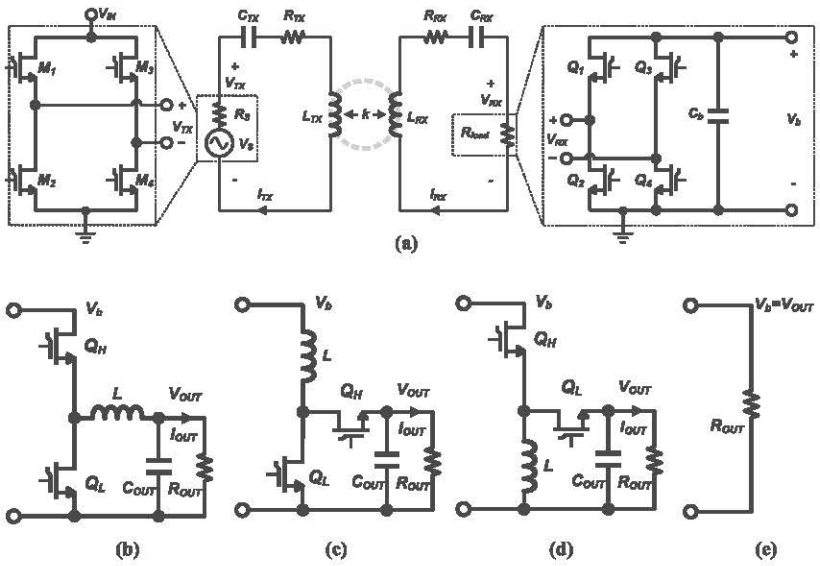


Fig. 2. (a) Example of SS WPT system usable with PRR and AR architectures. (b) to (e) Possible architectures used at rectifier output stage.

input power varies [27], [28]. Since this technique does not allow for independent control of the resistive and reactive parts of the equivalent load impedance, it does not yield the maximum achievable power efficiency. The resistive and reactive parts of the impedance can be independently controlled by adjusting the phase-shift of the active rectifier and its output voltage level. Thus, the transferred power efficiency and the amount of transferred power can be maximized as described in [19]. In this paper a low-cost receiver chip for low-power WPT systems, implementing this Adaptive Rectifier (AR) concept, is proposed. The chip was specifically developed for a 2.5W WPT battery charger targeted for consumer electronic (wearable devices, biometrics and watches), whose power levels are within few Watts. The issue of minimizing system size and cost is addressed by operating at 6.78 MHz and integrating the most of the control circuit. The proposed hardware solution is ideally suited for single-receiver systems but it can be extended to multi-receiver ones. In the proposed AR-based receiver, the phase-shift technique discussed in [19] is employed to realize an adaptive impedance matching. While the results of a prototype operating at 100 kHz of resonance frequency are reported in [19], such work does not introduce any integrated circuit solution to the AR concept and does not cover the challenges of high frequency operation in WPT systems. In this paper, a PLL-based control architecture has been introduced to implement the AR concept for high frequency operation while achieving high power density and efficiency for WPT systems operating at 6.78MHz. PLL-based closed-loop control automatically compensates for Process-Voltage-Temperature variations of delays in the design and provides robust control against variations in the system and IC.

The paper is organized as follows. In Section II, the efficiency and maximum input/output voltage range of WPT systems with Post-Regulated Rectifier (PRR) and AR architectures are compared. In Section III, the proposed AR receiver chip hardware implementation is presented. Section IV reports the experimental results relevant to the proposed AR receiver chip and compares this receiver to other prior art solutions.

II. PRR vs AR WPT Systems

The Series-Series (SS) resonant WPT system shown in Fig. 2 consists of a transmitter (TX) and a receiver (RX). The TX has an inverter, a series capacitor C_{TX} and a coil L_{TX}. The RX has a coil L_{RX}, a series capacitor C_{RX} and a full-bridge rectifier connected to the DC load R_{OUT}, through PRR architectures (Fig. 2(b)–2(d)) or directly through the AR architecture (Fig. 2(e)). Despite an SS WPT system is assumed for this analysis, the concepts discussed herein are general and can be extended to other coil compensation networks too. The TX coil sees the inverter output as a voltage source V_s, with a series resistance R_s, whereas the RX coil sees the rectifier input as an equivalent load resistance R_{load}. The inverter generates a square-wave voltage at the input of the TX coil at the WPT system resonance frequency $\omega = 2\pi f_w$. In PRR-WPT systems, the full-bridge rectifier operates with duty-cycle $D = 100\%$ so that the square-wave receiver voltage V_{RX} is synchronous with the rectifier current I_{RX}, as shown in Fig. 3(a). The load voltage/current regulation is then achieved by means of the adjustment of the post-regulator duty-cycle. In AR-WPT systems, the square-wave receiver voltage V_{RX} can have a phase lead/lag φ with respect to the rectifier current I_{RX}, and its duty-cycle D can theoretically vary from 0 to 1, as shown in Fig. 3(b). The load voltage/current regulation is achieved by means of the adjustment of the AR duty-cycle. Whichever rectifier architecture is adopted, if C_{TX} and C_{RX} are tuned to resonate with L_{TX} and L_{RX} at the system frequency, the current, voltage and power delivered by the receiver coil can be expressed as presented in [19] and given in (1):

$$I_{RX} = \frac{\omega L_m V_s}{(R_s + R_{TX})(R_{load} + R_{RX}) + \omega^2 L_m^2}$$

$$V_{RX} = R_{load} I_{RX}; \quad P_{RX} = \frac{1}{2} V_{RX} I_{RX} \tag{1}$$

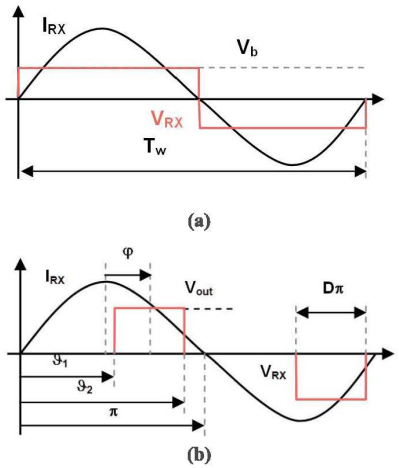


Fig. 3. Output waveforms of SS WPT systems with (a) PRR topologies and (b) AR topologies.

where R_{load} is the equivalent load resistance at the rectifier input, R_s is the equivalent source resistance, $L_m = k\sqrt{(L_{TX}L_{RX})}$ is the mutual inductance between coils, $V_s = 4V_{IN}/\pi$ is the first harmonic amplitude of the TX coil voltage, and I_{RX} and V_{RX} are the first harmonic amplitudes of RX coil current and voltage. Similarly, the current, voltage and power at the input of TX coil can be formulated as in (2):

$$I_{TX} = \frac{V_s(R_{load}+R_{RX})}{(R_s+R_{TX})(R_{load}+R_{RX})+\omega^2 L_m^2}$$
$$V_{TX} = V_s - R_s I_{TX}; \quad P_{TX} = \frac{1}{2}V_{TX}I_{TX} \tag{2}$$

From (1) and (2), given the DC load voltage V_{OUT} and current I_{OUT} requirements, the performance of the WPT system is determined by the receiver architecture and control, which influence the value of R_{load}. The receiver architecture and control also determine the ease of hardware implementation. The features to analyze in order to assess the performance and hardware cost of receiver architecture are: output power, conversion efficiency, resulting WPT system efficiency, current, voltage and duty-cycle operation ranges, part count, FET voltage rating and driving voltage. Analyzing these features provides the elements to understand when and why the AR solution can be preferred to the PRR ones. For this purpose, a model of the receiver load resistance R_{load} and of the entire WPT system, including all power losses, has been developed as follows. Given the rectifier architecture, the power delivered by the RX coil includes the rectifier and the post-regulator losses (for PRR solutions) and the power P_{out} delivered to the DC load R_{out}. Consequently, it can be expressed as follows in (3):

$$P_{RX} = R_{load}I_{RX,rms}^2 = R_{load}\frac{I_{RX}^2}{2} = P_{rect} + P_{post} + P_{out} \tag{3}$$

Let us assume that the rectifier and post-regulator use the same power FETs. Then, (3) can be rewritten as in Table I, for PRR and AR receiver architectures, where R_{ds}, Q_g, t_{sw}, V_{SD} and t_{dt} are the FET channel resistance, gate charge, switching time and body-diode forward voltage and dead-time, respectively. Also, D is the post-regulator or rectifier duty-cycle ($D' = 1 - D$) and f_s is the post regulator switching frequency. Replacing expressions in the third column of Table I into equations in the second column of Table I provides a second set of equations, connecting R_{load} and I_{RX} for each rectifier architecture, which can be solved together with (1), also connecting R_{load} and I_{RX}, to obtain the entire WPT system solution for any value of the duty-cycle D, in the feasible range [D_{min} >0, D_{max} <1].

The model discussed above can be used to theoretically demonstrate that the efficiency performance of the AR solution in loosely coupled WPT systems is comparable to the best one among PRR solutions in terms of WPT system efficiency, while offering the advantage of lower part count, wider operation range and FET selection. As an example, a WPT system with f_w = 6.78 MHz, V_{TX} = 8 V, R_s = 0.3 Ω, L_{TX} = 7.5 μH, R_{TX} = 2.13 Ω, L_{RX} = 0.95 μH, R_{RX} = 1.15 Ω, $C_{TX} = (\omega L_{TX})^{-1}$, $C_{RX} = (\omega L_{RX})^{-1}$, and k = 0.06, is considered in a charger configuration. Such WPT system is supposed to charge a Lithium battery from 3.3 V to 4.3 V, through a constant-current phase at 0.45 A, followed by a constant-voltage phase at 4.3 V. Four receiver architectures are considered including buck, boost and buck-boost PRR and AR. All architectures are assumed to use the Vishay FET Si2372DS [29], both for the rectifier and the post-regulators.

For each feasible operating point (V_{OUT}, I_{OUT}), the rectifier conversion efficiency and the WPT system efficiency have been calculated by using the aforementioned model for PRR and AR architectures. The results are shown in Fig. 4, where the white lines represent the locus of battery operating points during the charging process, which is stopped at 0.1 A, the minimum current the AR rectifier can deliver in continuous mode. The values of the rectifier conversion efficiency, the bulk voltage V_B and the WPT system efficiency at the three corners of the charge line are highlighted in the plots.

Based on the developed model, the buck and buck-boost PRR architectures allow for the widest voltage and current operability ranges. The buck PRR yields very low WPT system efficiency, whereas the boost and buck-boost PRR enable the highest conversion and WPT system efficiency. However, the resulting boost and buck-boost PRR bulk voltage values are quite low (0.8 V to 1.1 V), thus requiring additional circuitry to generate the FET gate drive supply voltage. The AR architecture ensures a global WPT system efficiency comparable to boost and buck-boost PRR and allows an operability range between boost and buck-boost PRR. Also, it can use the rectifier output for FET gate drive to reduce the number of external components and resulting hardware complexity.

It is also worth noting that in PRR architectures, when the WPT system operates in no-load conditions, R_{load} goes to infinity, the rectifier output is open and consequently the receiver voltage V_{RX} rises to the peak value $V_{RX,pk} = \omega L_m V_s/(R_s + R_{TX})$, which yields a peak rectifier output voltage of $V_{b,pk} = \pi V_{RX,pk}/4$. Therefore, all power switches in the PRR architectures must be rated for the V_{bpk} voltage. In WPT-based personal electronic devices, such voltage is

TABLE I

POWER DELIVERED BY THE RECEIVER COIL EXPRESSED IN TERMS OF RECTIFIER AND PRR LOSSES AND OUTPUT POWER

	$R_{load}\frac{I_{RX}^2}{2}$ **for different AR and PRR architectures**	I_{out}
Buck	$\underbrace{R_{ds}I_{RX}^2}_{\substack{\text{rectifier}\\\text{conduction}\\\text{losses}}}+\underbrace{2V_{dr}Q_g(2f_w+f_s)}_{\substack{\text{rectifier and post-regulator}\\\text{gate losses}}}+\underbrace{\left(\frac{V_{out}}{D}t_{sw}+2V_{SD}t_{dt}\right)f_sI_{out}}_{\substack{\text{post-regulator switching losses}\\\text{and dead-time losses}}}+\underbrace{R_{ds}I_{out}^2}_{\substack{\text{post-regulator}\\\text{conduction}\\\text{losses}}}+\underbrace{R_LI_{out}^2}_{\substack{\text{inductor}\\\text{conduction}\\\text{losses}}}+\underbrace{R_{out}I_{out}^2}_{\substack{\text{output}\\\text{power}}}$	$\frac{2I_{RX}}{\pi D}$
Boost	$\underbrace{R_{ds}I_{RX}^2}_{\substack{\text{rectifier}\\\text{conduction}\\\text{losses}}}+\underbrace{2V_{dr}Q_g(2f_w+f_s)}_{\substack{\text{rectifier and post-regulator}\\\text{gate losses}}}+\underbrace{(V_{out}t_{sw}+2V_{SD}t_{dt})f_s\frac{I_{out}}{D'}}_{\substack{\text{post-regulator switching losses}\\\text{and dead-time losses}}}+\underbrace{R_{ds}\frac{I_{out}^2}{D'^2}}_{\substack{\text{post-regulator}\\\text{conduction}\\\text{losses}}}+\underbrace{R_L\frac{I_{out}^2}{D'^2}}_{\substack{\text{inductor}\\\text{conduction}\\\text{losses}}}+\underbrace{R_{out}I_{out}^2}_{\substack{\text{output}\\\text{power}}}$	$\frac{2D'I_{RX}}{\pi}$
Buck-boost	$\underbrace{R_{ds}I_{RX}^2}_{\substack{\text{rectifier}\\\text{conduction}\\\text{losses}}}+\underbrace{2V_{dr}Q_g(2f_w+f_s)}_{\substack{\text{rectifier and post-regulator}\\\text{gate losses}}}+\underbrace{\left(\frac{V_{out}}{D}t_{sw}+2V_{SD}t_{dt}\right)f_s\frac{I_{out}}{D'}}_{\substack{\text{post-regulator switching losses}\\\text{and dead-time losses}}}+\underbrace{R_{ds}\frac{I_{out}^2}{D'^2}}_{\substack{\text{post-regulator}\\\text{conduction}\\\text{losses}}}+\underbrace{R_L\frac{I_{out}^2}{D'^2}}_{\substack{\text{inductor}\\\text{conduction}\\\text{losses}}}+\underbrace{R_{out}I_{out}^2}_{\substack{\text{output}\\\text{power}}}$	$\frac{2D'I_{RX}}{\pi D}$
AR	$\underbrace{R_{ds}I_{RX}^2}_{\substack{\text{rectifier}\\\text{conduction}\\\text{losses}}}+\underbrace{4V_{dr}Q_gf_w}_{\substack{\text{rectifier}\\\text{gate losses}}}+\underbrace{2I_{RX}f_w(V_{out}t_{sw}+2V_{SD}t_{dt})\cos(\varphi)\cos\left(\frac{\pi D}{2}\right)}_{\text{rectifier switching losses and dead-time losses}}+\underbrace{R_{out}I_{out}^2}_{\substack{\text{output}\\\text{power}}}$	$\frac{2I_{RX}}{\pi}$

around 30V. With the AR architecture, instead, the no-load condition ensures the RX coil is shorted through the rectifier FETs, thus inherently limiting the maximum voltage peak and the FETs voltage rating.

III. AR ARCHITECTURE - PRINCIPLE OF OPERATION

The proposed AR IC solution implements the concept of a synchronous rectifier with independent control of voltage amplitude and phase shift. At system level, its principle of operation and efficiency optimization are discussed in [19], whereas an effective model for the power and efficiency analysis is given in [30]. The AR circuit is shown in Fig. 5, while Fig. 3(b) shows the current I_{RX} and voltage V_{RX} at the output of the receiver coil, where $\vartheta_1 = \pi(1-D)/2+\varphi$ and $\vartheta_2 = \pi(1+D)/2+\varphi$. The independent control of duty-cycle D and phase φ, with $0 \le D \le 1$ and $-\pi/2 \le \varphi \le \pi/2$, allows the modulation of the resistive and reactive components of the equivalent load impedance $\dot{Z}_{load} = \bar{V}_{RX}/\bar{I}_{RX}$ seen at the input of the rectifier [19]. $\dot{Z}_{load}$ is the ratio of the first harmonics of voltage v_{RX} and current i_{RX} respectively, thus combining the possibility of load power modulation and phase compensation.

The AR implementation proposed in this paper uses synchronization and pulse-width modulation circuits that detect the zero-crossing of i_{RX} and adaptively synthesize the desired duty-cycle D and phase φ of v_{RX}. To do that, it is necessary to introduce zero voltage intervals in the voltage v_{RX}. This is done by turning on Q_2 and Q_4 simultaneously. The FETs $Q_1, \ldots, Q_4$ are then driven so that the differential input voltage v_{RX} is characterized by the three-level periodic waveform shown in Fig. 3(b). As a result, two FETs are always in series with the RX coil in all switching states, whereas the DC load is connected to the RX coil only during the time corresponding to the πD phase. The FETs switching synchronization is realized in the proposed AR IC by employing the closed-loop control scheme shown in Fig. 6. Edge sensitive control of the rectifier in such systems allows for flexible duty-cycle control and provides improved system design freedom for different applications.

The implemented IC is comprised of a low-side zero-crossing detector, high-speed comparators, delay circuits, PLL, external compensation circuit, saw-tooth generator, PWM comparator, driver circuit and supporting circuitry (reference and internal rail generators).

Due to high-frequency operation and accurate timing control needed, it is critical to optimize the circuit blocks for both speed and accuracy with enough immunity to switching noise and coupling. Zero crossing detector circuit has to detect the zero crossings of the receiver current without producing any glitch or jitter, which may cause the PLL to lose its steady state operating point and may lead the close loop system to lose its regulation. Similarly, PLL circuit needs to quickly find the operating point and synchronize to its input by having wide bandwidth. Also, it needs to have high gain to have lower steady-state error and high noise rejection, which helps operating at high frequency with correct timing. The PWM comparator and ramp generators are also required to have enough speed and accuracy for high frequency operation and accurate timing control.

Power FETs are used in H-bridge configuration to achieve voltage rectification for AC to DC conversion. The timing of the full-bridge rectifier switching is determined by measuring the zero-current crossing of the RX current. In this design, this is achieved by monitoring the current through the low-side power FETs by using the zero-crossing detector to digitize the zero crossings of the receiver current. Due to switching

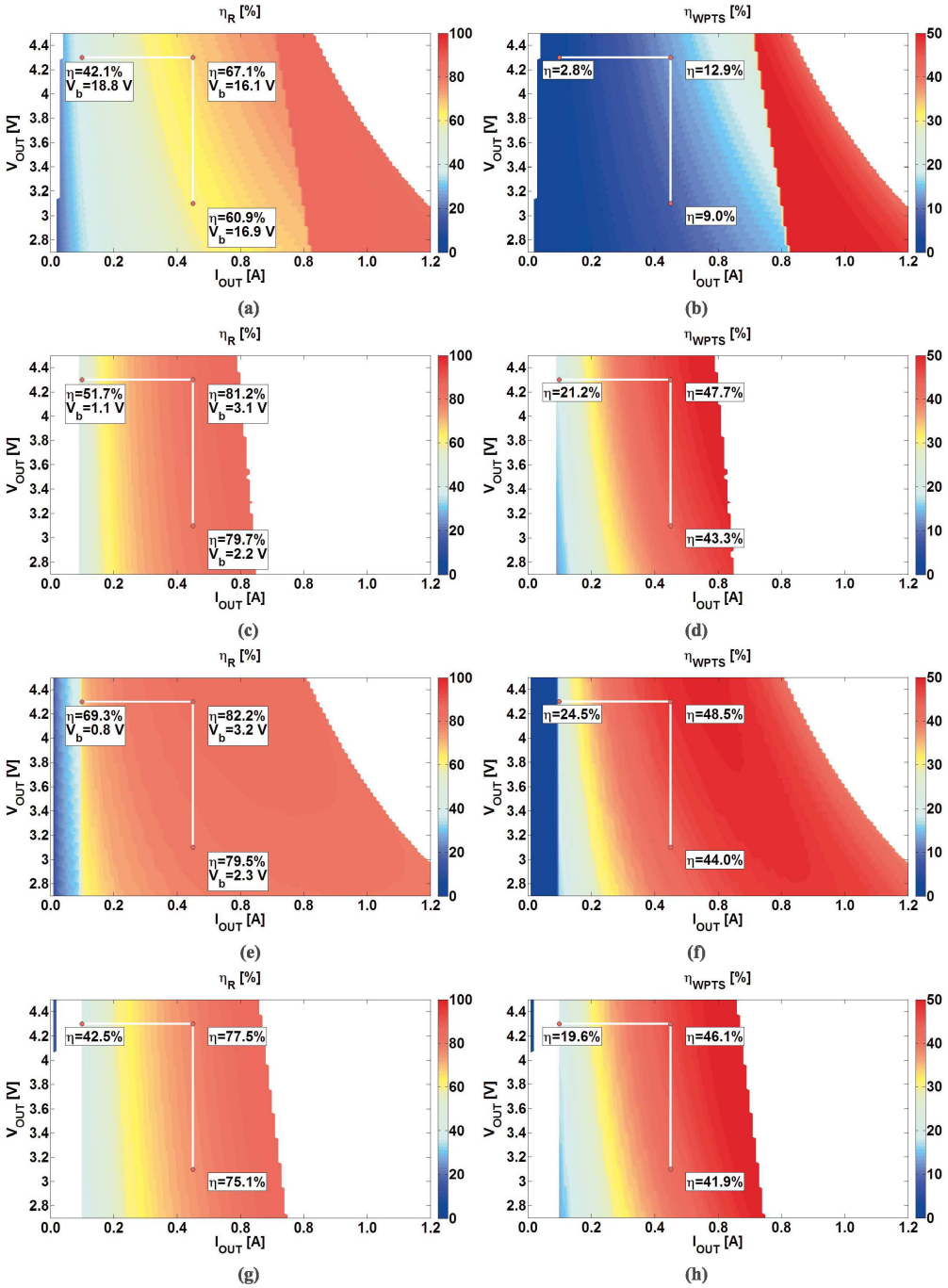


Fig. 4. Conversion efficiency for (a) Buck PRR receiver, (c) Boost PRR receiver, (e) Buck-boost PRR receiver and (g) AR receiver. System efficiency for (b) Buck PRR receiver, (d) Boost PRR receiver, (f) Buck-boost PRR receiver and (h) AR receiver.

noise and capacitive coupling, it is challenging to sense the RX current. This is addressed in this design by incorporating a deglitch circuit together with high-speed comparator for implementing the zero-crossing detector circuit. After that, a delay is introduced into the sensed zero-crossing signal and the sensed gate drive signals. In this way, either phase lead or lag can be controlled in the AR to adjust the reactive impedance of the AR to compensate for passive component mismatch.

An off-chip FPGA is used to modulate the duty-cycle of the AR switches in order to increase or decrease the real impedance of the AR and provide more or less power to the load. For that purpose, a proportional controller is utilized in the FPGA to produce the error signal V_{ERR} and regulate the output voltage. The control signals for the power FETs are generated by using this error signal and comparing it to the generated ramp. The edge-sensitive control of the proposed rectifier allows a flexible and reliable duty-cycle control.

The PLL is utilized to align and adjust the FETs gate drive signals relative to the delayed zero-crossing detector's output. Also, the system clock generated by the PLL is used by the

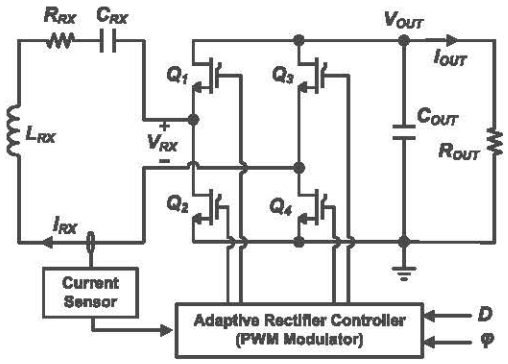


Fig. 5. Adaptive Rectifier circuit schematic.

saw-tooth generator, the output of which is used by the PWM comparator to compare the error voltage V_{ERR}, and generate FET control signals V_{G1}, V_{G2}, V_{G3}, and V_{G4}. Synchronous rectification relies on correct timing of gate signals that needs to be recovered from the input AC current signal by, for instance, detecting its zero current crossings. Zero current crossing detection generates the reference clock of the whole system. Any jitter, unintended delay or uncertainty in zero-crossing detection yields an inaccurate reference clock, which can cause efficiency loss or loss of regulation. To ensure correct timing of gate signals, the proposed receiver IC utilizes the zero-crossing detector circuit shown in Fig. 7, based on a high speed comparator. The circuit senses and digitizes the receiver current while passing through low-side FETs, Q_2 and Q_4.

The RX current is sensed by using sense resistors in series with low-side sense FETs. The main challenge of detecting the zero crossings of the rectifier current using sense resistors is that their size has to be chosen for optimal operation for accuracy, speed and efficiency. A smaller voltage swing at the input of comparator requires increase in accuracy specification (offset, etc.) for comparator design. Therefore, FETs and sense resistors need to be optimized for the best design trade-off. A benefit of using the suggested design for zero-crossing detection is that the comparator input signal can be bidirectional without having another circuit stage. This comparator consumes about 1 mA quiescent current to achieve a propagation delay of 700 ps in response to 5 mV input step. It has also 10 mV hysteresis to increase its immunity to noise. The offset of the comparator is kept below 15 mV (±3-sigma) for accurate detection.

The rising edge of the comparator signal is used as the reference clock edge for the PLL. Around the zero crossings, the zero-crossing detector can produce glitches due to the capacitive couplings or switching noise. In order to keep the PLL locked during the close-loop operation, the reference clock extracted from the zero crossings of the rectifier current must be free of glitches. This problem is solved by adding a deglitch of about 14 ns at the falling edge of the comparator output. This allows holding the comparator output for 14 ns when the comparator output changes from high to low and helps filtering any potential glitches around the zero crossings.

The phase control of the proposed receiver is achieved by introducing a phase lead or lag, based on the delay difference of the reference clock generated by the zero-crossing comparator and the feedback clock that controls the gate of the power FETs in the AR. For this purpose, the programmable delay circuit shown in Fig. 8 is incorporated. Depending on the desired delay or phase, the MUX selects one of these delayed signals and supplies to the PLL circuit. The difference of the delays introduced to the zero-crossing detector output and to the feedback clock sets the amount of phase lead or lag. The resolution of the programmable delay is set to about 1ns and the number of stages is set to 64.

The PLL based control scheme in the proposed AR design forces the gate driver signals to align with the zero-crossing of the rectifier current regardless of the delays of blocks in the feedback path. This helps the control loop to automatically compensate for Process-Voltage-Temperature variations in the design. In addition, the use of the PLL in this design allows for the system design to be relaxed against timing constraints imposed by the gate driver delay/strength. Moreover, since the PLL processes only edges, the proposed design becomes insensitive to the duty cycle of the zero crossings of the rectifier current signal. The PLL circuit shown in Fig. 8 consists of a Phase and Frequency Detector (PFD), a charge pump, and voltage controlled oscillator (VCO) circuits. A third-order charge-pump based PLL is used to take advantage of its noise rejection and lower steady-state error.

In order to suppress any charge sharing from the parasitic capacitances on the nodes connected to sink and source current sources they are biased by the unity-gain amplifier [31]. This helps avoiding any sink and source current mismatch that can result in a phase error and jitter. The ramp generator and the oscillator operate at 13.56 MHz to be able to generate the control signals for the active rectifier circuit. The ramp signal amplitude is controlled by a reference voltage, V_{PEAK}. The output of the comparator resets the ramp and restarts the integration at every clock cycle. This output is also fed to a flip flop to divide its frequency by two. The cross over frequency and phase of the PLL are set to 230 kHz and 70 degrees, respectively, to ensure the PLL stability and fast settling at 6.78 MHz operation. For that purpose, the main capacitor C_1 is set to 100 pF, while C_2 and R are set to 2.5 pF and 50 kΩ, to achieve the PLL compensation across process-voltage-supply corners.

The ramp signal used for generating the oscillator clock is also used for the PWM controller to generate the PWM signal. The duty cycle of the signal generated by this circuit becomes $D = V_{err}/V_{peak}$. The PWM comparator shown in Fig. 8 is a high speed and low quiescent current comparator based on [33] and used for oscillator as well. It is designed to consume less than 120 μA and have ~5 ns propagation delay to achieve fast speed and low quiescent current. The control signals for the power FETs in the AR circuit are then generated by using the divided down version of the VCO clock and PWM signals as illustrated in Fig. 8. A simplified first order dynamic model has been adopted to setup the AR control, based on the assumption that the WPT system does not require wide control bandwidth in low power battery charging applications of interest for the receiver chip presented in this paper. In particular, as discussed in Section II, the combination of (1) with one of

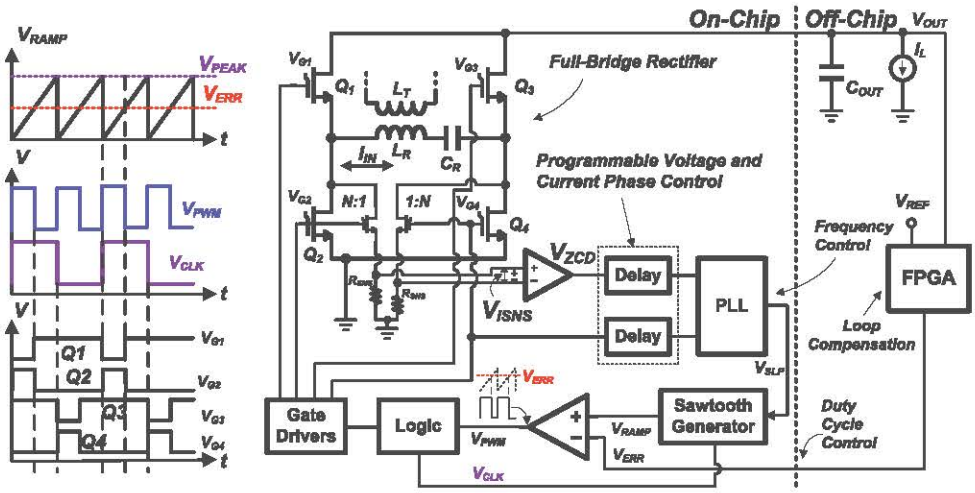


Fig. 6. Proposed adaptive rectifier circuit and waveforms of the critical control signals.

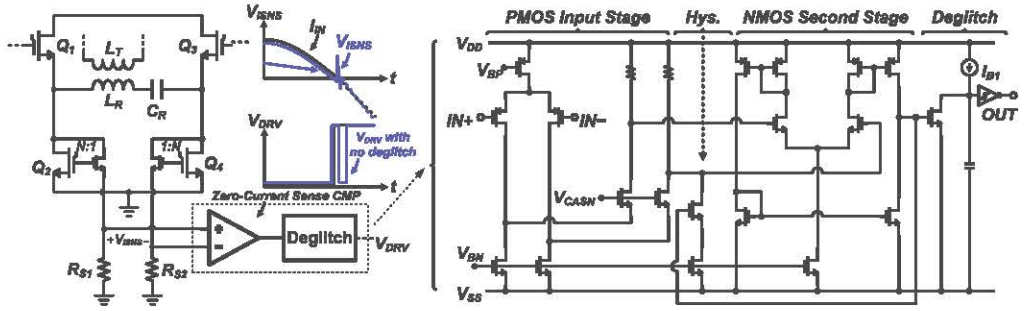


Fig. 7. Current sensing and comparator circuits.

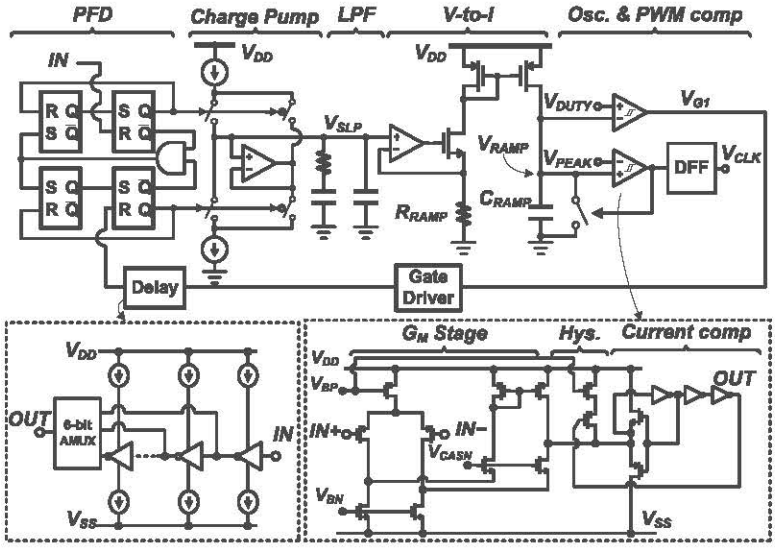
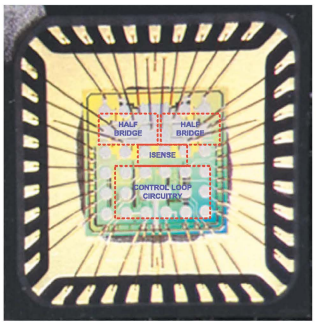
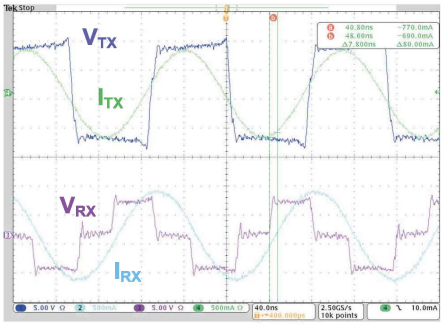


Fig. 8. PLL portion of the design including delay and comparator circuits.

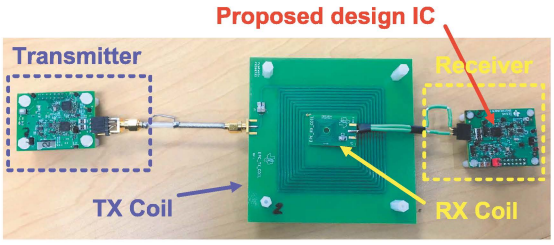
the equations in Table I allow to find the solution of the WPT system, providing the expression of the receiver current I_{RX} as a function of the load resistance R_{OUT}, of the input voltage V_{IN} and of the duty-cycle D. Therefore, for given load and input voltage conditions, the AC small-signal receiver current can be expressed as $\hat{i}_{RX} = H_d\hat{d}$, where $\hat{d}$ is the AC small-signal component of the duty-cycle and H_d depends on the DC operating conditions determined by R_{OUT}, V_{IN}



(a)



(b)



(c)

Fig. 9. (a) Die picture of the proposed active rectifier circuit. (b) Typical 6.78 MHz waveforms, with input current i_{L2} (cyan) and differential input voltage v_{rect}(magenta). (c) Adaptive rectifier test-chip in an open-cavity QFN package.

and D. The average rectifier output current is $2/\pi$ times the I_{RX} current and is injected into the parallel of the load resistance R_{OUT} and output capacitor impedance $1/(sC_{OUT})$. This yields a simplified duty-to-output voltage gain $\hat{v}_{OUT}/\hat{d}$, as given in (4):

$$\frac{\hat{v}_{OUT}}{\hat{d}} = \frac{2H_d}{\pi} \frac{R_{OUT}}{1 + sR_{OUT}C_{OUT}} \tag{4}$$

IV. Measurement Results

The proposed AR chip was fabricated in 0.18 μm BCD process. The die photo in an open-cavity QFN package and the location of main circuit components are shown in Fig. 9(a). The total die area of this IC is 7.56 mm^2 (2.75 mm $\times$ 2.75 mm) but only 3 mm^2 active die area is used for implementing the AR circuit. This active die area is partitioned in a way that 1.5 mm^2 is used for driver and power FETs while the other 1.5 mm^2 portion is allocated for analog and control circuitry.

Besides having less power components, this type of rectifier also offers an opportunity to reduce the silicon cost. Indeed, at all times, the maximum voltage sustained by FETs $Q_1, \ldots, Q_4$ is the output voltage, which is regulated by the rectifier itself and is in most applications lower than 5 V. The maximum operating voltage of the receiver is set to 9V by using the power FETs rated for 9 V. These power FETs are sized to have nominal channel resistance of 240 mΩ. The AR IC can regulate the output from 3.5 V to 5V (9 V absolute max) for 500 mA maximum load current. The TX and RX current and differential voltage waveforms are also shown in Fig. 9(b) for the case where duty cycle of the transmitter is powered with 8 V input and receiver is adjusted to regulate output voltage to 4 V. Also, a phase shift is introduced to the receiver to achieve the optimum operating point for the system efficiency and power transfer. The experimental set-up shown in Fig. 9(c) has been employed to characterize the AR across different system conditions and to collect data across multiple duty-cycles and phase values. A 2 W LED is adopted to load the AR. An FPGA is used to control the system parameters in the experimental setup in order to have better capability of jointly controlling output, duty-cycle and phase. The error amp implemented in the FPGA has allowed for taking the experimental data across various operating conditions. Also, phase is controlled by changing the programmable delay settings through the FPGA. Once desired system dynamics are well-defined for a specific application, the error amp and compensation components can also be integrated into the receiver IC. RX and TX coils are used for the wireless power transfer across different angle and spatial locations. The TX coil is built using 1.7 oz/sqft copper PCB and sized to 70 mm $\times$ 70 mm with 9 turns. Its measured quality factor is 156. Its measured inductance and self-resonance frequency are 6.76 μH and 20 MHz, respectively. The RX coil is designed using 1-layer and 1.7 oz/sqft copper PCB coil and sized to 15 mm $\times$ 15mm with 8 turns to have its inductance around 0.9 μH. The measured quality factor of the RX coil is 47, while its measured self-resonance is 73 MHz. The RX is also suitable for higher power applications, but geometry of the coils needs to be adjusted to meet the requirements of the specific high power application.

The proposed AR was tested in a 2.5 W and 50% efficient wireless power system, with a coupling coefficient of the TX and RX coils of $k = 0.085$ (*case study I*). As the power delivered to the load approaches zero, the AR can operate either at zero duty-cycle and arbitrary phase or arbitrary duty-cycle and phase equal to $\pi/2$ radians. The first strategy creates a series L-C tank with substantial (but limited) circulating current, which induces EMF on the TX coil. This reduces the TX current, limiting ohmic losses in the system. The second strategy detunes receiver and transmitter tank, in most cases reducing system losses even further. In a commercial product, the TX current can be dynamically optimized in many different ways. The proposed AR is characterized in this experimental setup with input supply voltage V_s set to 8 V and regulated output voltage loaded with two red LEDs in series (4 V total). The other system parameters are set as $R_s = 0.3\ \Omega$, $L_{TX} = 7.5\ \mu$H, $R_{TX} = 2\ \Omega$, $L_{RX} = 0.95\ \mu$H and $R_{RX} = 1.1\ \Omega$. C_{TX} has 1% and

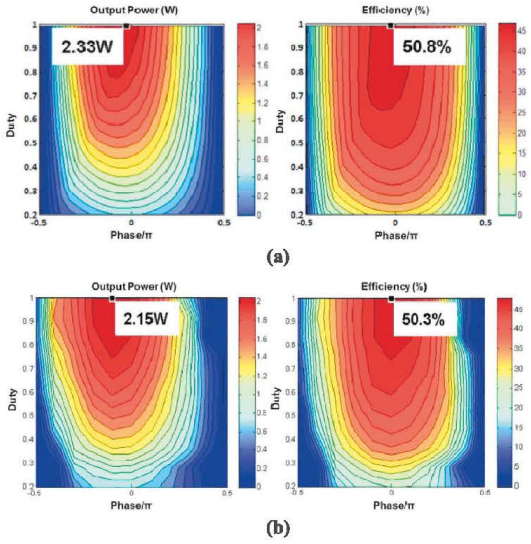


Fig. 10. Output power and efficiency of the system using the proposed adaptive rectifier. RX coil is aligned with the center of the TX coil ($k = 0.085$). (a) Simulation results based on the system model. (b) Experimental results.

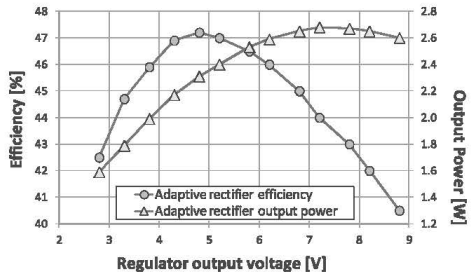


Fig. 11. System efficiency and output power vs output voltage achieved with the proposed AR ($k = 0.076$).

C_{RX} has 5% mismatches with respect to their nominal value. Fig. 10 shows the simulation and experimental results for the output power and system efficiency. The simulations done using the model closely predict the experimental data. As shown in Fig. 10(a), the system model estimates 2.33 W of maximum power at 50.8% system conversion efficiency. Similarly, the experimental results show that the maximum output power is 2.15 W at 50.3% system conversion efficiency, as shown in Fig. 10(b). These data are all measured with RX coil aligned with the center of the TX coil ($k = 0.085$). As typical in all WPT systems, the above values of efficiency can be influenced by PCB parasitic losses.

The proposed AR is also characterized in a WPT system with $k = 0.076$ (*case study II*) and over the output voltage operability range from 2.8 V to 8.8 V. The measured efficiency and delivered output power of the proposed AR are shown in Fig. 11. For these conditions, a maximum of 47.2% WPT system efficiency is achieved at 4.8 V rectifier output voltage while delivering 2.31 W, and a maximum of 2.68 W power is delivered at 44% WPT system efficiency and 7.2 V rectifier output voltage.

The spatial freedom provided by the proposed AR is also demonstrated by using it in a low coupling setup.

TABLE II

INPUT/OUTPUT POWER AND EFFICIENCY FOR TWO DUTY-CYCLE AND PHASE SETTINGS AND POWER DISSIPATION DISTRIBUTION

	Condition I: D=1, φ=0		**Condition II: D=0.43, φ=0.19 ($1/\pi$)**	
Parameters	***Simulation***	***Bench test***	***Simulation***	***Bench test***
$I_{ac,in,rms}$ [A]	0.550	0.550	0.620	0.629
$V_{ac,in,rms}$ [V]	4.919	4.913	3.207	3.237
$P_{ac,in}$ [W]	2.435	2.432	1.550	1.573
I_{out} [A]	0.505	0.505	0.291	0.289
V_{out} [V]	4.646	4.643	4.231	4.196
P_{out} [W]	2.346	2.345	1.235	1.213
P_{cond} [W]	0.070	-	0.112	-
P_{gate} [W]	0.016	-	0.011	-
P_{sw} [W]	0.003	-	0.191	-
Receiver Efficiency [%]	96.35	96.42	79.68	77.11

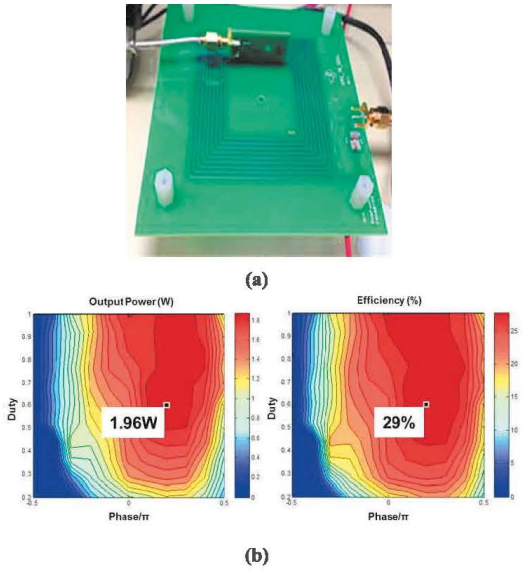


Fig. 12. (a) Experimental setup illustrating receiver coil location and orientation. RX coil is placed at the side of the TX coil with an angle of 80 degree ($k = 0.03$). (b) Receiver coil Output power (left) and efficiency (right) of the system using the proposed adaptive rectifier.

Fig. 12(a) shows the RX coil placed at the side of the TX coil, with an angle of 80 degrees and a coupling coefficient $k = 0.03$ (*case study III*). Fig. 12(b) shows the experimental data collected in such low coupling condition. The adaptive tuning technique appears particularly effective: 1.96 W output power can be achieved at 29% system efficiency. Impedance matching, and thus maximum power point transfer (MPPT), is achieved at ~0.6 duty-cycle and with a slight phase-shift to compensate for resonant capacitors mismatch. It is worth to note that the proposed AR IC solution allows for programming both the phase and the duty-cycle (see Fig. 5) to modulate the load impedance seen from the input of the rectifier. This feature can be exploited for MPPT, as the AR IC can monitor the rectifier output power by sensing output voltage and load current, and search for MPPT by adjusting phase and/or duty-cycle.

TABLE III
PROPOSED RECTIFIER VS. PRIOR ART

	This work	[10]	[26]	[33]	[34]	[35]
Receiver structure	Adaptive rectifier	Regulating rectifier	Rectifier +buck	R^3 rectifier	Boost +AR	Rectifier +buck
Coil type	Resonant	Resonant	Resonant	Resonant	Resonant	Resonant
Max. output power	2.5 W	6 W	6 W	6 W	1 W	5 W
Carrier	6.78 MHz	6.78 MHz	6.78 MHz	6.78 MHz	6.78 MHz	6.78 MHz
Receiver efficiency	96%	86%	84.6 %	92.2%	>50%	81%
Distance	7 mm	NA	7 mm	NA	1 mm	NA
Active Die Area	3 mm^2	5.52 mm^2	14.44 mm^2	4.77 mm^2	6.25 mm^2	6.25 mm^2
Power density	1200 mW/mm^2	NA	415 mW/mm^2	1257 mW/mm^2	160 mW/mm^2	800 mW/mm^2
Process	0.18 µm BCD	0.35 µm BCD	0.13 µm BCD	0.35 µm CMOS	0.18 µm CMOS	0.18 µm BCD
Off chip components	1 capacitor	5 diodes and 3 capacitors	1 inductor and 2 capacitors	1 capacitor	1 capacitor	1 inductor and 2 capacitors
Protection circuit	Not needed	Schottky diode	**NA**	**NA**	**NA**	By SPC

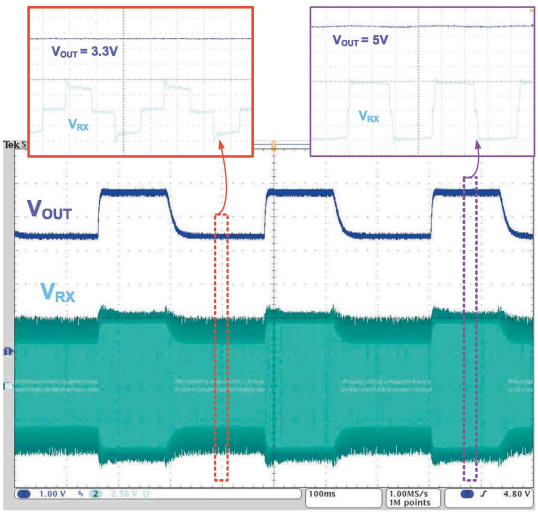


Fig. 13. Output voltage regulation achieved by using the proposed AR. Output voltage setting is changed by changing the duty-cycle periodically to regulate output to 3.3V or 5V.

The efficiency of the receiver IC is measured and compared with simulation results for two conditions. The first condition is set for duty-cycle $D = 100\%$ with phase $\varphi = 0°$, which yield ~96% (simulated and measured) receiver efficiency for output voltage of ~4.64V. For this condition, the conduction power loss dominates other losses. The second condition is set for duty-cycle $D = 43\%$ with phase $\varphi = 34°$, which results in 79.6% (simulated) and 77% (measured) receiver efficiency for rectifier output voltage of ~4.2V. For this duty cycle and phase condition, the switching loss becomes more than the other losses. For these two conditions, the simulated conduction, gate and switching losses are reported in Table II. The receiver efficiency represents the conversion efficiency of the receiver from the rectifier input to its output. The WPT system efficiency is much lower compared to receiver efficiency, due to low coupling factor of the systems of interest in this paper. Thus, only a fraction of the power can be transferred from the TX to the RX side. Moreover, the losses in the inverter and in the coils also impact the overall efficiency.

Table III shows the performance of the proposed rectifier compared with prior art. In particular, the AR discussed in this paper has been compared to previous literature works designed for 1W, 5W and 6W ([10], [26], and [33]–[35]) in order to show the differences between architectures in terms of power density, number of external components and protection capabilities. While these solutions are designed for different power values and require bigger die areas for higher power, size impact of these architectures has been showed by reporting their power density while quoting their active die area and process. The proposed solution achieves a power density level which is comparable to the best of the higher power solutions [33], but with higher efficiency, and is much higher than the power density of the lower power solution discussed in [34], with higher efficiency as well. The number of off-chip components is just one, which also shows the impact of the proposed architecture in system size. In addition, the protection capability of the proposed AR shows technological advance of this architecture at 6.78 MHz operation. The AR does not require over-voltage protection circuitry, as it inherently operates by imposing low load impedance to the output of receiver coil. In normal operation, the receiver coil is clamped to the output voltage, which is the voltage of battery under charge. The feedback loop keeps the output regulated ensuring that, when the charge of the battery is complete and the no-load condition is reached, the duty-cycle is reduced to zero. In this condition, the coil is shorted, through the rectifier FETs Q_2 and Q_4, to stop the energy transfer to the output. This prevents the over-voltage condition by inherently limiting the maximum voltage peak. In addition, voltage on Q_1 and Q_3 switches is always clamped by the output voltage. As a result, the FETs voltage rating can be kept low. To avoid unstable operation during the startup, power FETs are kept off until the rectifier output voltage reaches around 2.5 V to have enough headroom for the receiver IC to operate properly and its functional blocks to settle for their initial operating conditions. Once the rectifier output is higher than 2 V, PLL is started to synchronize the zero-cross detector output with the bypassed V_{G4} (while Q_4 is kept turned off) for its initialization and fast settling before closed loop control is enabled.

Fig. 13 illustrates the duty-cycle control of the close-loop system, where the regulated output voltage is changed by periodically changing the duty-cycle. The time response shown in Fig. 13 aligns with the expected behavior given in (4) and shows that the simplified first order model approximates the real system behavior sufficiently well for practical narrow bandwidth control design purposes.

V. Conclusions

The single-stage full-bridge synchronous Adaptive Rectifier (AR) offers better performance and cost trade-off compared to other double-stage full-bridge Post-Regulated Rectifier (PRR) architectures in low power WPT systems. This paper shows that the AR solution in loosely coupled WPT systems is comparable to PRR solutions in terms of WPT system efficiency, while offering the advantage of lower part count and wider operation range. The AR solution also provides better system flexibility to deal with mismatches, whereas PRR solutions inherently lack robustness against WPT system uncertainties and power control flexibility. Moreover, all power switches in the PRR must be rated for higher peak voltage, while AR can operate with low-voltage switches. The AR chip presented in this paper was implemented in 0.18 μm BCD process to be used as receiver IC for WPT systems that require low system footprint and complexity, and low silicon cost. This chip enables high-frequency operation, autonomous receiver-side power control, active receiver-side impedance tuning, and adaptability to varying coupling coefficients. Experimental results prove the 6.78 MHz WPT system operation at low coupling coefficients with about 50% system efficiency while delivering up to 2.5 W and enabling small solution size.

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